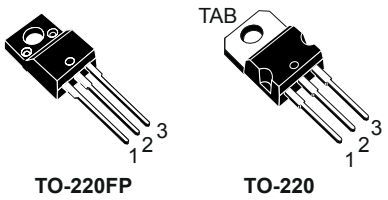
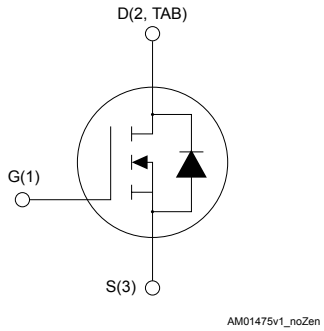
STF16N65M5, STP16N65M5

Datasheet

N-channel 650 V, 230 mΩ typ., 12 A MDmesh M5 Power MOSFETs in a TO-220FP and TO-220 packages



TO-220FP **TO-220**



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF16N65M5	650 V	279 mΩ	12 A
STP16N65M5			

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links
STF16N65M5
STP16N65M5

Product summary	
Order code	**STF16N65M5**
Marking	16N65M5
Package	TO-220FP
Packing	Tube
Order code	**STP16N65M5**
Marking	16N65M5
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
V_{DS}	Drain-source voltage	650		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	12		A
	Drain current (continuous) at T_C = 100 °C	7.3		
I_{DM}(1)	Drain current (pulsed)	48		A
P_{TOT}	Total power dissipation at T_C = 25 °C	90	25	W
dv/dt(2)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	-	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Maximum operating junction temperature	150		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 12 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	5	1.38	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A	-	230	279	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1250	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	100	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	30	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 6 A, V_{GS} = 0 to 10 V (see the Figure 17. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	25	-	ns
$t_{r(v)}$	Voltage rise time		-	7	-	ns
$t_{f(i)}$	Current fall time		-	6	-	ns
$t_{c(off)}$	Crossing time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	12	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	48	A
V_{SD}(2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	300	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	3.5	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	23	-	A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	350	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	4	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	24	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

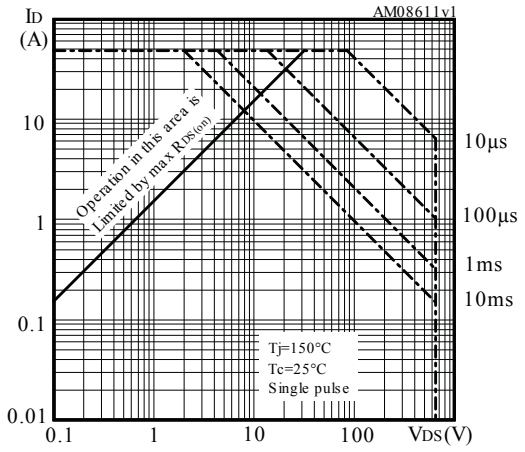


Figure 2. Normalized transient thermal impedance for TO-220FP

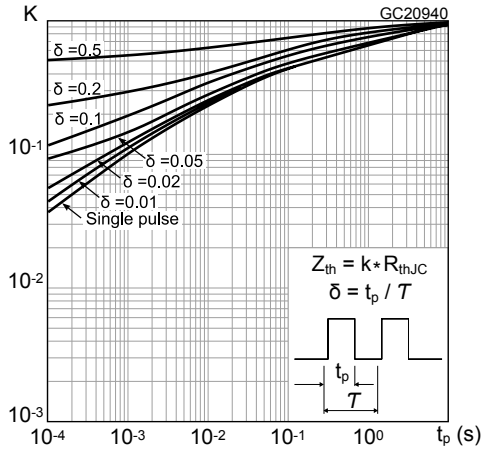


Figure 3. Safe operating area for TO-220

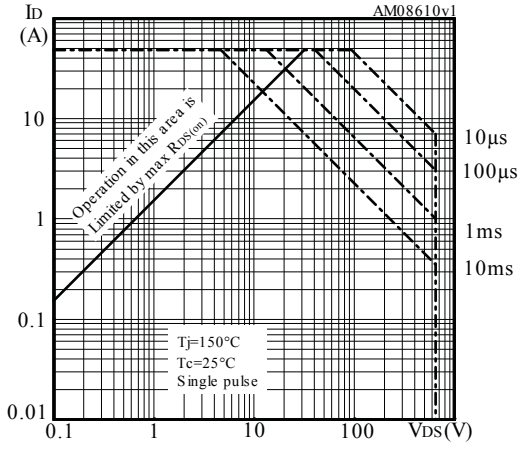


Figure 4. Normalized transient thermal impedance for TO-220

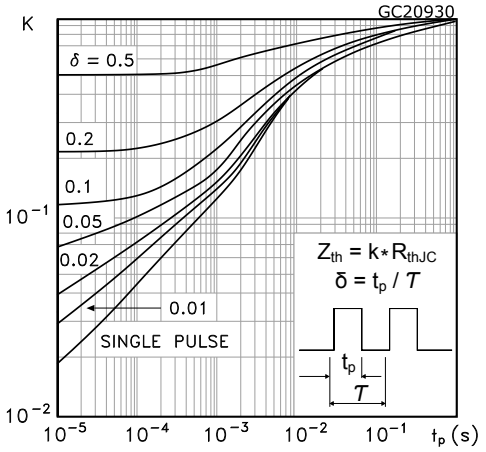


Figure 5. Typical output characteristics

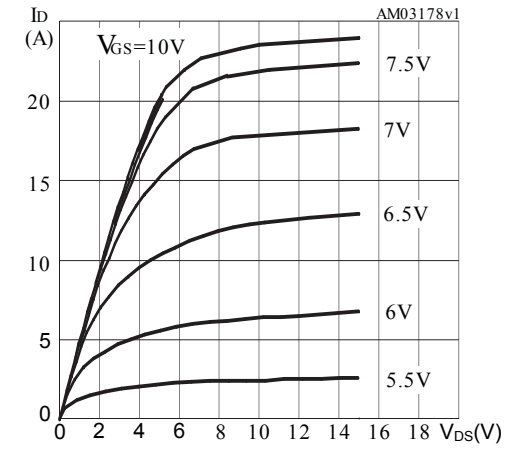


Figure 6. Typical transfer characteristics

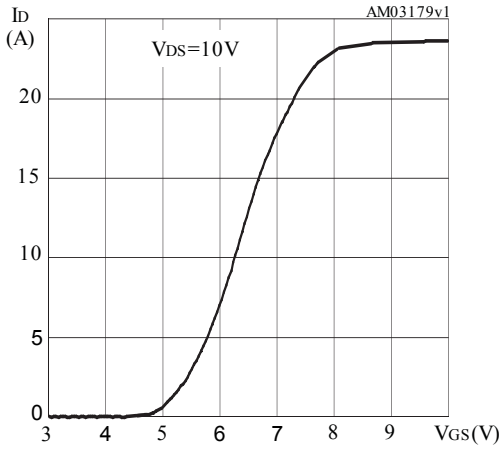


Figure 7. Typical gate charge characteristics

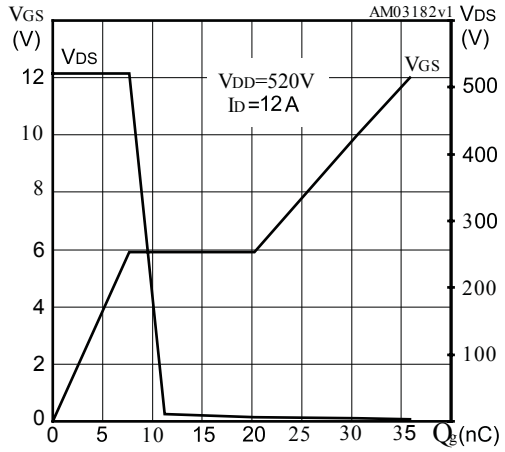


Figure 8. Typical drain-source on-resistance

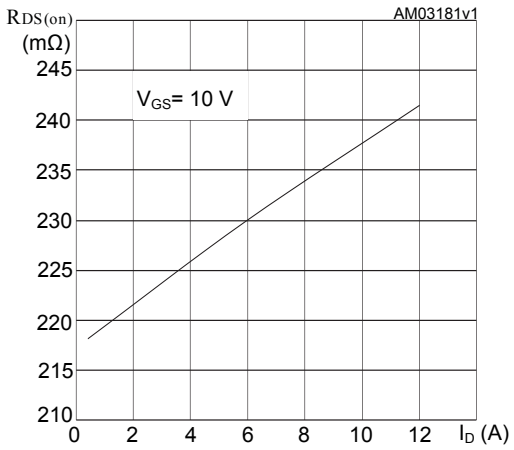


Figure 9. Typical capacitance characteristics

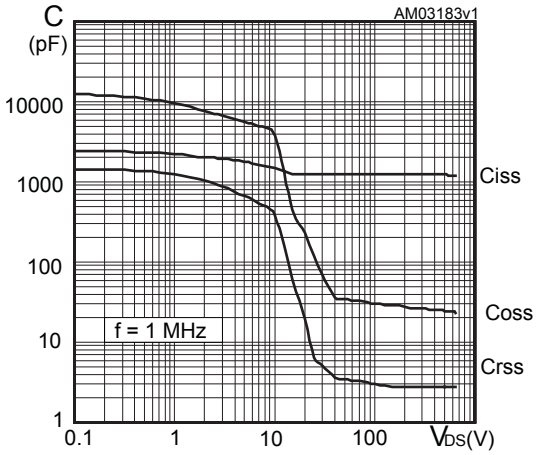


Figure 10. Typical output capacitance stored energy

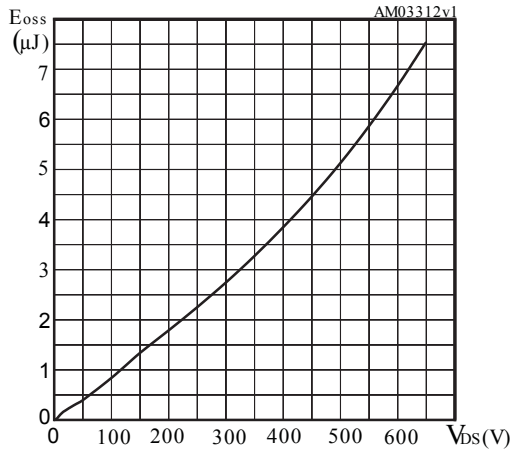


Figure 11. Normalized gate threshold vs temperature

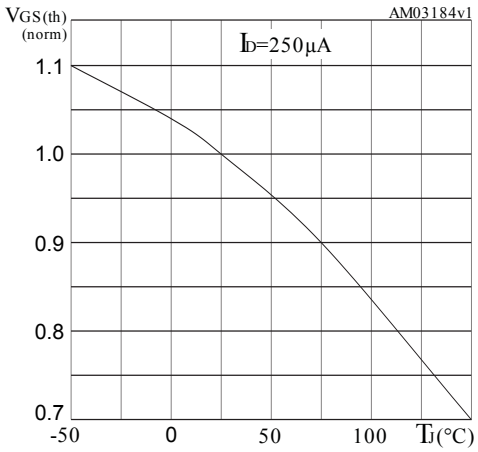


Figure 12. Normalized on-resistance vs temperature

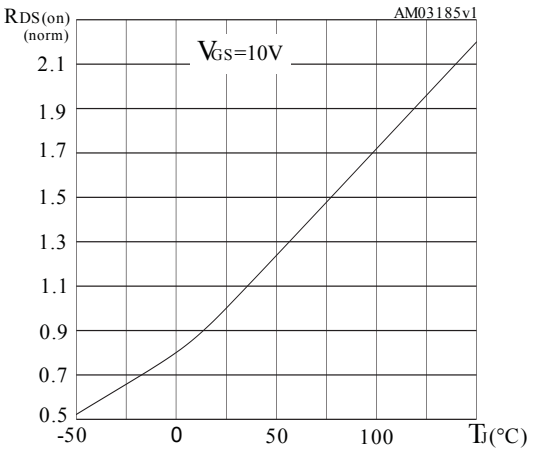


Figure 13. Typical reverse diode forward characteristics

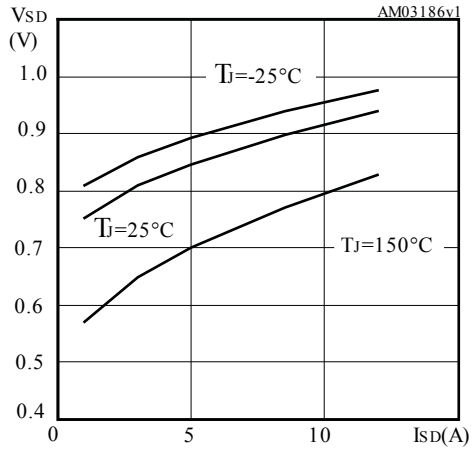


Figure 14. Normalized breakdown voltage vs temperature

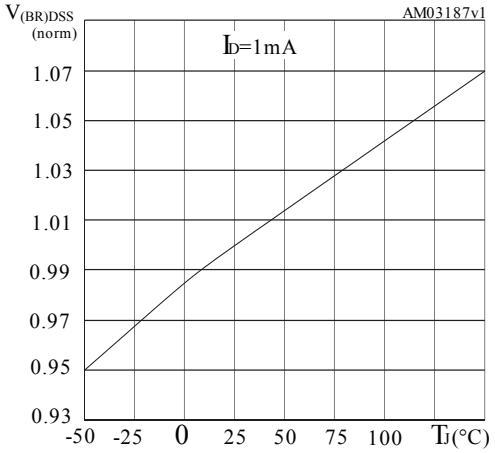
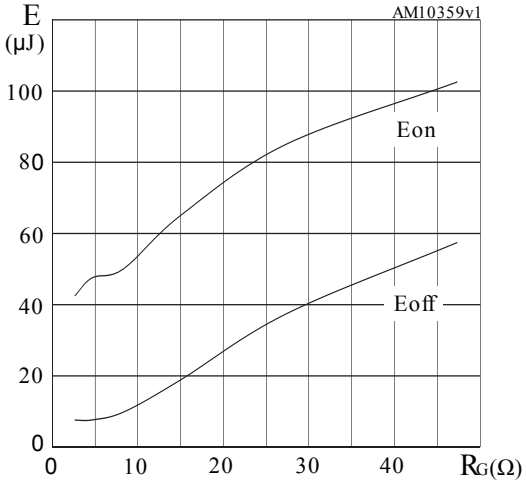


Figure 15. Typical switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 16. Test circuit for resistive load switching times

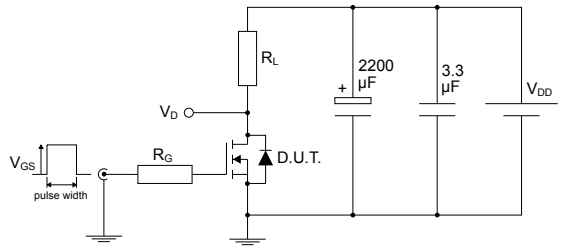


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Figure 17. Test circuit for gate charge behavior

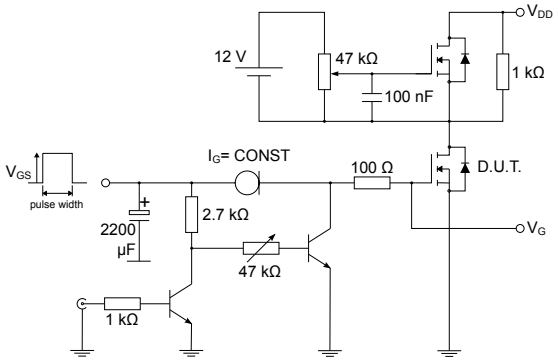

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Figure 18. Test circuit for inductive load switching and diode recovery times

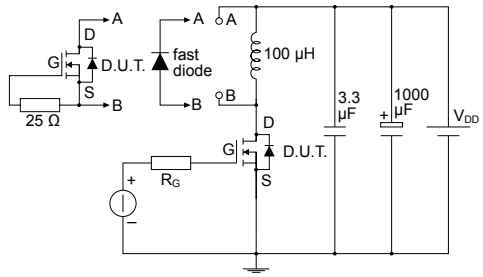

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Figure 19. Unclamped inductive load test circuit

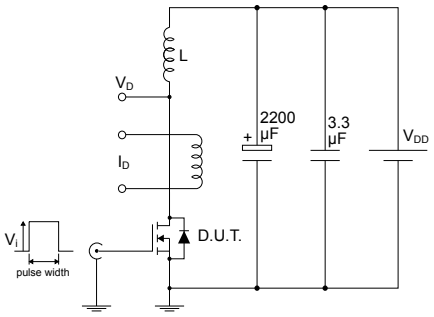

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Figure 20. Unclamped inductive waveform

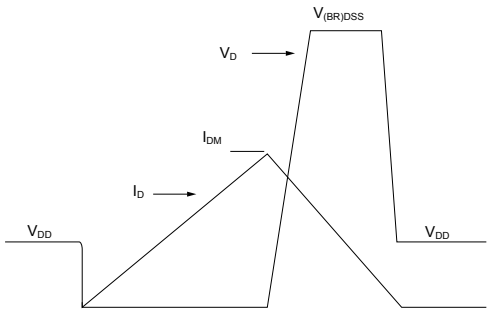

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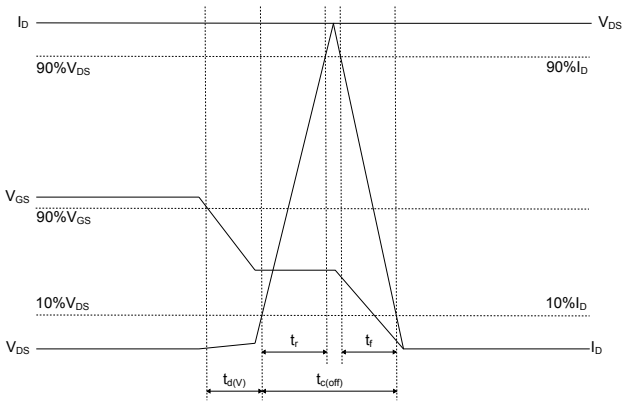
Figure 21. Switching time waveform



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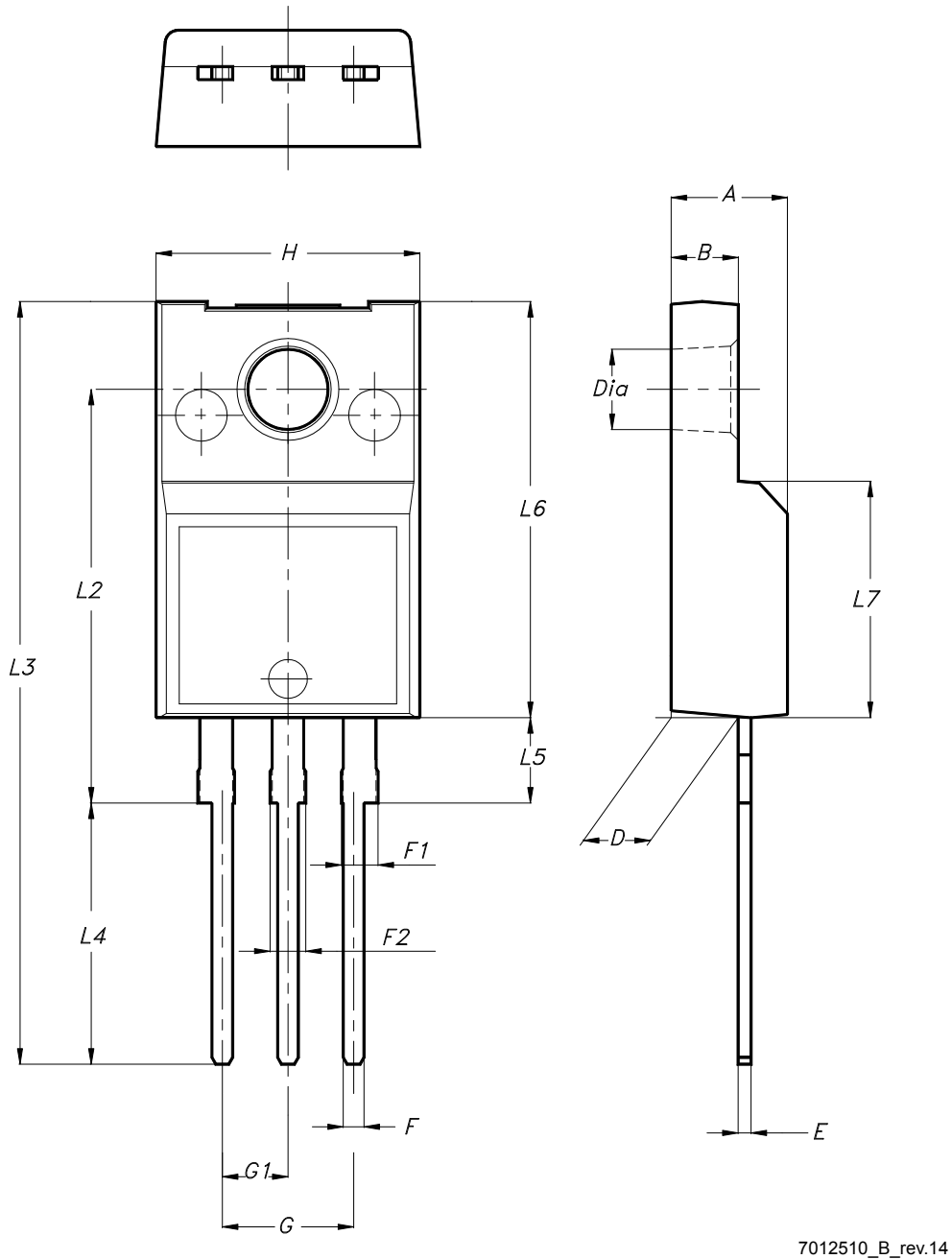
4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 22. TO-220FP type B package outline



7012510_B_rev.14

Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-220 type A package information

Figure 23. **TO-220 type A package outline**

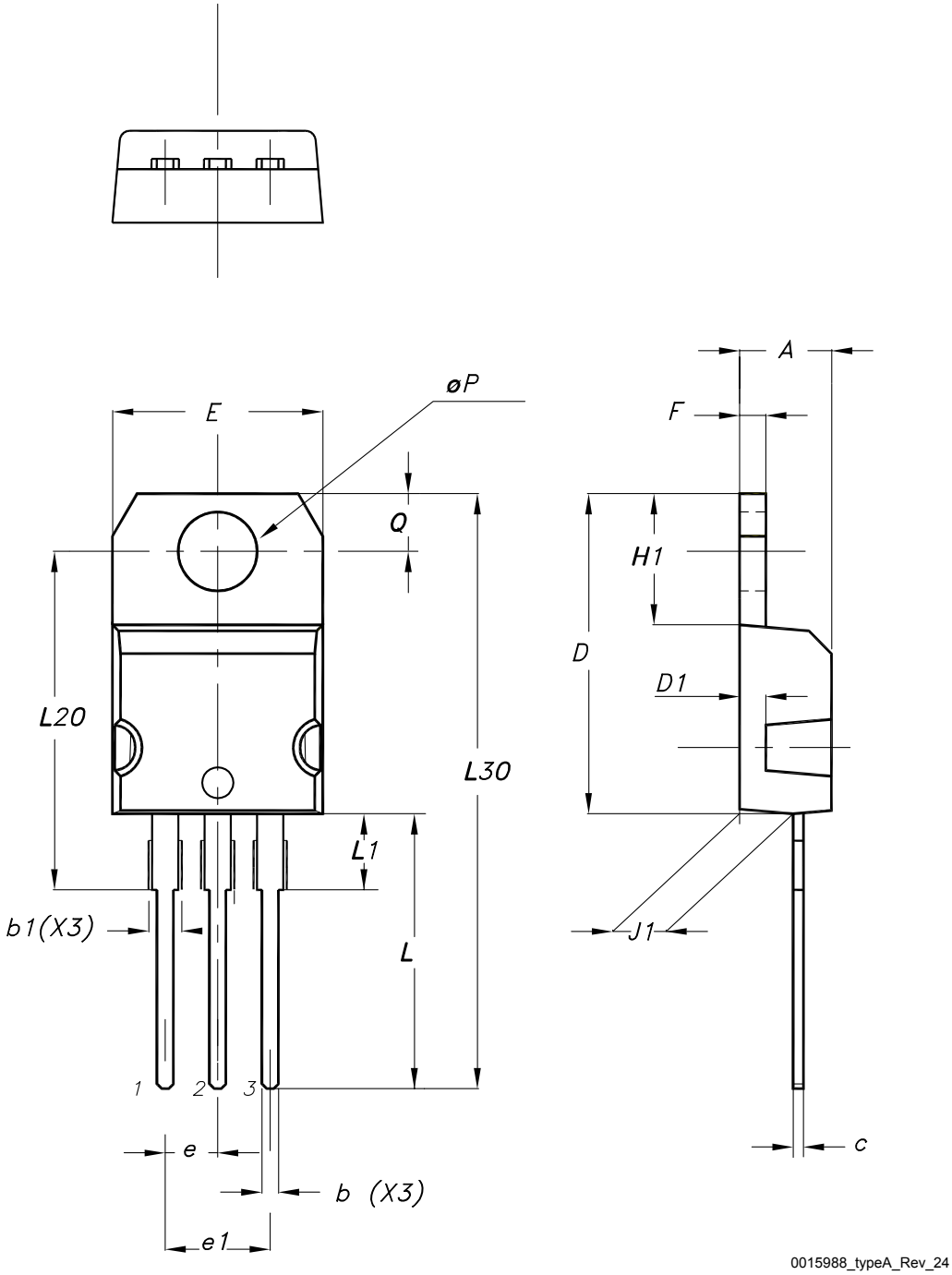


Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
12-Feb-2009	1	First release.
21-Oct-2010	2	Document status promoted from preliminary data to datasheet. Added new package, mechanical data: I²PAK. Removed DPAK, D²PAK packages and mechanical data.
10-Feb-2011	3	Modified $R_{DS(on)}$ value (see *Table 4* and *Figure 11*).
13-Oct-2011	4	Modified *Section 2.1: Electrical characteristics (curves)*: *Figure 8*, *Figure 9*, *Figure 10*, *Figure 11*, *Figure 15* and *Figure 16*. Added *Figure 18*. Updated $R_{DS(on)}$ value in *Table 4*. Updated values in *Table 6*. Minor text changes.
03-Feb-2026	5	Removed order code STI16N65M5, STU16N65M5 and STW16N65M5. Updated Section 4: Package information. Minor text changes.

Contents