ESP32-S2-SOLO-2
ESP32-S2-SOLO-2U

Datasheet Version 1.3

2.4 GHz Wi-Fi (802.11 b/g/n) module
Built around ESP32-S2 series of SoC, Xtensa® single-core 32-bit LX7 microprocessor
Flash up to 16 MB, optional 2 MB PSRAM in chip package
36 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector

ESP32-S2-SOLO-2

ESP32-S2-SOLO-2U

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-s2-solo-2_esp32-s2-solo-2u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S2 or ESP32-S2R2 embedded, Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC
- 2 MB PSRAM (ESP32-S2R2 only)

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Peripherals

- Up to 36 GPIOs
- SPI, LCD, UART, I2C, I2S, Camera interface, IR, pulse counter, LED PWM, TWAI® (compatible with ISO 11898-1, i.e. CAN Specification 2.0), full-speed USB OTG, ADC, DAC, touch sensor, temperature sensor, general-purpose timers, watchdog timers

Note:

* Please refer to *ESP32-S2 Series Datasheet* for detailed information about the module peripherals.

Integrated Components on Module

- 40 MHz crystal oscillator
- Quad SPI flash up to 16 MB

Antenna Options

- ESP32-S2-SOLO-2: On-board PCB antenna
- ESP32-S2-SOLO-2U: External antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
  - 85 °C version: −40 ~ 85 °C
  - 105 °C version: −40 ~ 105 °C (ESP32-S2-SOLO-2-H4 and ESP32-S2-SOLO-2U-H4 only)

Certification

- RF certification: See certificates
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD/Latch-up

1.2 Series Comparison

ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

ESP32-S2-SOLO-2 comes with a PCB antenna (ANT). ESP32-S2-SOLO-2U comes with an external antenna connector (CONN).

A wide selection of module variants are available. The variant nomenclature is shown in Figure 1-1, and the series comparisons are listed in Table 1-1 and Table 1-2.

The nomenclature for the module variants is as follows:

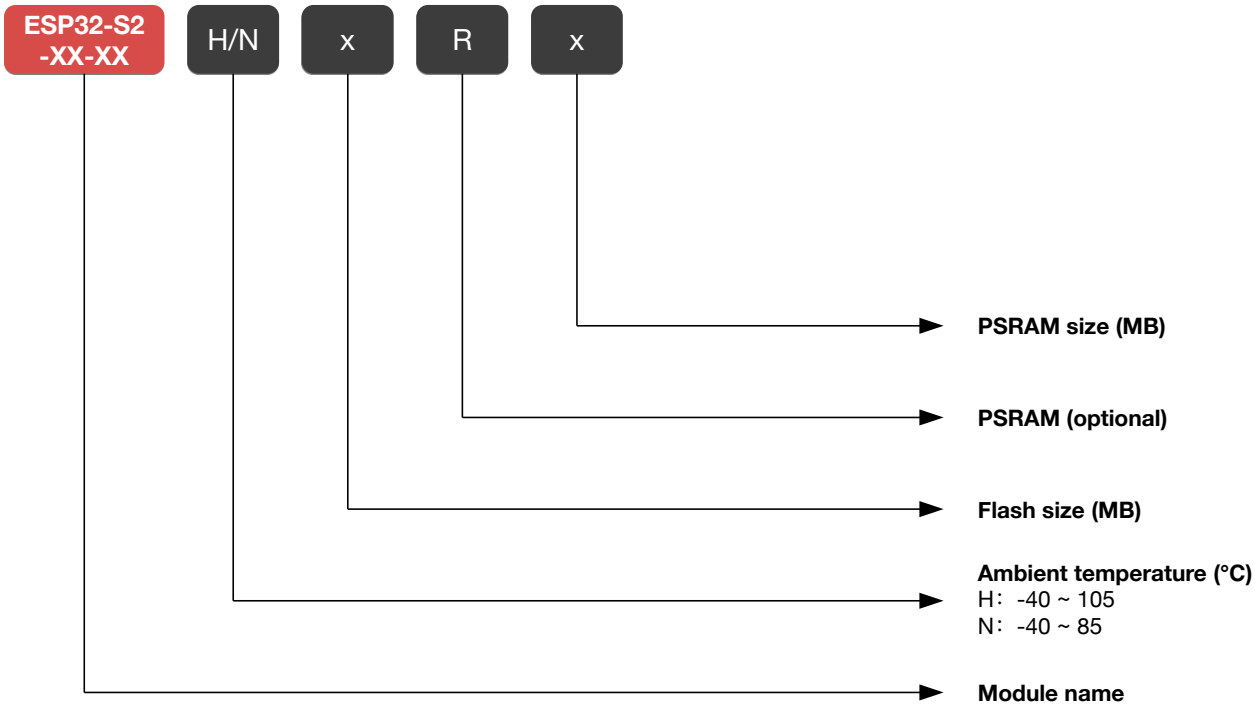

Figure 1-1. ESP32-S2 Module Variant Nomenclature

Table 1-1. ESP32-S2-SOLO-2 (ANT) Series Comparison

Ordering Code	Flash[3]	PSRAM[3]	Ambient Temp.[1] (°C)	Size[2] (mm)
ESP32-S2-SOLO-2-N4	4 MB (Quad SPI)	—	−40 ~ 85	18.0 × 25.5 × 3.1
ESP32-S2-SOLO-2-H4 (End of life)		—	−40 ~ 105	
ESP32-S2-SOLO-2-N4R2		2 MB (Quad SPI)	−40 ~ 85	
ESP32-S2-SOLO-2-N8 (End of life)	8 MB (Quad SPI)	—		
ESP32-S2-SOLO-2-N16	16 MB (Quad SPI)	—		

[1] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[2] For details, refer to Section 9.1 *Module Dimensions*.

[3] For specifications, refer to Section 5.5 *Memory Specifications*.

Table 1-2. ESP32-S2-SOLO-2U (CONN) Series Comparison[1]

Ordering Code	Flash	PSRAM	Ambient Temp. (°C)	Size (mm)
ESP32-S2-SOLO-2U-N4	4 MB (Quad SPI)	—	−40 ~ 85	18.0 × 19.2 × 3.2
ESP32-S2-SOLO-2U-H4		—	−40 ~ 105	
ESP32-S2-SOLO-2U-N4R2		2 MB (Quad SPI)	−40 ~ 85	
ESP32-S2-SOLO-2U-N16	16 MB (Quad SPI)	—		

[4] This table shares the same notes presented in Table 1-1 above.

In this datasheet unless otherwise stated, ESP32-S2-SOLO-2 refers to all variants of ESP32-S2-SOLO-2, whereas ESP32-S2-SOLO-2U refers to all variants of ESP32-S2-SOLO-2U.

At the core of the modules is ESP32-S2 series chip revision v1.0. ESP32-S2 series of chips has an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. It has a low-power co-processor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals.

Note:
For more information on ESP32-S2R2, please refer to *ESP32-S2 Series Datasheet*.
For chip revision identification, ESP-IDF release that supports a specific chip revision, and other information on chip revisions, please refer to *ESP32-S2 Series SoC Errata* > Section *Chip Revision*.

1.3 Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices

- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

Contents

1 Module Overview 2
1.1 Features 2
1.2 Series Comparison 3
1.3 Applications 4
2 Block Diagram 10
3 Pin Definitions 11
3.1 Pin Layout 11
3.2 Pin Description 11
4 Boot Configurations 14
4.1 Chip Boot Mode Control 15
4.2 VDD_SPI Voltage Control 15
4.3 ROM Messages Printing Control 16
4.4 Chip Power-up and Reset 16
5 Electrical Characteristics 18
5.1 Absolute Maximum Ratings 18
5.2 Recommended Operating Conditions 18
5.3 DC Characteristics (3.3 V, 25 °C) 18
5.4 Current Consumption Characteristics 19
5.4.1 Current Consumption in Active Mode 19
5.4.2 Current Consumption in Other Modes 19
5.5 Memory Specifications 20
6 RF Characteristics 22
6.1 Wi-Fi Radio 22
6.1.1 Wi-Fi RF Standards 22
6.1.2 Wi-Fi RF Transmitter (TX) Specifications 22
6.1.3 Wi-Fi RF Receiver (RX) Specifications 23
7 Module Schematics 25
8 Peripheral Schematics 27
9 Physical Dimensions 28
9.1 Module Dimensions 28
9.2 Dimensions of External Antenna Connector 29
10 PCB Layout Recommendations 31
10.1 PCB Land Pattern 31
10.2 Module Placement for PCB Design 32

11 Product Handling 33
11.1 Storage Conditions 33
11.2 Electrostatic Discharge (ESD) 33
11.3 Soldering Profiles 33
11.3.1 Reflow Profile 33
11.3.2 Wave Profile 34
11.4 Ultrasonic Vibration 34

Datasheet Versioning 35

Related Documentation and Resources 36

Revision History 38

List of Tables

1-1 ESP32-S2-SOLO-2 (ANT) Series Comparison 4
1-2 ESP32-S2-SOLO-2U (CONN) Series Comparison[1] 4
3-1 Pin Definitions 12
4-1 Default Configuration of Strapping Pins 14
4-2 Description of Timing Parameters for the Strapping Pins 15
4-3 Chip Boot Mode Control 15
4-4 VDD_SPI Voltage Control 16
4-5 UART ROM Message Printing Control 16
4-6 Description of Timing Parameters for Power-up and Reset 17
5-1 Absolute Maximum Ratings 18
5-2 Recommended Operating Conditions 18
5-3 DC Characteristics (3.3 V, 25 °C) 18
5-4 RF Current Consumption in Active Mode 19
5-5 Current Consumption in Modem-sleep Mode 20
5-6 Current Consumption in Low-Power Modes 20
5-7 Flash Specifications 20
5-8 PSRAM Specifications 21
6-1 Wi-Fi RF Standards 22
6-2 TX Power with Spectral Mask and EVM Meeting 802.11 Standards 22
6-3 TX EVM Test 23
6-4 RX Sensitivity 23
6-5 Maximum RX Level 24
6-6 RX Adjacent Channel Rejection 24

List of Figures

1-1 ESP32-S2 Module Variant Nomenclature 3
2-1 ESP32-S2-SOLO-2 Block Diagram 10
2-2 ESP32-S2-SOLO-2U Block Diagram 10
3-1 Pin Layout (Top View) 11
4-1 Visualization of Timing Parameters for the Strapping Pins 15
4-2 Visualization of Timing Parameters for Power-up and Reset 17
7-1 ESP32-S2-SOLO-2 Schematics 25
7-2 ESP32-S2-SOLO-2U Schematics 26
8-1 Peripheral Schematics 27
9-1 ESP32-S2-SOLO-2 Physical Dimensions 28
9-2 ESP32-S2-SOLO-2U Physical Dimensions 28
9-3 Dimensions of External Antenna Connector 29
10-1 ESP32-S2-SOLO-2 Recommended PCB Land Pattern 31
10-2 ESP32-S2-SOLO-2U Recommended PCB Land Pattern 32
11-1 Reflow Profile 33
11-2 Wave Soldering Profile 34

2 Block Diagram

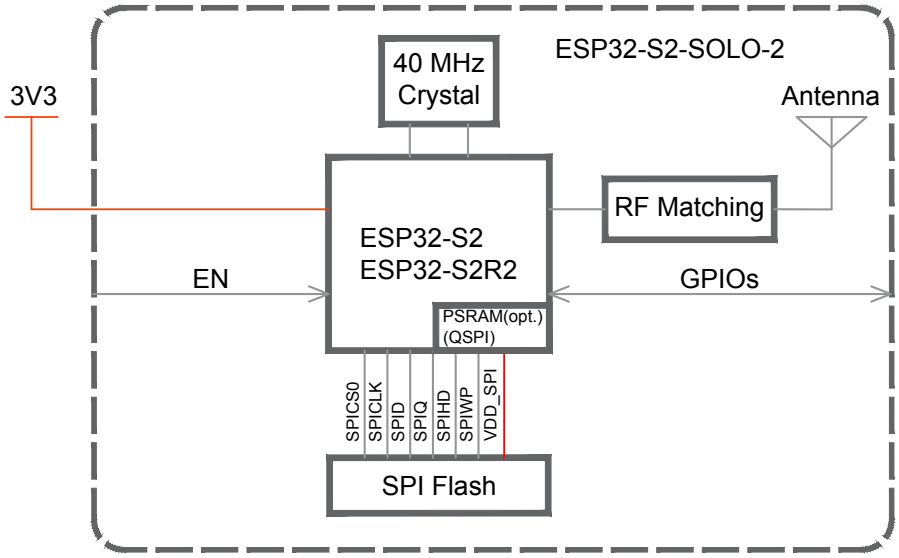

Figure 2-1. ESP32-S2-SOLO-2 Block Diagram

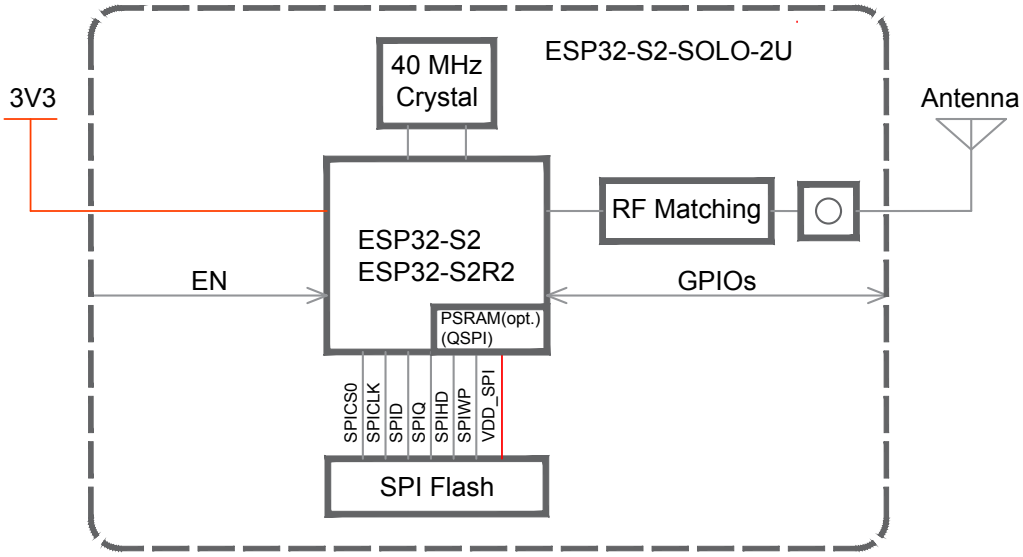

Figure 2-2. ESP32-S2-SOLO-2U Block Diagram

Note:

For the pin mapping between the chip and the in-package flash/PSRAM, please refer to *ESP32-S2 Series Datasheet* > Table *Pin Mapping Between Chip and In-package Flash/PSRAM*.

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 9.1 *Module Dimensions*.

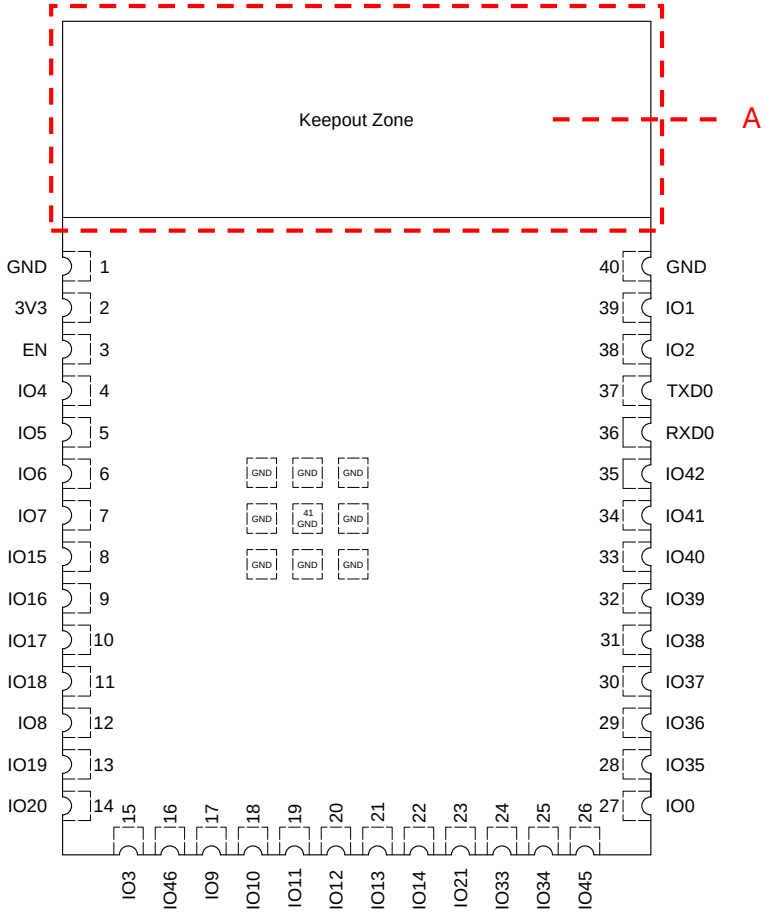

Figure 3-1. Pin Layout (Top View)

Note A:
The zone marked with dotted lines is the antenna keepout zone. The pin diagram is applicable to ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U, but the latter has no antenna keepout zone.
To learn more about the keepout zone for module's antenna on the base board, please refer to *ESP32-S2 Hardware Design Guidelines* > Section *General Principles of PCB Layout for Modules*.

3.2 Pin Description

The module has 41 pins. See pin definitions in Table 3-1 *Pin Definitions*.

For peripheral pin configurations, please refer to *ESP32-S2 Series Datasheet* > Section *Peripheral Pin Configurations*.

Table 3-1. Pin Definitions

Name	No.	Type[1]	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
IO18	11	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO3	15	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO46	16	I	GPIO46
IO9	17	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
IO10	18	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
IO11	19	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
IO12	20	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
IO13	21	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
IO14	22	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
IO21	23	I/O/T	RTC_GPIO21, GPIO21
IO33	24	I/O/T	SPIIO4, GPIO33, FSPIHD
IO34	25	I/O/T	SPIIO5, GPIO34, FSPICS0
IO45	26	I/O/T	GPIO45
IO0	27	I/O/T	RTC_GPIO0, GPIO0
IO35	28	I/O/T	SPIIO6, GPIO35, FSPID
IO36	29	I/O/T	SPIIO7, GPIO36, FSPICLK
IO37	30	I/O/T	SPIDQS, GPIO37, FSPIQ
IO38	31	I/O/T	GPIO38, FSPIWP
IO39	32	I/O/T	MTCK, GPIO39, CLK_OUT3
IO40	33	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	34	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	35	I/O/T	MTMS, GPIO42
RXD0	36	I/O/T	U0RXD, GPIO44, CLK_OUT2
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0

Cont'd on next page

Table 3-1 – cont'd from previous page

Name	No.	Type[1]	Function
GND	40	P	Ground
EPAD	41	P	Ground

[1] P: power supply; I: input; O: output; T: high impedance.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-S2 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 7 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse parameters at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pins: GPIO0 and GPIO46
- **VDD_SPI voltage**
  - Strapping pin: GPIO45
  - eFuse parameters: EFUSE_VDD_SPI_FORCE and EFUSE_VDD_SPI_TIEH
- **ROM message printing**
  - Strapping pin: GPIO46
  - eFuse parameters: EFUSE_UART_PRINT_CONTROL and EFUSE_UART_PRINT_CHANNEL

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP32-S2 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S2 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 4-2 and Figure 4-1.

Table 4-2. Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

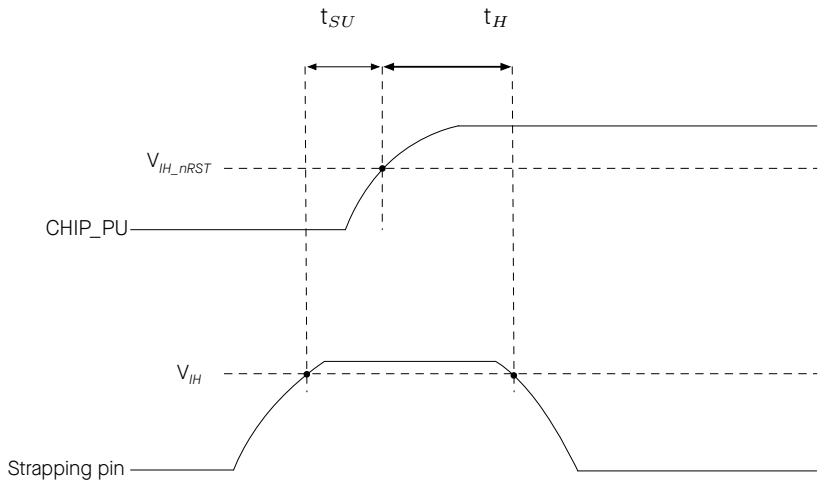

Figure 4-1. Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 4-3 *Chip Boot Mode Control*.

Table 4-3. Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI boot mode	**1**	Any value
Joint download boot mode [2]	0	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB-OTG Download Boot
- UART Download Boot
- SPI Download Boot

4.2 VDD_SPI Voltage Control

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 4-4. VDD_SPI Voltage Control

VDD_SPI power source [2]	Voltage	EFUSE_VDD_SPI_FORCE	GPIO45	EFUSE_VDD_SPI_TIEH
VDD3P3_RTC via R_{SPI}	**3.3 V**	**0**	**0**	Ignored
		1	Ignored	1
Flash Voltage Regulator	1.8 V	0	1	Ignored
		1	Ignored	0

[1] **Bold** marks the default value and configuration.

[2] See *ESP32-S2 Series Datasheet* > Section *Power Scheme*.

4.3 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0**
- UART1

EFUSE_UART_PRINT_CONTROL and GPIO46 control ROM messages printing to **UART** as shown in Table 4-5 *UART ROM Message Printing Control*.

EFUSE_UART_PRINT_CHANNEL controls if the ROM messages will be printed to UART0 or UART1.

- 0: UART0
- 1: UART1

Table 4-5. UART ROM Message Printing Control

UART ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO46
Enabled	**0**	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

[1] **Bold** marks the default value and configuration.

4.4 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails need a short time to stabilize. After that, CHIP_PU – the pin used for power-up and reset – is pulled high to activate the chip. For information on CHIP_PU as well as power-up and reset timing, see Figure 4-2 and Table 4-6.

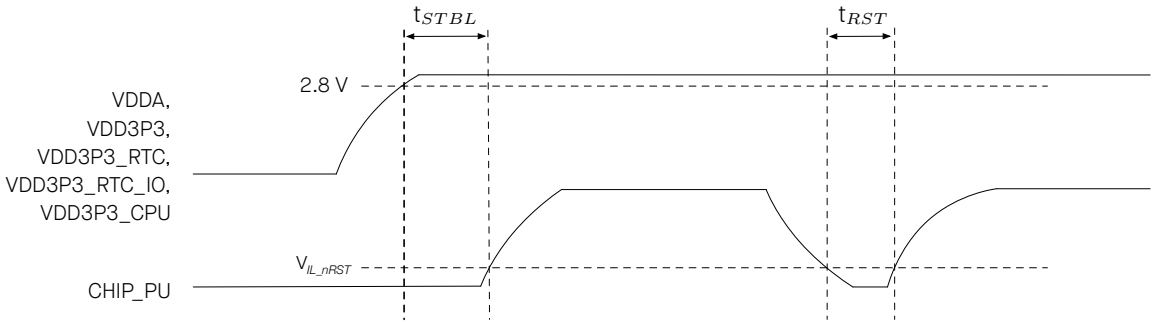

Figure 4-2. Visualization of Timing Parameters for Power-up and Reset

Table 4-6. Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_RTC_IO, and VDD3P3_CPU to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip (see Table 5-3)	50

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 5-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 5-2 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	105	°C

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	Power supply voltage		3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply		0.5	—	—	A
T_A	Operating ambient temperature	85 °C version	−40	—	85	°C
		105 °C version			105	

5.3 DC Characteristics (3.3 V, 25 °C)

Table 5-3. DC Characteristics (3.3 V, 25 °C)

Parameter	Description	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD [1]	—	VDD [1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD [1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH} [2]	High-level output voltage	0.8 × VDD [1]	—	—	V
V_{OL} [2]	Low-level output voltage	—	—	0.1 × VDD [1]	V
I_{OH}	High-level source current (VDD [1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD [1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_PU voltage is within the specified range)	0.75 × VDD [1]	—	VDD [1] + 0.3	V

V_{IL_nRST}	Chip reset voltage (CHIP_PU voltage is within the specified range)	−0.3	—	0.25 × VDD [1]	V

[1] VDD – voltage from a power pin of a respective power domain.
[2] V_{OH} and V_{OL} are measured using high-impedance load.

5.4 Current Consumption Characteristics

Owing to the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *RTC and Low-Power Management* in *ESP32-S2 Series Datasheet*.

5.4.1 Current Consumption in Active Mode

Table 5-4. RF Current Consumption in Active Mode

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	320
		802.11g, 20 MHz, 54 Mbps, @17.5 dBm	273
		802.11n, 20 MHz, MCS7, @16.5 dBm	265
		802.11n, 40 MHz, MCS7, @16.5 dBm	274
	RX	802.11b/g/n, 20 MHz	77
		802.11n, 40 MHz	81

[1] The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on 100% duty cycle.
[2] The current consumption figures in RX mode are for cases where the peripherals are disabled and the CPU idle.

Note:
The content below is excerpted from Section *Power Consumption in Other Modes* in *ESP32-S2 Series Datasheet*.

5.4.2 Current Consumption in Other Modes

The measurements below are applicable to ESP32-S2, ESP32-S2FH2, and ESP32-S2FH4. Since ESP32-S2FN4R2 and ESP32-S2R2 come with in-package PSRAM, their current consumption might be higher.

Table 5-5. Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ	
			All Peripherals Clocks Disabled (mA)	All Peripherals Clocks Enabled (mA)[1]
Modem-sleep[2,3]	240	CPU is idle	20.0	28.0
		CPU is running	23.0	32.0
	160	CPU is idle	14.0	21.0
		CPU is running	16.0	24.0
	80	CPU is idle	10.5	18.4
		CPU is running	12.0	20.0

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 5-6. Current Consumption in Low-Power Modes

Work mode	Description		Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance		750
Deep-sleep	The ULP co-processor is powered on[2]	ULP-FSM	170
		ULP-RISC-V	190
	ULP sensor-monitored pattern[3]		22
	RTC timer + RTC memory		25
	RTC timer only		20
Power off	CHIP_PU is set to low level, the chip is powered off		1

[1] In Light-sleep mode, with all related SPI pins pulled up, the current consumption of the embedded PSRAM is 140 μA. Chip variants with in-package PSRAM include ESP32-S2FN4R2 and ESP32-S2R2.

[2] During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I2C are able to operate.

[3] The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 22 μA.

5.5 Memory Specifications

The data below is sourced from the memory vendor datasheet. These values are guaranteed through design and/or characterization but are not fully tested in production. Devices are shipped with the memory erased.

Table 5-7. Flash Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.65	1.80	2.00	V

Cont'd on next page

Table 5-7 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz
—	Program/erase cycles	100,000	—	—	cycles
T_{RET}	Data retention time	20	—	—	years
T_{PP}	Page program time	—	0.8	5	ms
T_{SE}	Sector erase time (4 KB)	—	70	500	ms
T_{BE1}	Block erase time (32 KB)	—	0.2	2	s
T_{BE2}	Block erase time (64 KB)	—	0.3	3	s
T_{CE}	Chip erase time (16 Mb)	—	7	20	s
	Chip erase time (32 Mb)	—	20	60	s
	Chip erase time (64 Mb)	—	25	100	s
	Chip erase time (128 Mb)	—	60	200	s
	Chip erase time (256 Mb)	—	70	300	s

Table 5-8. PSRAM Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.62	1.80	1.98	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz

6 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

6.1 Wi-Fi Radio

6.1.1 Wi-Fi RF Standards

Table 6-1. Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel [1]		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	802.11b: 1, 2, 5.5 and 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	802.11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna, external antenna connector

[1] Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software. See ESP RF Test Tool and Test Guide for instructions.

[2] For the modules that use external antenna connectors, the output impedance is 50 Ω. For other modules without external antenna connectors, the output impedance is irrelevant.

6.1.2 Wi-Fi RF Transmitter (TX) Specifications

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 6-2.

Table 6-2. TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	19.5	—
802.11b, 11 Mbps	—	19.5	—
802.11g, 6 Mbps	—	17.5	—

Cont'd on next page

Table 6-2 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11g, 54 Mbps	—	17.5	—
802.11n, HT20, MCS0	—	17.5	—
802.11n, HT20, MCS7	—	16.5	—
802.11n, HT40, MCS0	—	17.5	—
802.11n, HT40, MCS7	—	16.5	—

Table 6-3. TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @19.5 dBm	—	-25.0	-10
802.11b, 11 Mbps, @19.5 dBm	—	-25.0	-10
802.11g, 6 Mbps, @17.5 dBm	—	-25.0	-5
802.11g, 54 Mbps, @17.5 dBm	—	-28.0	-25
802.11n, HT20, MCS0, @17.5 dBm	—	-27.0	-5
802.11n, HT20, MCS7, @16.5 dBm	—	-30.5	-27
802.11n, HT40, MCS0, @17.5 dBm	—	-27.0	-5
802.11n, HT40, MCS7, @16.5 dBm	—	-30.0	-27

[1] SL stands for standard limit value.

6.1.3 Wi-Fi RF Receiver (RX) Specifications

Table 6-4. RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	-97.0	—
802.11b, 2 Mbps	—	-94.5	—
802.11b, 5.5 Mbps	—	-92.0	—
802.11b, 11 Mbps	—	-88.5	—
802.11g, 6 Mbps	—	-92.5	—
802.11g, 9 Mbps	—	-91.0	—
802.11g, 12 Mbps	—	-89.5	—
802.11g, 18 Mbps	—	-87.5	—
802.11g, 24 Mbps	—	-84.5	—
802.11g, 36 Mbps	—	-80.5	—
802.11g, 48 Mbps	—	-76.5	—
802.11g, 54 Mbps	—	-75.0	—
802.11n, HT20, MCS0	—	-92.0	—
802.11n, HT20, MCS1	—	-89.0	—
802.11n, HT20, MCS2	—	-86.5	—

Cont'd on next page

Table 6-4 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT20, MCS3	—	–83.5	—
802.11n, HT20, MCS4	—	–79.5	—
802.11n, HT20, MCS5	—	–75.5	—
802.11n, HT20, MCS6	—	–74.0	—
802.11n, HT20, MCS7	—	–72.5	—
802.11n, HT40, MCS0	—	–89.0	—
802.11n, HT40, MCS1	—	–86.5	—
802.11n, HT40, MCS2	—	–84.0	—
802.11n, HT40, MCS3	—	–80.0	—
802.11n, HT40, MCS4	—	–76.5	—
802.11n, HT40, MCS5	—	–72.5	—
802.11n, HT40, MCS6	—	–71.0	—
802.11n, HT40, MCS7	—	–69.5	—

Table 6-5. Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 6-6. RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	14	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	13	—
802.11n, HT40, MCS0	—	19	—
802.11n, HT40, MCS7	—	8	—

7 Module Schematics

This is the reference design of the module.

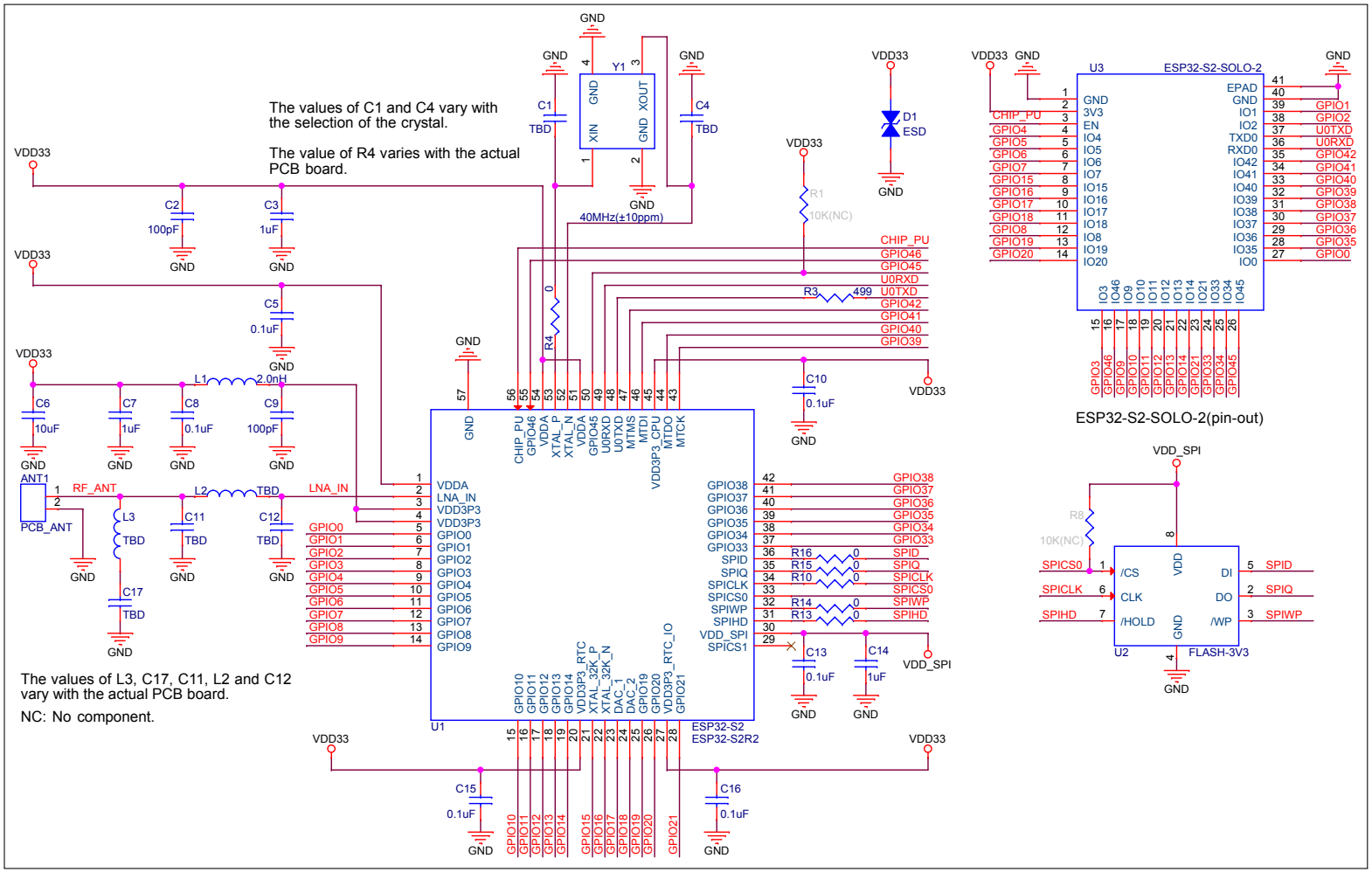

Figure 7-1. ESP32-S2-SOLO-2 Schematics

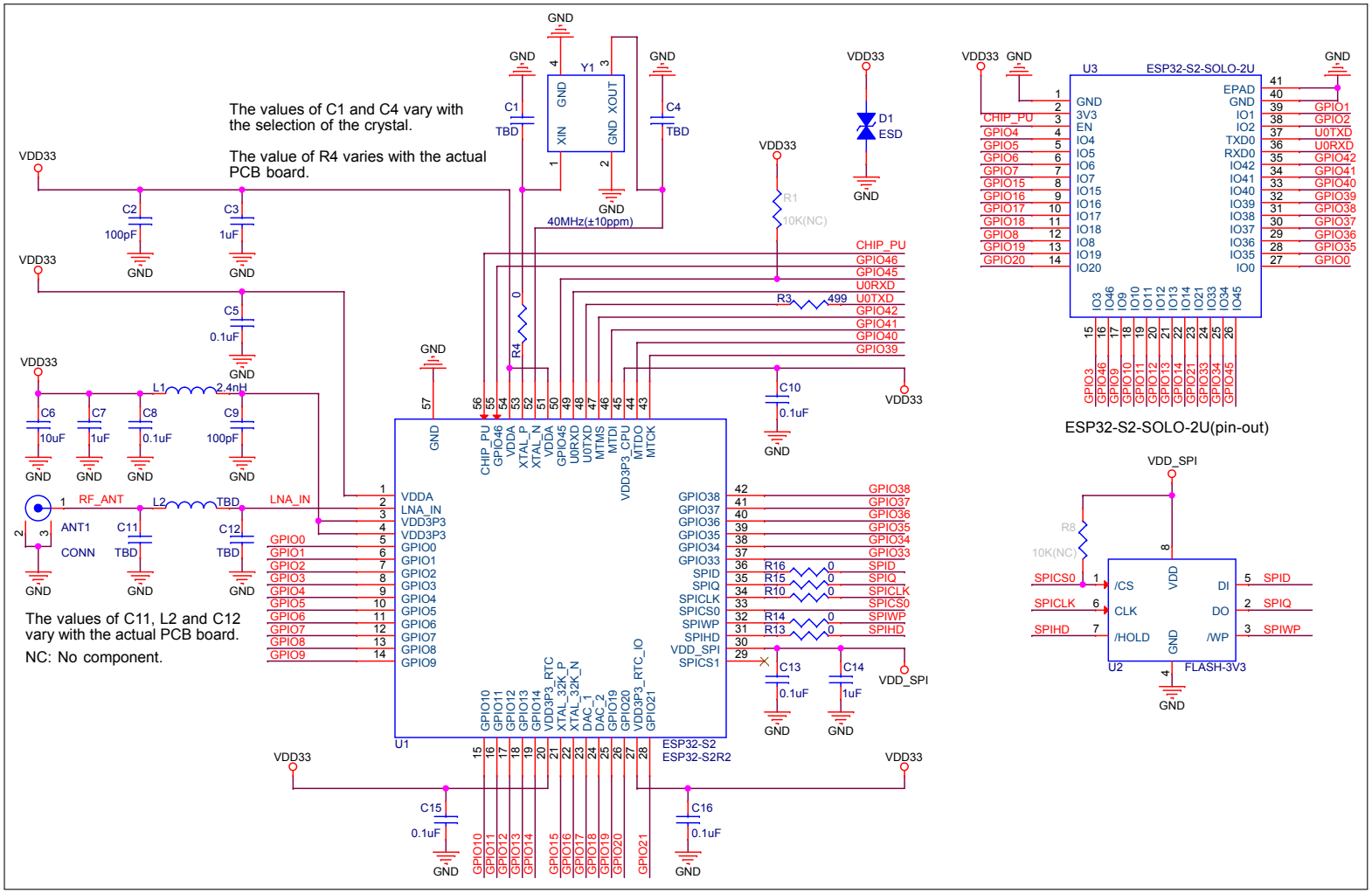

Figure 7-2. ESP32-S2-SOLO-2U Schematics

8 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

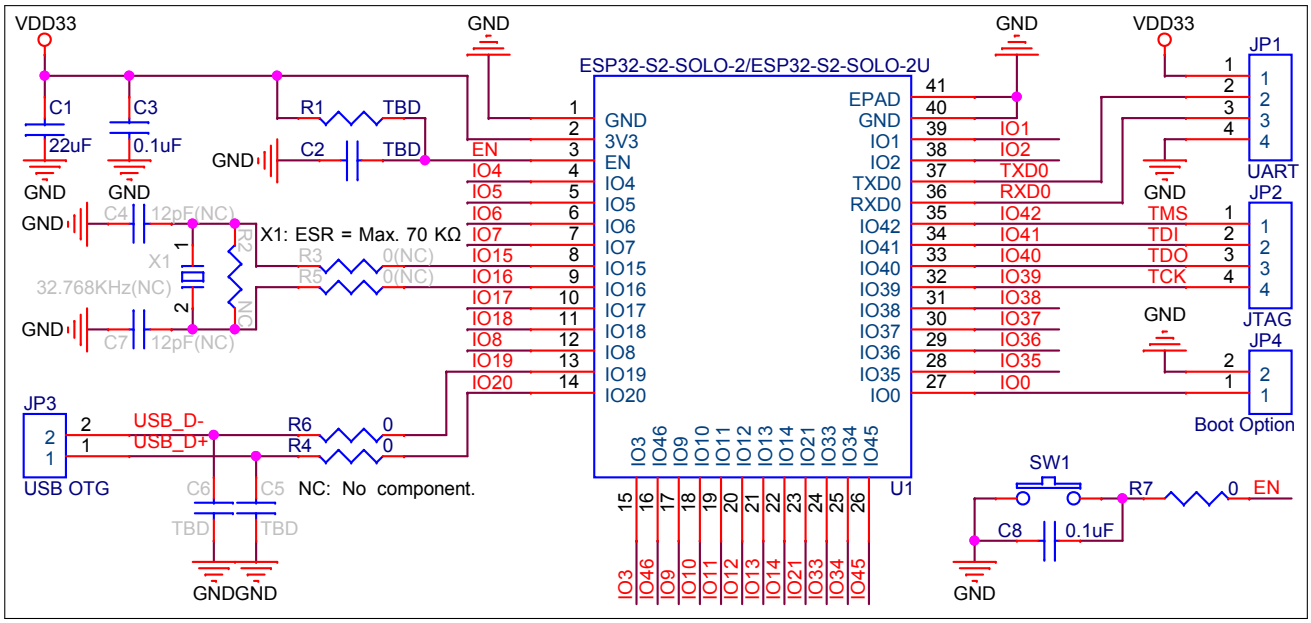

Figure 8-1. Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S2 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to *ESP32-S2 Series Datasheet* > Section *Power Scheme*.

9 Physical Dimensions

9.1 Module Dimensions

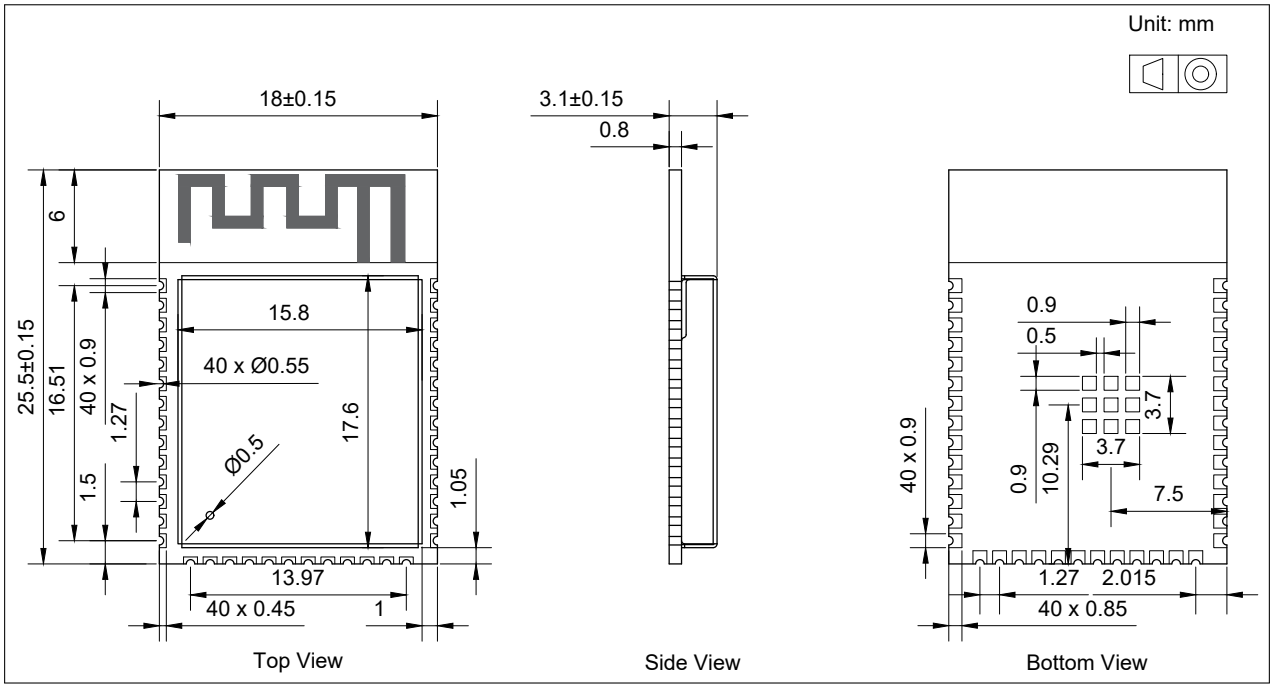

Figure 9-1. ESP32-S2-SOLO-2 Physical Dimensions

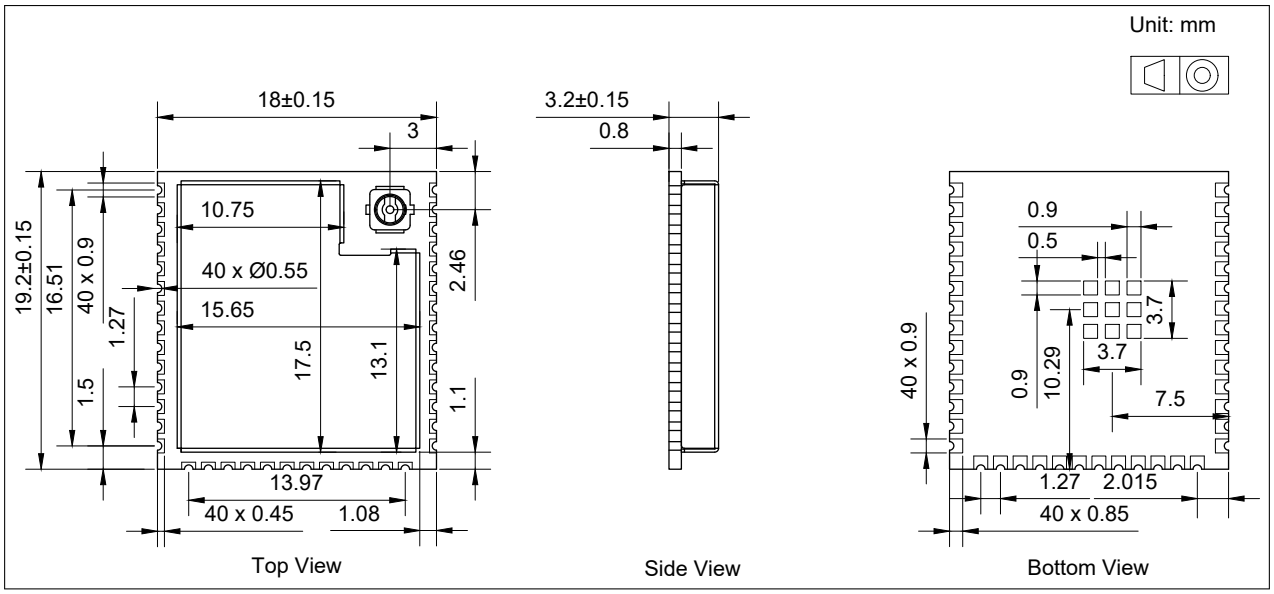

Figure 9-2. ESP32-S2-SOLO-2U Physical Dimensions

Note:
For information about tape, reel, and product marking, please refer to *ESP32-S2 Module Packaging Information*.

9.2 Dimensions of External Antenna Connector

ESP32-S2-SOLO-2U uses the first generation external antenna connector as shown in Figure 9-3 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

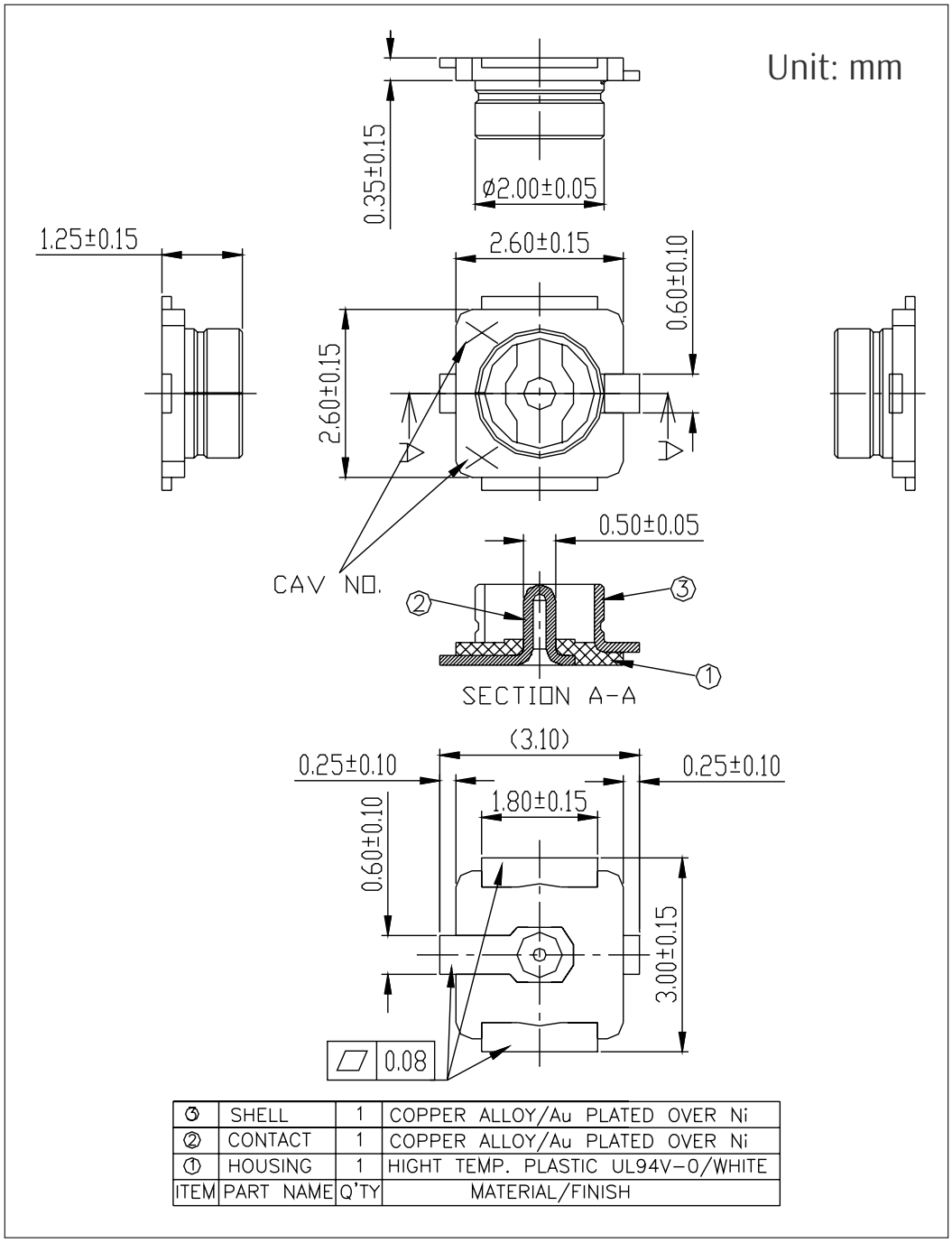

Figure 9-3. Dimensions of External Antenna Connector

The external antenna used for ESP32-S2-SOLO-2U during certification testing is the first generation monopole

antenna, with material code TFPD05H08750011.

The module does not include an external antenna upon shipment. If needed, select a suitable external antenna based on the product's usage environment and performance requirements.

It is recommended to select an antenna that meets the following requirements:

- 2.4 GHz band
- 50 Ω impedance
- The maximum gain does not exceed 2.33 dBi, the gain of the antenna used for certification
- The connector matches the specifications shown in Figure 9-3 *Dimensions of External Antenna Connector*

Note:
If you use an external antenna of a different type or gain, additional testing, such as EMC, may be required beyond the existing antenna test reports for Espressif modules. Specific requirements depend on the certification type.

10 PCB Layout Recommendations

10.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 10-1 *ESP32-S2-SOLO-2 Recommended PCB Land Pattern* and Figure 10-2 *ESP32-S2-SOLO-2U Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 10-1 and Figure 10-2. You can view the source files for ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U with Autodesk Viewer.
- 3D models of ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

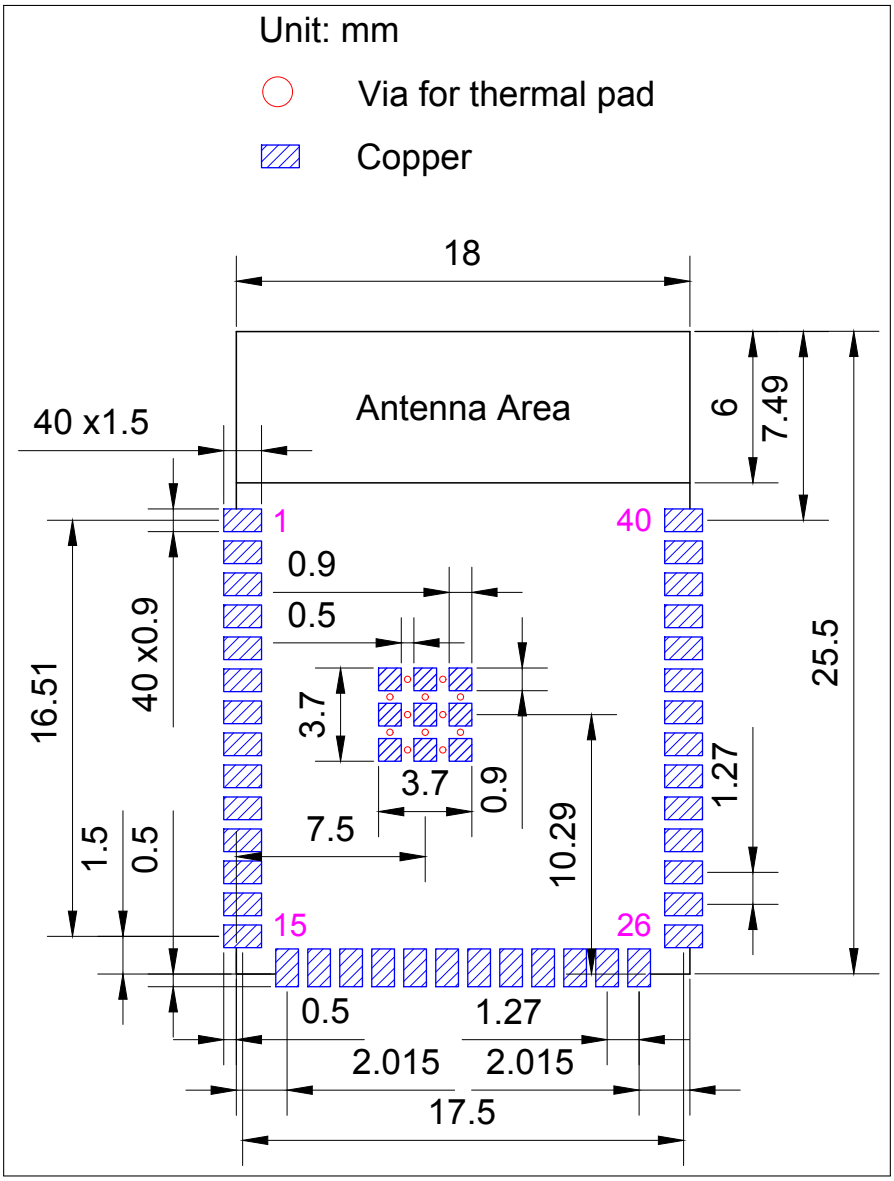

Figure 10-1. ESP32-S2-SOLO-2 Recommended PCB Land Pattern

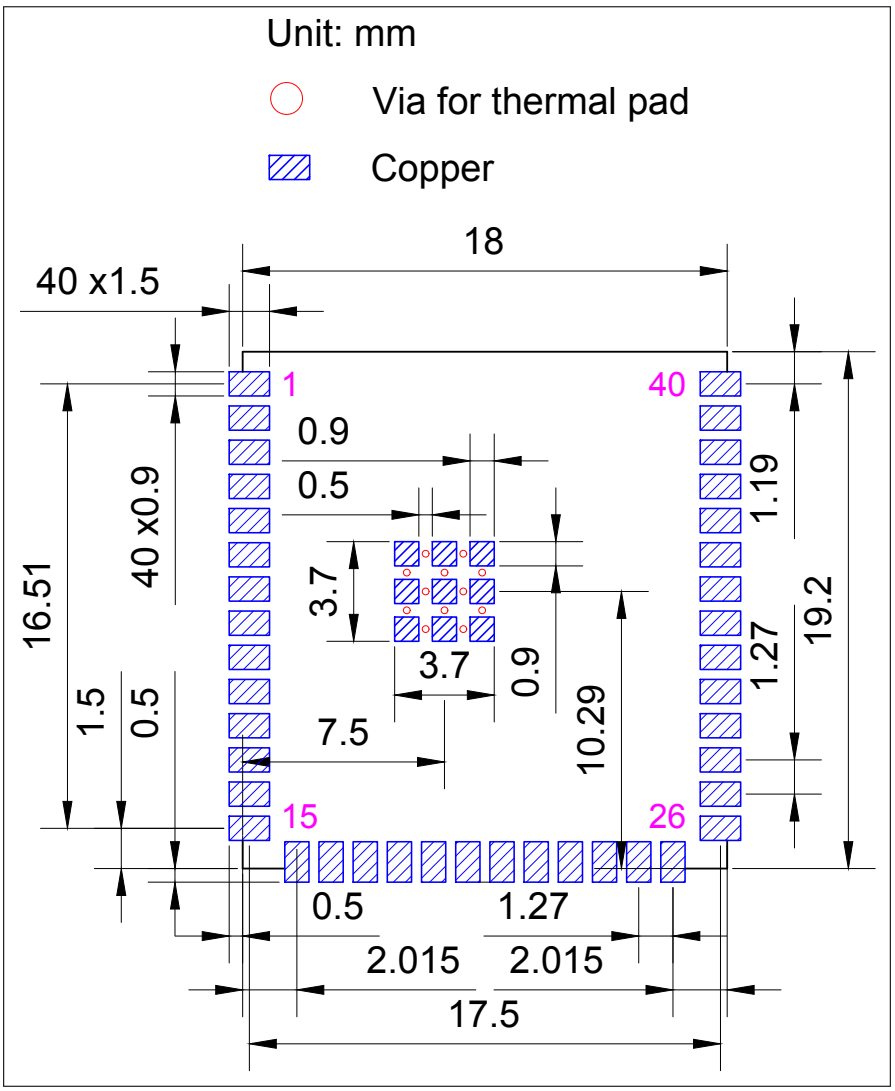

Figure 10-2. ESP32-S2-SOLO-2U Recommended PCB Land Pattern

10.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-S2 Hardware Design Guidelines* > Section *General Principles of PCB Layout for Modules*.

11 Product Handling

11.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

11.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

11.3 Soldering Profiles

11.3.1 Reflow Profile

Solder the module in a single reflow.

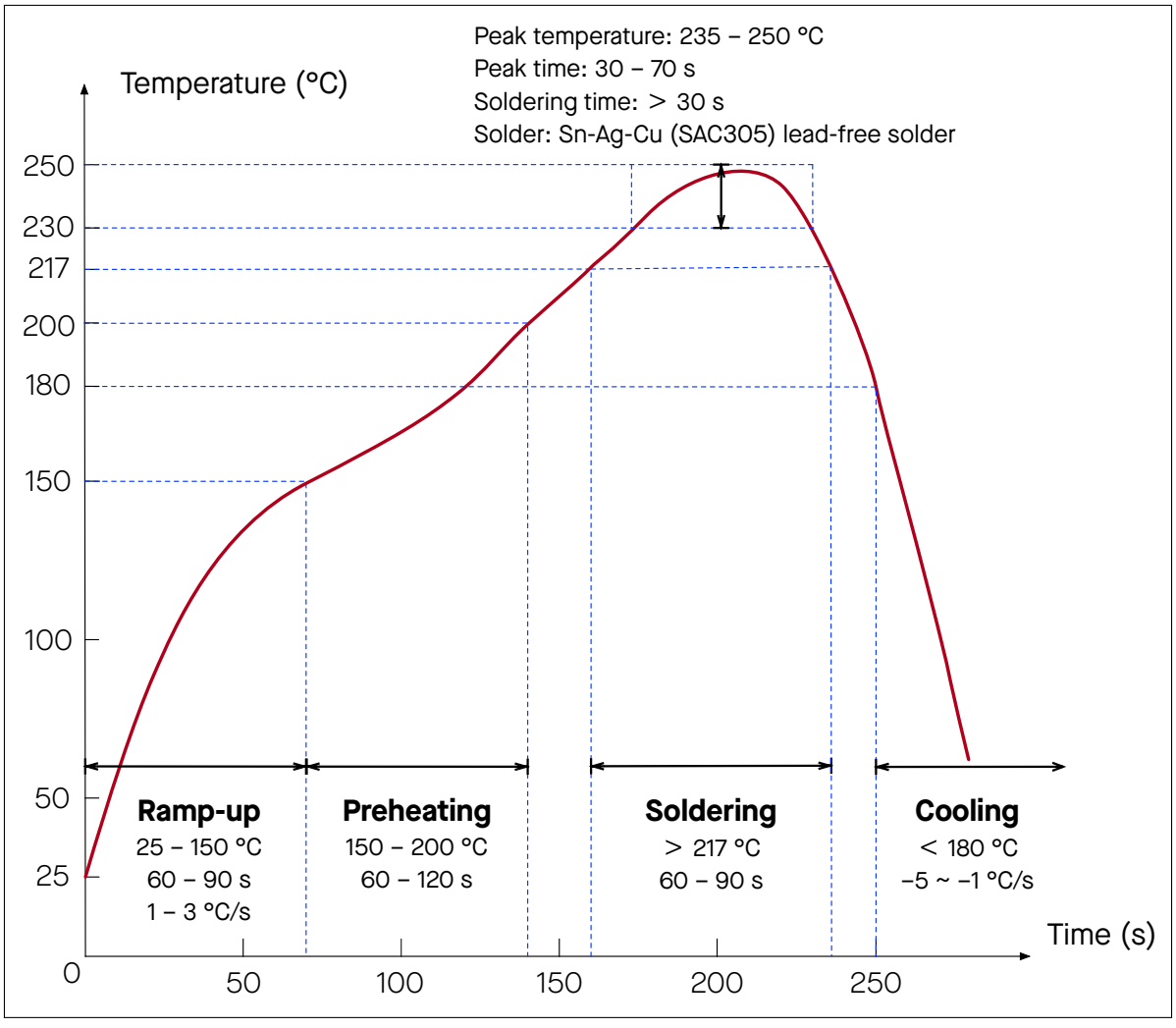

Figure 11-1. Reflow Profile

11.3.2 Wave Profile

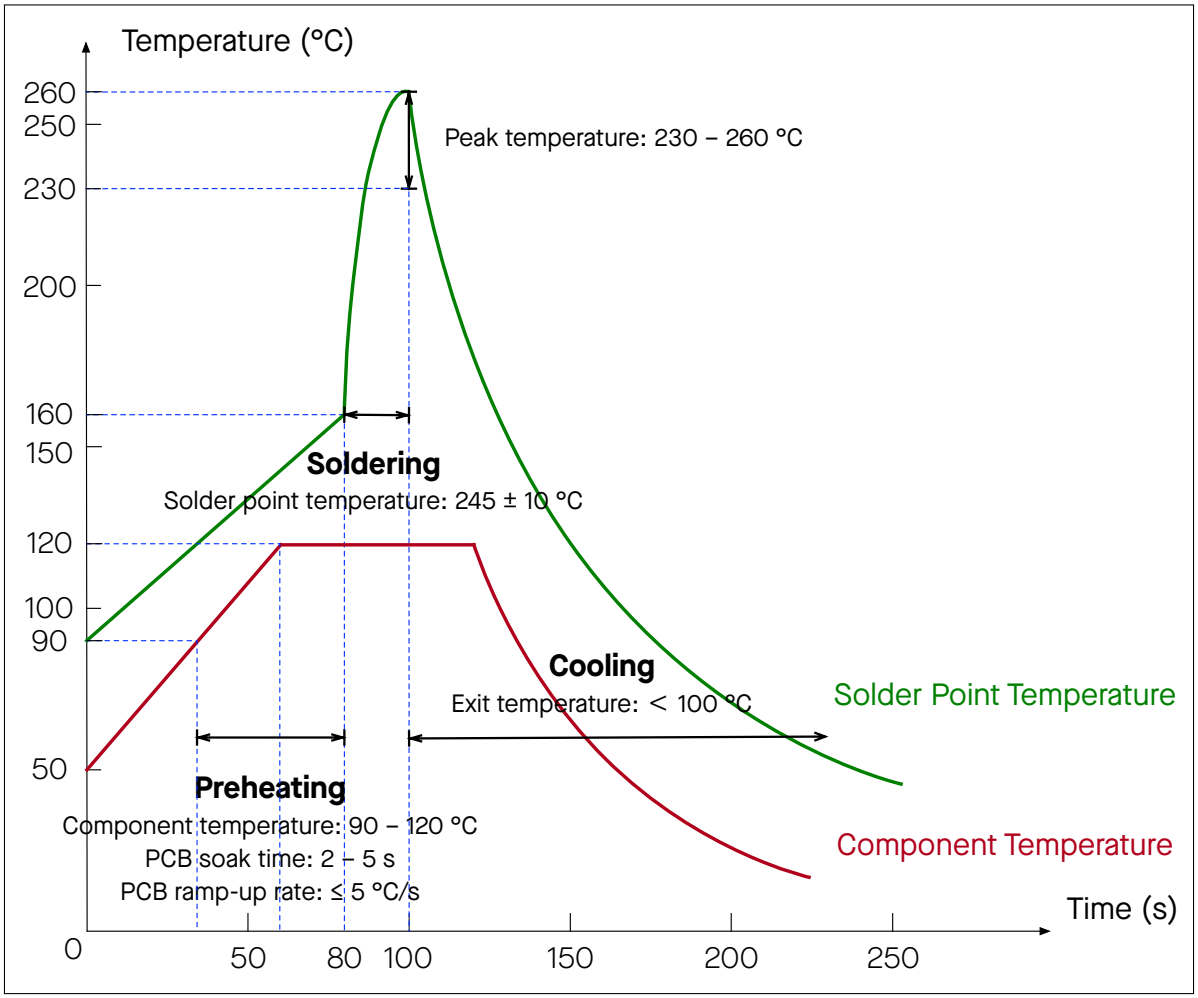

Figure 11-2. Wave Soldering Profile

11.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Datasheet Versioning

Datasheet Version	Status	Watermark	Definition
v0.1 ~ v0.5 (excluding v0.5)	Draft	Confidential	This datasheet is under development for products in the design stage. Specifications may change without prior notice.
v0.5 ~ v1.0 (excluding v1.0)	Preliminary release	Preliminary	This datasheet is actively updated for products in the verification stage. Specifications may change before mass production, and the changes will be documentation in the datasheet's Revision History.
v1.0 and higher	Official release	—	This datasheet is publicly released for products in mass production. Specifications are finalized, and major changes will be communicated via Product Change Notifications (PCN).
Any version	—	Not Recommended for New Design (NRND)[1]	This datasheet is updated less frequently for products not recommended for new designs.
Any version	—	End of Life (EOL)[2]	This datasheet is no longer mtained for products that have reached end of life.

[1] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet are not recommended for new designs.

[2] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet have reached end of life.

Related Documentation and Resources

Related Documentation

- ESP32-S2 Series Datasheet – Specifications of the ESP32-S2 hardware.
- *ESP32-S2 Technical Reference Manual* – Detailed information on how to use the ESP32-S2 memory and peripherals.
- *ESP32-S2 Hardware Design Guidelines* – Guidelines on how to integrate the ESP32-S2 into your hardware product.
- *ESP32-S2 Series SoC Errata* – Descriptions of known errors in ESP32-S2 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S2
- *ESP32-S2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *ESP-FAQ* – A summary document of frequently asked questions released by Espressif.
  https://espressif.com/projects/esp-faq/en/latest/index.html
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S2 Series SoCs* – Browse through all ESP32-S2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S2
- *ESP32-S2 Series Modules* – Browse through all ESP32-S2-based modules.
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Revision History

Date	Version	Release notes
2025-11-24	v1.3	• Added Section 4.4 *Chip Power-up and Reset* • Added Section 5.5 *Memory Specifications* • Added Section 11.4 *Datasheet Versioning* • Upgraded document template
2025-11-07	v1.2	• In Chapter *Series Comparison*: – Added Figure 1-1 *ESP32-S2 Module Variant Nomenclature* – Removed ESP32-S2-SOLO-2-N8R2, ESP32-S2-SOLO-2-N16R2, ESP32-S2-SOLO-2U-N8,ESP32-S2-SOLO-2U-N8R2 and ESP32-S2-SOLO-2U-N16R2 – Marked ESP32-S2-SOLO-2-N8 and ESP32-S2-SOLO-2-H4 end of life • In Section 9.2 *Dimensions of External Antenna Connector*: Added the external antenna information for certification • In Chapter 10.1 *PCB Land Pattern*: added 3D models
2024-09-05	v1.1	Formatting updates
2024-05-10	v1.0	• Added information about certification and test in Section 1.1 *Features*
2024-04-16	v0.6	• Updated EPAD descriptions in Section 8 *Peripheral Schematics* • Added descriptions in Section 10.1 *PCB Land Pattern* • Other formatting updates
2022-09-19	v0.5	Preliminary release

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