Product Change Notification: ALAN-16SLVL366

Date:

11-Feb-2025

Product Category:

8-Bit Microcontrollers, Analog to Digital Converters, CAN Controller, CAN I/O Expander, Digital Potentiometers, Interface- Infrared Products, Interface- Passive-Keyless-Entry Analog Front End, Linear Comparators, Linear Op Amps, Linear Programmable Gain Amplifiers, Linear Regulators, Power Management - System Supervisors/Voltage Detectors, Switching Regulators, Touch Controllers, Voltage References

Notification Subject:

CCB 7364 Initial Notice: Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for multiple device families available in various packages.

Affected CPNs:

ALAN-16SLVL366_Affected_CPN_02112025.pdf
ALAN-16SLVL366_Affected_CPN_02112025.csv

PCN Status: Initial Notification

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change: Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for multiple device families available in various packages.

Pre and Post Summary Changes:

	Pre Change	Post Change
Fabrication Site*	Microchip Technology Tempe – Fab 2 (TMGR)	Microchip Technology Gresham – Fab 4 (GRTM)

Wafer Size	8"	8"

Impacts to Datasheet: None

Change Impact: None

Reason for Change: To improve manufacturability and on time delivery performance by qualifying a new fabrication location (GRTM - FAB 4), which is a Microchip-owned facility that offers significant expansion potential to better meet future client demand. *Note: The attached file called Tempe_Fab2_IATF_Decertification is for the manufacturing site deactivation of Microchip Technology Tempe – Fab 2 (TMGR), contact your local Microchip sales office for inquiries.

Change Implementation Status: In Progress

Estimated Qualification Completion Date: July 2025

Note: Please be advised the qualification completion times may be extended because of unforeseen business conditions however implementation will not occur until after qualification has completed and a final PCN has been issued. The final PCN will include the qualification report and estimated first ship date. Also note that after the estimated first ship date guided in the final PCN customers may receive pre and post change parts.

Timetable Summary:

	February 2025					>	July 2025				
Work Week	05	06	07	08	09		27	28	29	30	31
Initial PCN Issue Date			X								
Qual Report Availability										X	
Final PCN Issue Date										X	

Method to Identify Change: Traceability Code

Qualification Plan: Please open the attachments included with this PCN labeled as PCN_#_Qual_Plan.

Revision History: February 11, 2025: Issued initial notification.

Note: The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable product.

Attachments:

Tempe_Fab2_IATF_Decertification.pdf
PCN_ALAN-16SLVL366__Qual_Plan.pdf

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our **PCN home page** select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the **PCN FAQ** section.

If you wish to change your PCN profile, including opt out, please go to the **PCN home page** select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

QUALIFICATION PLAN SUMMARY

PCN# ALAN-16SLVL366

Date:
January 13, 2025

Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for multiple device families available in various packages.

Purpose: Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for multiple device families available in various packages. This is Q006 grade 1 qualification.

CCB No.: 7364

Misc.	Assembly site	MMT
	BD Number	A-056966 Rev A
	MP Code (MPC)	A7AV17S2XA20
	Part Number (CPN)	PIC16C74B/PIC16LC74B
	Assembly Shipping Media	Tube
	Base Quantity Multiple (BQM)	10
	Reliability Site	MMT
Lead-Frame	Paddle size	200x200 mils
	Material	CDA194
	DAP Surface Prep	Ag
	Treatment	Ag Spot Plated
	Process	Stamped
	Lead-lock	Yes
	Part Number	10104001
	Lead Plating	Matte Sn
Bond Wire	Material	CuPdAu
Die Attach	Part Number	CRM-1064L
	Conductive	Yes
MC	Part Number	GE800
PKG	Package Type	PDIP
	Pin/Ball Count	40L
	PKG width/size	.600in

Test Name	Conditions	Reliability Stress Read Point **Grade 1: -40°C to +125°C (MCHP E Temp)**	Pre & Post Reliability Stress Test Temperature **Grade 1: -40°C to +125°C (MCHP E Temp)**	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	J-STD-002D ; Perform 8 hours of steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.			22	5	1	27	>95% lead coverage	5	Standard Pb-free solderability is the requirement.
Wire Bond Pull - WBP	Mil. Std. 883-2011			5	0	1	5	0 fails after TC	5	30 bonds from a min. 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001			5	0	1	5	0	5	30 bonds from a min. 5 devices.
Physical Dimensions	Measure per JESD22 B100 and B108			10	0	3	30	0	5	
Lead Integrity (For through-hole device only)	JESD22 B105			5	0	1	5	0	5	10 leads from each of 5 parts. Not required for SMD, only required for through-hole.
External Visual	Mil. Std. 883-2009/2010			All devices prior to submission for qualification testing	0	3	ALL	0	5	
HTSL (High Temp Storage Life)	JESD22-A103 +125°C, +150°C or +175°C *2x Stress*	<u>1st Readpoint:</u> Grade 1: 500 hrs (+175°C) or 1000 hrs (150°C) <u>2nd Readpoint:</u> Grade 1: 1000 hrs (+175°C) or 2000 hrs (150°C)	Grade 1: +25°C, +85°C, +125°C	45	5	3	150	0	21 - 167	Perform per the requirements in AEC-Q100/Q101. Spares should be properly identified.
HAST	JESD22-A101 or A110 +130°C/85% RH for 96 hrs or +110°C/85%RH for 264 hrs *2x Stress*	<u>1st Readpoint:</u> Grade 1: 96 hrs (+130°C/85% RH) or 264 hrs (+110°C/85%RH) <u>2nd Readpoint:</u> Grade 1: 192 hrs (+130°C/85% RH) or 528 hrs (+110°C/85%RH)	Grade 1: +25°C, +85°C, +125°C	77	5	3	246	0	10 - 22	Perform per the requirements in AEC-Q006. Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
uHAST	JESD22-A102, A118, or A101 +130°C/85% RH for 96 hrs or +110°C/85% RH for 264 hrs	Grade 1: 96 hrs (+130°C/85% RH) or 264 hrs (+110°C/85% RH)	Grade 1: +25°C	77	5	3	246	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Temp Cycle	JESD22-A104 and Appendix 3 -55ºC to +125ºC, -55ºC to +150ºC *2x Stress*	<u>1st Readpoint:</u> Grade 1: 1000 cycles (-55ºC to +150ºC) <u>2nd Readpoint:</u> Grade 1: 2000 cycles (-55ºC to +150ºC)	Grade 1: +25°C,+85°C, +125°C	77	5	3	246	0	15 - 120	Perform per the requirements in AEC-Q006. Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Wire Bond Integrity (AEC-Q006 Requirements)	AEC-Q006							See Special Instructions		Wire pull / ball shear is performed after stress testing and decapsulation.
Cross Sectioning (AEC-Q006 Requirements)	IPC-TM-650, Methods 2.1.1 and 2.1.1.2 Criteria of examination: <u>• Ball bond area</u> o Amount and distribution of intermetallic - an alternative planar analysis method to evaluate ball bond IMC formation is also acceptable. o Crack initiation/propagation o Corrosion after 1x stress <u>• Wedge bond area</u> o Amount of contact o Wire angle to wedge o Crack initiation/propagation o Corrosion after 1x stress o Intermetallics formed in the bond area			1	0	3	3	1/0/00	5	

Purpose: Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for multiple device families available in various packages.

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Test	Number of Lot/s	Sample Size (per lot)	Total Samples	Conditions
ELFR	3	800	2400	48 hours @ 125°C
DLT	3	77	231	1000 Hours @ 125°C
Retention Bake	3	231	693	1008 hours @ 150°C
ESD (HBM)	2	12	24	3 each @ ±250V, ±500V, ±1KV & ±2KV
ESD (CDM)	2	9	18	3 each @ ±250V, ±500V, ±750V
Latch Up	2	12	24	3 room, 3 125°C AECQ100-004
				3 room, 3 125°C MILSTD 883
Electrical Distribution	3	30	90	Data log parameters at room, hot, and cold temperatures at Vcc min/max and Frequency min/max.

Date: January 30, 2025
RE: Tempe (Fab 2) Wafer Fabrication Facility ISO/IATF Decertification
IATF Certificate: 08435-2002-AQ-HOU-IATF-33RSTM

On December 2, 2024, Microchip announced manufacturing restructuring plans that include the closure of the Tempe (Fab 2) Wafer Fabrication Facility.

This memo is to further announce that as part of the facility closure, its active IATF-16949 certificate will be withdrawn, in early Q3, 2025. Additionally, the facility will be removed from Microchip's Corporate ISO-9001 certificate by the end of 2025.

Microchip is committed to ensuring product quality during the entire time that Fab 2 remains operational. All established and certified process control measures remain in place and adherence to these practices will continue for the life of the fab, regardless of the status of IATF-16949 certification. Additionally, all Microchip devices are 100% electrically tested, with only known good products shipped to customers.

Please contact your local **Microchip Sales Office** with questions or concerns regarding this notification.

Regards,
Microchip Corporate Quality Systems

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