

Hex Inverter with Schmitt Trigger Input

74AC14, 74ACT14

General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

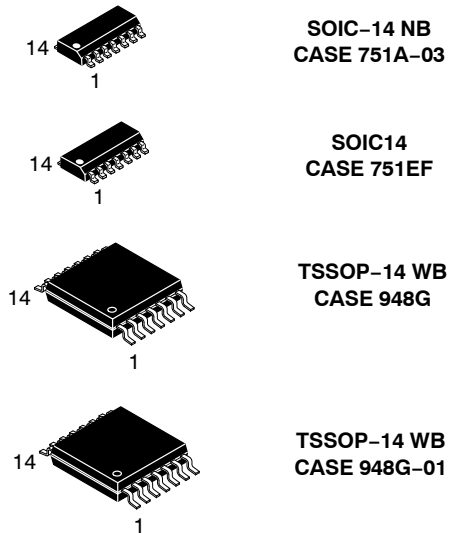
Features

- I_{CC} Reduced by 50%
- Outputs Source/Sink 24 mA
- 74ACT14 has TTL-Compatible Inputs
- These are Pb-Free Devices

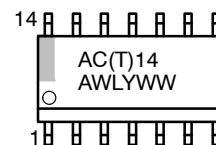
ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------------|---------------------------|-------------|
| Supply Voltage | V_{CC} | -0.5 to +7.0 | V |
| DC Input Diode Current $V_I = -0.5$ V $V_I = V_{CC} + 1.5$ V | I_{IK} | -20 +20 | mA |
| DC Input Voltage | V_I | -0.5 to $V_{CC} + 1.5$ | V |
| DC Output Diode Current $V_O = -0.5$ V $V_O = V_{CC} + 0.5$ V | I_{OK} | -20 +20 | mA |
| DC Output Voltage | V_O | -0.5 to $V_{CC} + 0.5$ | V |
| DC Output Source or Sink Current | I_O | ± 50 | mA |
| DC V_{CC} or Ground Current per Output Pin | I_{CC} or I_{GND} | ± 50 | mA |
| Storage Temperature | T_{STG} | -65 to +150 | $^{\circ}C$ |
| Junction Temperature | T_J | 140 | $^{\circ}C$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

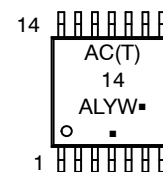


MARKING DIAGRAM



AC14, ACT14 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

MARKING DIAGRAM



AC14, ACT14 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

74AC14, 74ACT14

ORDERING INFORMATION

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74AC14SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74AC14MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide |
| 74ACT14SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74ACT14MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide |

NOTE: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

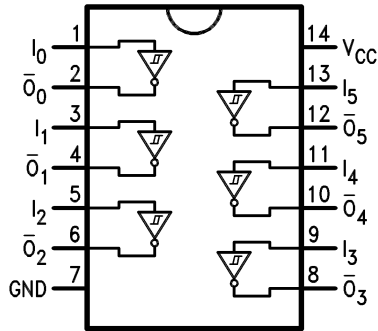


Figure 1. Connection Diagram

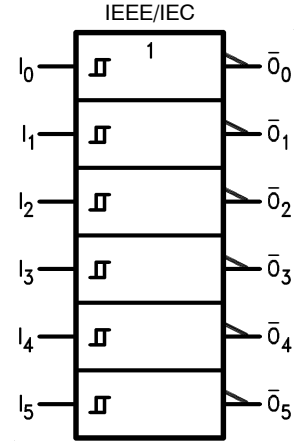


Figure 2. Logic Symbol

PIN DESCRIPTION

| Pin | Description |
|-------------|-------------|
| A_n | Inputs |
| \bar{O}_n | Outputs |

FUNCTION TABLE

| Input | Output |
|-------|-----------|
| A | \bar{O} |
| L | H |
| H | L |

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|----------|-----------------------------|------------|------------|------|
| V_{CC} | Supply Voltage AC ACT | 2.0 4.5 | 6.0 5.5 | V |
| V_I | Input Voltage | 0 | V_{CC} | V |
| V_O | Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature | -40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

74AC14, 74ACT14

DC ELECTRICAL CHARACTERISTICS FOR AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Unit |
|-----------------------------|-----------------------------------|---------------------|--|------------------------|-------------------|---------------------------------|----|------|
| | | | | Typ | Guaranteed Limits | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50 μA | 2.99 | 2.9 | 2.9 | V | |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 3.0 | I _{OH} = 12 mA | - | 2.56 | 2.46 | | |
| | | 4.5 | I _{OH} = 24 mA | - | 3.86 | 3.76 | | |
| | | 5.5 | I _{OH} = 24 mA (Note 1) | - | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50 μA | 0.002 | 0.1 | 0.1 | V | |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 3.0 | I _{OL} = 12 mA | - | 0.36 | 0.44 | | |
| | | 4.5 | I _{OL} = 24 mA | - | 0.36 | 0.44 | | |
| | | 5.5 | I _{OL} = 24 mA (Note 1) | - | 0.36 | 0.44 | | |
| I _{IN} (Note 3) | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | - | ±0.1 | ±1.0 | μA | |
| V _{t+} | Maximum Positive Threshold | 3.0 | T _A = Worst Case | - | 2.2 | 2.2 | V | |
| | | 4.5 | | - | 3.2 | 3.2 | | |
| | | 5.5 | | - | 3.9 | 3.9 | | |
| V _{t-} | Minimum Negative Threshold | 3.0 | T _A = Worst Case | - | 0.5 | 0.5 | V | |
| | | 4.5 | | - | 0.9 | 0.9 | | |
| | | 5.5 | | - | 1.1 | 1.1 | | |
| V _{H(MAX)} | Maximum Hysteresis | 3.0 | T _A = Worst Case | - | 1.2 | 1.2 | V | |
| | | 4.5 | | - | 1.4 | 1.4 | | |
| | | 5.5 | | - | 1.6 | 1.6 | | |
| V _{H(MIN)} | Minimum Hysteresis | 3.0 | T _A = Worst Case | - | 0.3 | 0.3 | V | |
| | | 4.5 | | - | 0.4 | 0.4 | | |
| | | 5.5 | | - | 0.5 | 0.5 | | |
| I _{OLD} | Minimum Dynamic | 5.5 | V _{OLD} = 1.65 V Max. | - | - | 75 | mA | |
| I _{OHD} | Output Current (Note 2) | 5.5 | V _{OHD} = 3.85 V Min. | - | - | -75 | mA | |
| I _{CC} (Note 3) | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | - | 2.0 | 20.0 | μA | |

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.
3. I_{IN} and I_{CC} at 3.0 V are guaranteed to be less than or equal to the respective limit at 5.5 V V_{CC}.

74AC14, 74ACT14

DC ELECTRICAL CHARACTERISTICS FOR ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Unit |
|---------------------|---|---------------------|---|------------------------|-------------------|---------------------------------|--|------|
| | | | | Typ | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1 V or V _{CC} - 0.1 V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50 μA | 4.49 | 4.34 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24 mA | - | 3.86 | 3.76 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24 mA (Note 4) | - | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50 μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24 mA | - | 0.36 | 0.44 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24 mA (Note 4) | - | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | - | ±0.1 | ±1.0 | | μA |
| V _{H(MAX)} | Maximum Hysteresis | 4.5 | T _A = Worst Case | - | 1.4 | 1.4 | | V |
| | | 5.5 | | - | 1.6 | 1.6 | | |
| V _{H(MIN)} | Minimum Hysteresis | 4.5 | T _A = Worst Case | - | 0.4 | 0.4 | | V |
| | | 5.5 | | - | 0.5 | 0.5 | | |
| V _{t+} | Maximum Positive Threshold | 4.5 | T _A = Worst Case | - | 2.0 | 2.0 | | V |
| | | 5.5 | | - | 2.0 | 2.0 | | |
| V _{t-} | Minimum Negative Threshold | 4.5 | T _A = Worst Case | - | 0.8 | 0.8 | | V |
| | | 5.5 | | - | 0.8 | 0.8 | | |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1 V | 0.6 | - | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current (Note 5) | 5.5 | V _{OLD} = 1.65 V Max. | - | - | 75 | | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85 V Min. | - | - | -75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | - | 2.0 | 20.0 | | μA |

4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0 ms, one output loaded at a time.

74AC14, 74ACT14

AC ELECTRICAL CHARACTERISTICS FOR AC

| Symbol | Parameter | V _{CC} (V) (Note 6) | T _A = +25°C, C _L = 50 pF | | | T _A = -40°C to +85°C, C _L = 50 pF | | Unit |
|------------------|-------------------|------------------------------|--|-----|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 3.3 | 1.5 | 9.5 | 13.5 | 1.5 | 15.0 | ns |
| | | 5.0 | 1.5 | 7.0 | 10.0 | 1.5 | 11.0 | |
| t _{PHL} | Propagation Delay | 3.3 | 1.5 | 7.5 | 11.5 | 1.5 | 13.0 | ns |
| | | 5.0 | 1.5 | 6.0 | 8.5 | 1.5 | 9.5 | |

6. Voltage range 3.3 is 3.3 V + 0.3 V. Voltage range 5.0 is 5.0 V + 0.5 V.

AC ELECTRICAL CHARACTERISTICS FOR ACT

| Symbol | Parameter | V _{CC} (V) (Note 7) | T _A = +25°C, C _L = 50 pF | | | T _A = -40°C to +85°C, C _L = 50 pF | | Unit |
|------------------|-------------------|------------------------------|--|-----|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 5.0 | 3.0 | 8.0 | 10.0 | 3.0 | 11.0 | ns |
| t _{PLH} | Propagation Delay | 5.0 | 3.0 | 8.0 | 10.0 | 3.0 | 11.0 | ns |

7. Voltage range 5.0 is 5.0 V + 0.5 V.

CAPACITANCE

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------|--|-------------------------|------------|------|
| C _{IN} | Input Capacitance | V _{CC} = OPEN | 4.5 | pF |
| C _{PD} | Power Dissipation Capacitance AC ACT | V _{CC} = 5.0 V | 25.0 80 | pF |

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 1 OF 2 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 2 OF 2 |

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

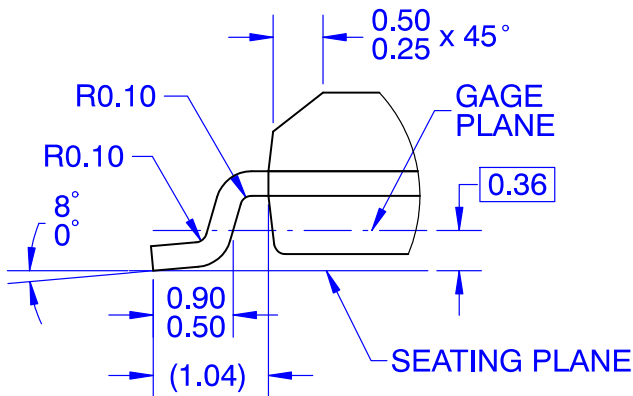
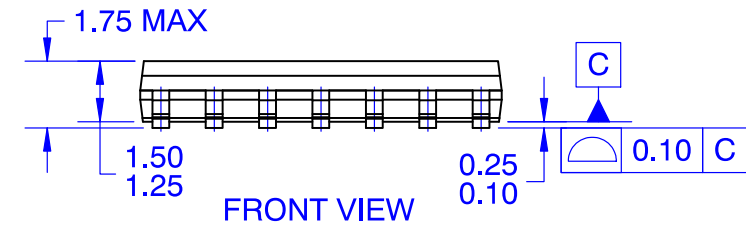
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



DETAIL A
SCALE 16 : 1

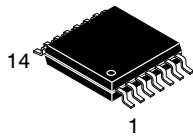
NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009

| | | |
|-------------------------|--------------------|--|
| DOCUMENT NUMBER: | 98AON13739G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC14 | PAGE 1 OF 1 |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

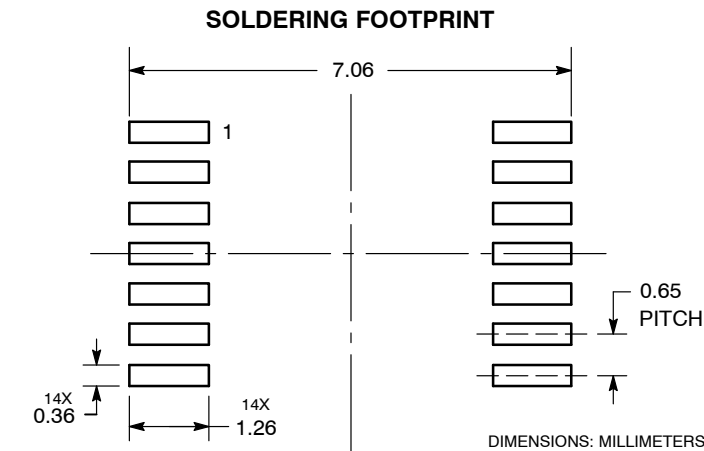
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



| | | |
|-------------------------|--------------------|--|
| DOCUMENT NUMBER: | 98ASH70246A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TSSOP-14 WB | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

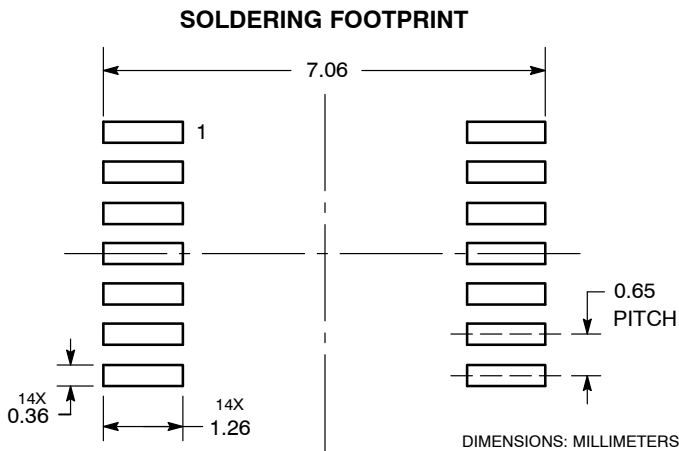
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



| | | |
|-------------------------|--------------------|--|
| DOCUMENT NUMBER: | 98ASH70246A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TSSOP-14 WB | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative