

**Display Elektronik GmbH**

# DATA SHEET

**EPD MODULE**

**DEE 128296B-W**

**2,9"**

**E-Paper Display**

Product Specification

Ver.: 1

**18.12.2021**

| <b>Version</b> | <b>Content</b>             | <b>Date</b> | <b>Producer</b> |
|----------------|----------------------------|-------------|-----------------|
| 0              | New Release                | 22.04.2021  | JQ              |
| 1              | Update Inspection Standard | 18.12.2021  | JQ              |
|                |                            |             |                 |
|                |                            |             |                 |
|                |                            |             |                 |
|                |                            |             |                 |

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## 1 General Description

DEE 128296B-W is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 2.9" active area contains 128x296 pixels, and has 2-bit full display capabilities. The module is a TFT array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2 Features

- ◆ 128×296pixels display
- ◆ White reflectance above 30%
- ◆ Contrast ratio above 8:1
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Landscape, portrait modes
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I<sup>2</sup>C signal master interface to read external temperature sensor

## 3 Application

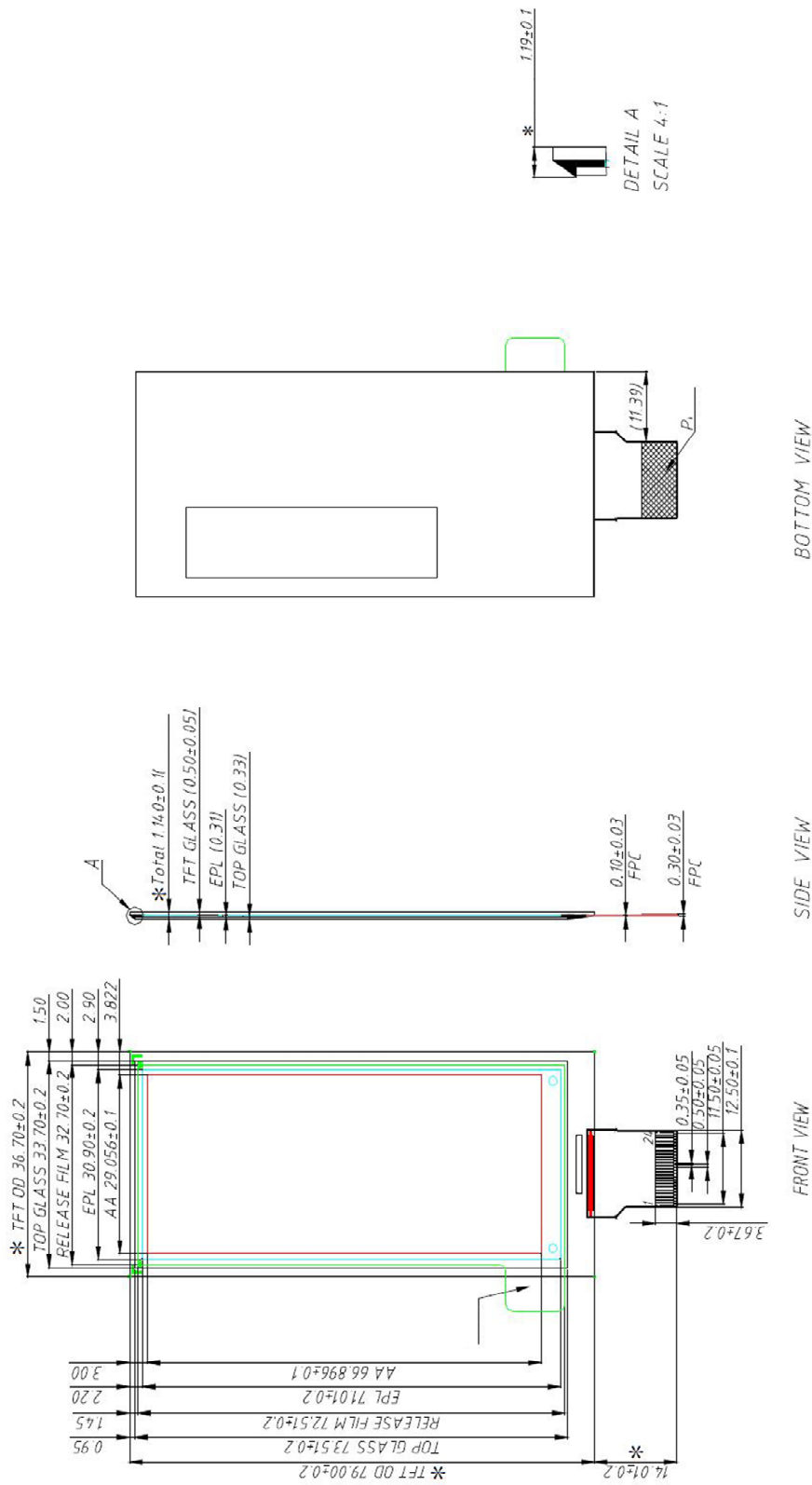
Electronic Shelf Label System

## 4 Mechanical Specification

### 4.1 Dimension

| Parameter           | Specifications       | Unit  |
|---------------------|----------------------|-------|
| Screen Size         | 2.9                  | Inch  |
| Display Resolution  | 128 x 296            | Pixel |
| Active Area         | 29.05 x 66.89        | mm    |
| Pixel Pitch         | 0.227 x 0.226        | mm    |
| Pixel Configuration | Rectangle            |       |
| Outline Dimension   | 36.70 x 79.00 x 1.14 | mm    |
| Weight              | 6.9                  | g     |

### 4.2 Mechanical Drawing of EPD Module



- NOTES:
1. Display mode 2.9" array for EPD;
  2. Unspecified Tolerance: ±0.20;
  3. Material conform to the RoHS standard;
  4. Mark "\*" for control DIM. reference dimension in I
  5. Product thickness include: TOP GLASS+EPL+TFT. EPL+TFT.

## 5 Input/output Pin Assignment

| No. | Name  | I/O | Description   | Remark   |
|-----|-------|-----|---|----------|
| 1   | NC    | /   | Do not connect with other NC pins   |          |
| 2   | GDR   | O   | N-Channel MOSFET Gate Drive Control   |          |
| 3   | RESE  | I   | Current Sense Input for the Control Loop  |          |
| 4   | NC    | /   | Do not connect with other NC pins   |          |
| 5   | VDHR  | C   | Positive Source driving voltage 1   |          |
| 6   | TSCL  | O   | I <sup>2</sup> C Interface to digital temperature sensor Clock pin  |          |
| 7   | TSDA  | I/O | I <sup>2</sup> C Interface to digital temperature sensor Data pin   |          |
| 8   | BS    | I   | Bus Interface selection pin   | Note 5-4 |
| 9   | BUSYN | O   | Busy state output pin   | Note 5-3 |
| 10  | RSTN  | I   | Reset signal input. Active Low.   |          |
| 11  | D/C   | I   | Data /Command control pin   | Note 5-2 |
| 12  | CSB   | I   | Chip select input pin   | Note 5-1 |
| 13  | SCL   | I   | Serial Clock pin (SPI)  |          |
| 14  | SDA   | I   | Serial Data pin (SPI)   |          |
| 15  | VDD   | P   | Power Supply for interface logic pins   |          |
| 16  | VDD   | P   | Power Supply for the chip   |          |
| 17  | VSS   | P   | Ground  |          |
| 18  | VDDD  | C   | Core logic power pin<br>VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances |          |
| 19  | VPP   | P   | Power Supply for OTP Programming  |          |
| 20  | VSH   | C   | Positive Source driving voltage 2   |          |
| 21  | VGH   | C   | Positive Gate driving voltage   |          |
| 22  | VSL   | C   | Negative Source driving voltage   |          |
| 23  | VGL   | C   | Negative Gate driving voltage   |          |
| 24  | VCOM  | C   | VCOM driving voltage  |          |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin Note

5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

| BS State | MCU Interface  |
|----------|--|
| L        | 4-lines serial peripheral interface(SPI)               |
| H        | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

## 6 Electrical Characteristics

### 6.1 Absolute Maximum Rating

| Parameter            | Symbol    | Rating               | Unit |
|----------------------|-----------|----------------------|------|
| Logic supply voltage | $V_{dd}$  | -0.5 to +4.0         | V    |
| Logic Input voltage  | $V_{IN}$  | -0.5 to $V_{dd}+0.5$ | V    |
| Logic Output voltage | $V_{OUT}$ | -0.5 to $V_{dd}+0.5$ | V    |

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

### 6.2 Panel DC Characteristics

The following specifications apply for:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ ,  $T_{OPR}=25^{\circ}C$ .

| Parameter                 | Symbol         | Condition            | Applicable pin | Min.         | Typ. | Max.         | Unit    |
|---------------------------|----------------|----------------------|----------------|--------------|------|--------------|---------|
| Logic supply voltage      | $V_{dd}$       | -                    | VDD            | 2.4          | 3.0  | 3.6          | V       |
| High level input voltage  | $V_{IH}$       | -                    | -              | $0.8 V_{dd}$ | -    | -            | V       |
| Low level input voltage   | $V_{IL}$       | -                    | -              | -            | -    | $0.2 V_{dd}$ | V       |
| High level output voltage | $V_{OH}$       | $I_{OH} = -100\mu A$ | -              | $0.9 V_{dd}$ | -    | -            | V       |
| Low level output voltage  | $V_{OL}$       | $I_{OL} = 100\mu A$  | -              | -            | -    | $0.1 V_{dd}$ | V       |
| OTP Program voltage       | $V_{PP}$       | -                    | VPP            | -            | 7.5  | -            | V       |
| Typical power panel       | $P_{TYP}$      | -                    | -              | -            | 12   | 30           | mW      |
| Deep sleep mode           | $P_{STPY}$     | -                    | -              | -            | 3    | -            | $\mu W$ |
| Typical operating current | $I_{opr\_VDD}$ | $V_{dd}=3.0V-$       | -              | -            | 4.0  | 10           | mA      |

|                                 |                  |  |     |     |    |      |     |
|---------------------------------|------------------|--|-----|-----|----|------|-----|
| Sleep mode current              | Islp_VDD         | VDD=3.0V<br>DC/DC OFF<br>No clock<br>No output load<br>Ram data retain     | VDD | -   | 20 | --   | uA  |
| Deep sleep mode current         | IdslpVDD         | VDD=3.0V<br>DC/DC OFF<br>No clock<br>No output load<br>Ram data not retain | VDD | -   | 1  | --   | uA  |
| Operation temperature range     | T <sub>OPR</sub> | -  | -   | 0   | -  | 50   | °C  |
| Operation illuminance intensity | E                | indoor only  | -   | -   | -  | 2000 | lux |
| Storage temperature range       | T <sub>STG</sub> | -  | -   | -25 | -  | 60   | °C  |
| Storage relative humidity       | RHst             | -  | -   | 30  | -  | 60   | %RH |

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

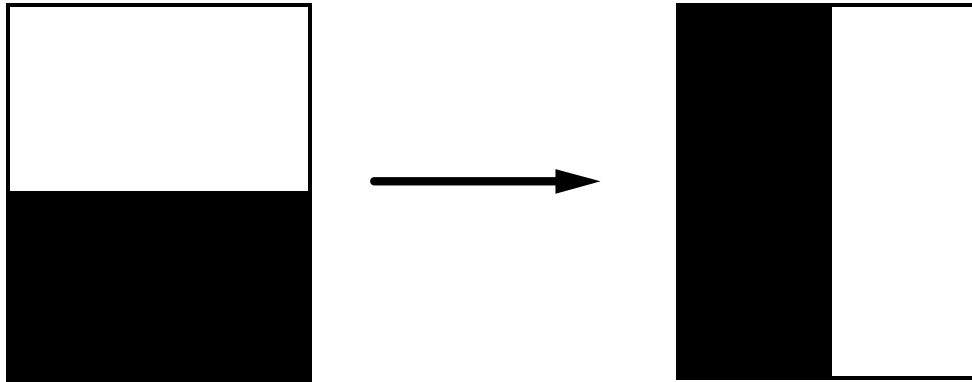


Figure 10-2 The typical power consumption measure pattern

- The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

### 6.3 Panel DC Characteristics (Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T<sub>OPR</sub> =25°C.

| Parameter           | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------|--------|-----------|----------------|------|------|------|------|
| VCOM output voltage | VCOM   | -         | VCOM           | -3.0 | -    | -0.2 | V    |



## 6.4 Panel AC Characteristics

### 6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name   | Data/Comnnand Interface |      | Control Signal |     |      |
|------------|-------------------------|------|----------------|-----|------|
|            | SDA                     | SCL  | CSB            | D/C | RSTN |
| 4-wire SPI | SDIN                    | SCLK | CSB            | D/C | RSTN |
| 3-wire SPI | SDIN                    | SCLK | CSB            | L   | RSTN |

Table 10-4-1: MCU interface assignment under different bus interface mode

### 6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

| Function      | CSB | D/C | SCLK |
|---------------|-----|-----|------|
| Write command | L   | L   | ↑    |
| Write data    | L   | H   | ↑    |

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

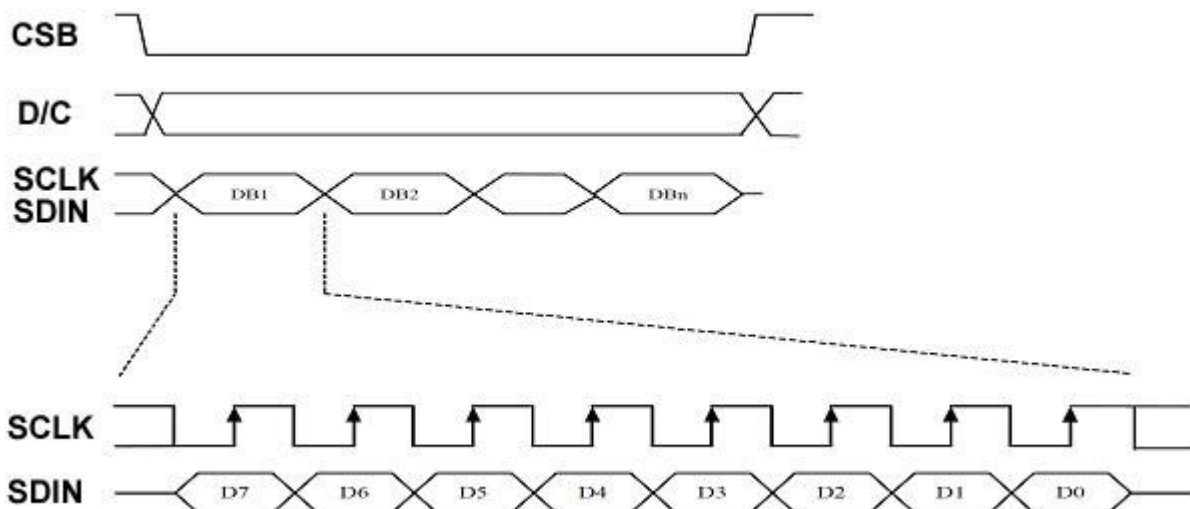


Figure 10-4-2: Write procedure in 4-wire SPI mode

**6.4.3 MCU Serial Interface (3-wire SPI)**

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

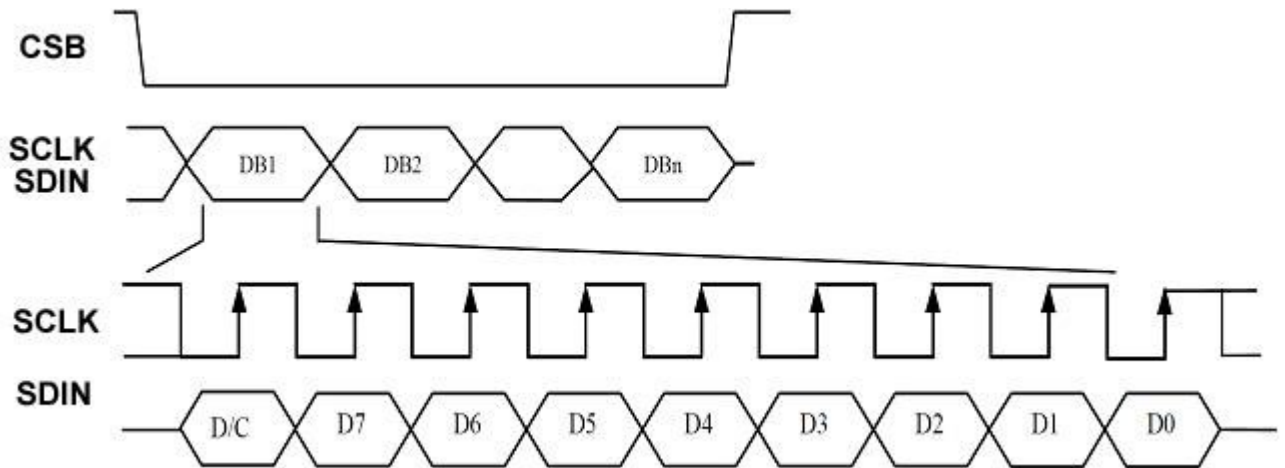
The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

| Function      | CSB | D/C    | SCLK |
|---------------|-----|--------|------|
| Write command | L   | Tie    | ↑    |
| Write data    | L   | LOWTie | ↑    |

Note: ↑ stands for rising edge of signal <sup>LOW</sup>

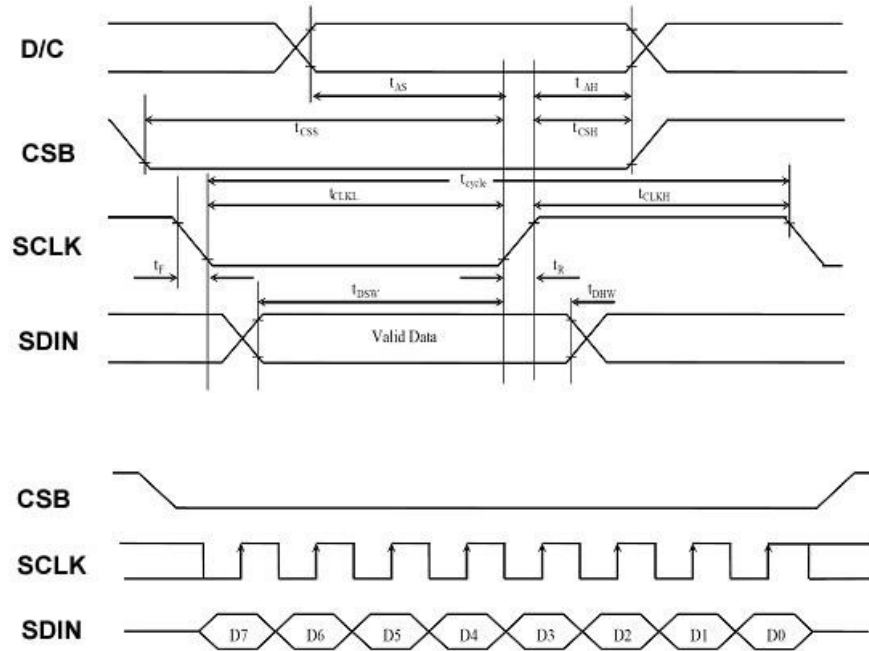
**Table 10-4-3: Control pins of 3-wire Serial interface**



**Figure 10-4-3: Write procedure in 3-wire SPI mode**

**6.4.4 Interface Timing**

The following specifications apply for: VSS=0V, VDD =3.0V, T<sub>OPR</sub> =25°C.



**Figure 10-4-4: Serial interface characteristics**

(V<sub>dd</sub> - VSS = 2.4V to 3.3V, T<sub>OPR</sub> = 25°C, CL=20pF)

| Symbol             | Parameter              | Min. | Typ. | Max. | Unit |
|--------------------|------------------------|------|------|------|------|
| t <sub>cycle</sub> | Clock Cycle Time       | 250  | -    | -    | ns   |
| t <sub>AS</sub>    | Address Setup Time     | 150  | -    | -    | ns   |
| t <sub>AH</sub>    | Address Hold Time      | 150  | -    | -    | ns   |
| t <sub>CSS</sub>   | Chip Select Setup Time | 120  | -    | -    | ns   |
| t <sub>CSH</sub>   | Chip Select Hold Time  | 60   | -    | -    | ns   |
| t <sub>DSW</sub>   | Write Data Setup Time  | 50   | -    | -    | ns   |
| t <sub>DHW</sub>   | Write Data Hold Time   | 15   | -    | -    | ns   |
| t <sub>CLKL</sub>  | Clock Low Time         | 100  | -    | -    | ns   |
| t <sub>CLKH</sub>  | Clock High Time        | 100  | -    | -    | ns   |
| t <sub>R</sub>     | Rise Time [20% ~ 80%]  | -    | -    | 15   | ns   |
| t <sub>F</sub>     | Fall Time [20% ~80%]   | -    | -    | 15   | ns   |

**Table 10-4-4: Serial Interface Timing Characteristics**

## 7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

| Symbol               | Parameter          | Conditions | Values |          |     | Units | Notes |
|----------------------|--------------------|------------|--------|----------|-----|-------|-------|
|                      |                    |            | Min.   | Typ.     | Max |       |       |
| R                    | White Reflectivity | White      | 30     | 35       | -   | %     | 11-1  |
| CR                   | Contrast Ratio     |            | 8:1    | 10:1     | -   | -     | 11-2  |
| White $\Delta$ L 24h | Reduce             |            | -      | $\leq 4$ | -   | -     | -     |
| T <sub>update</sub>  | Image update time  | at 25 °C   | -      | 3300     | -   | ms    | -     |

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

## 8 Handling, Safety, and Environment Requirements

### Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

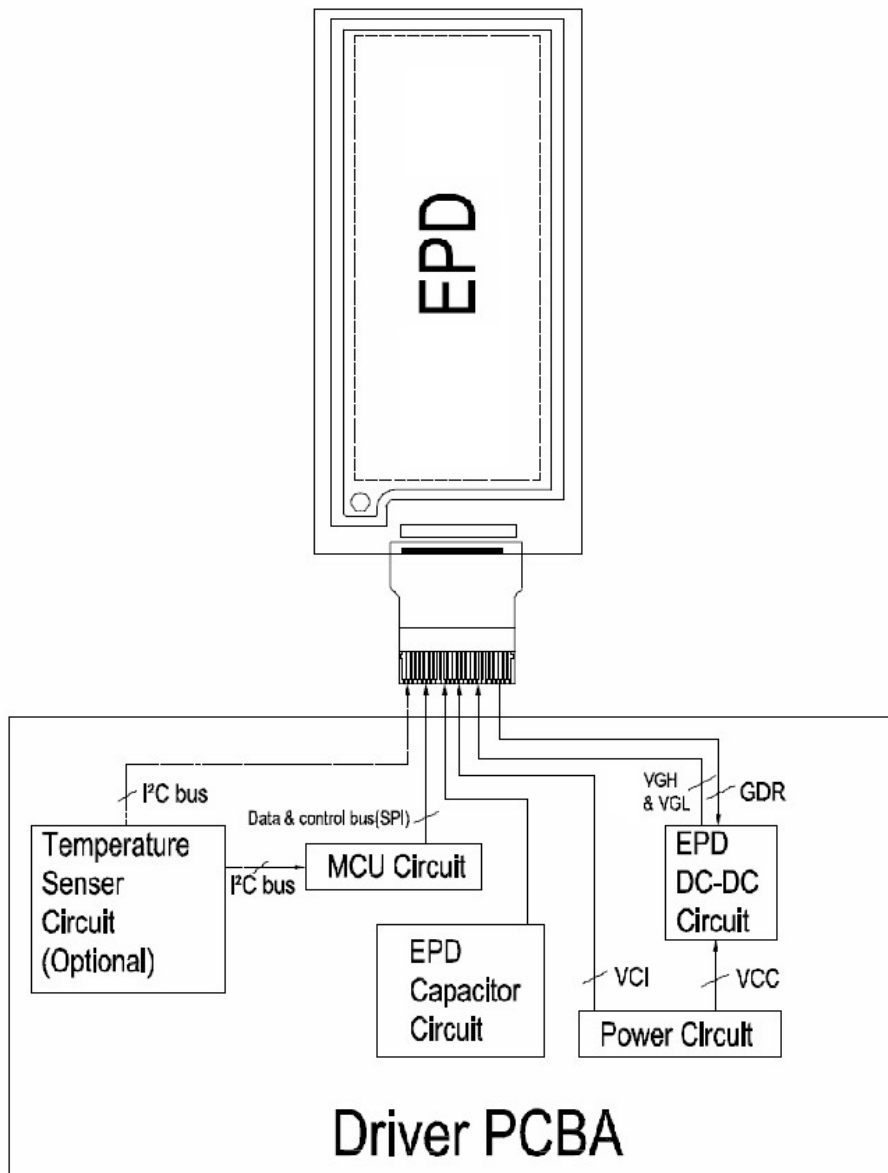
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

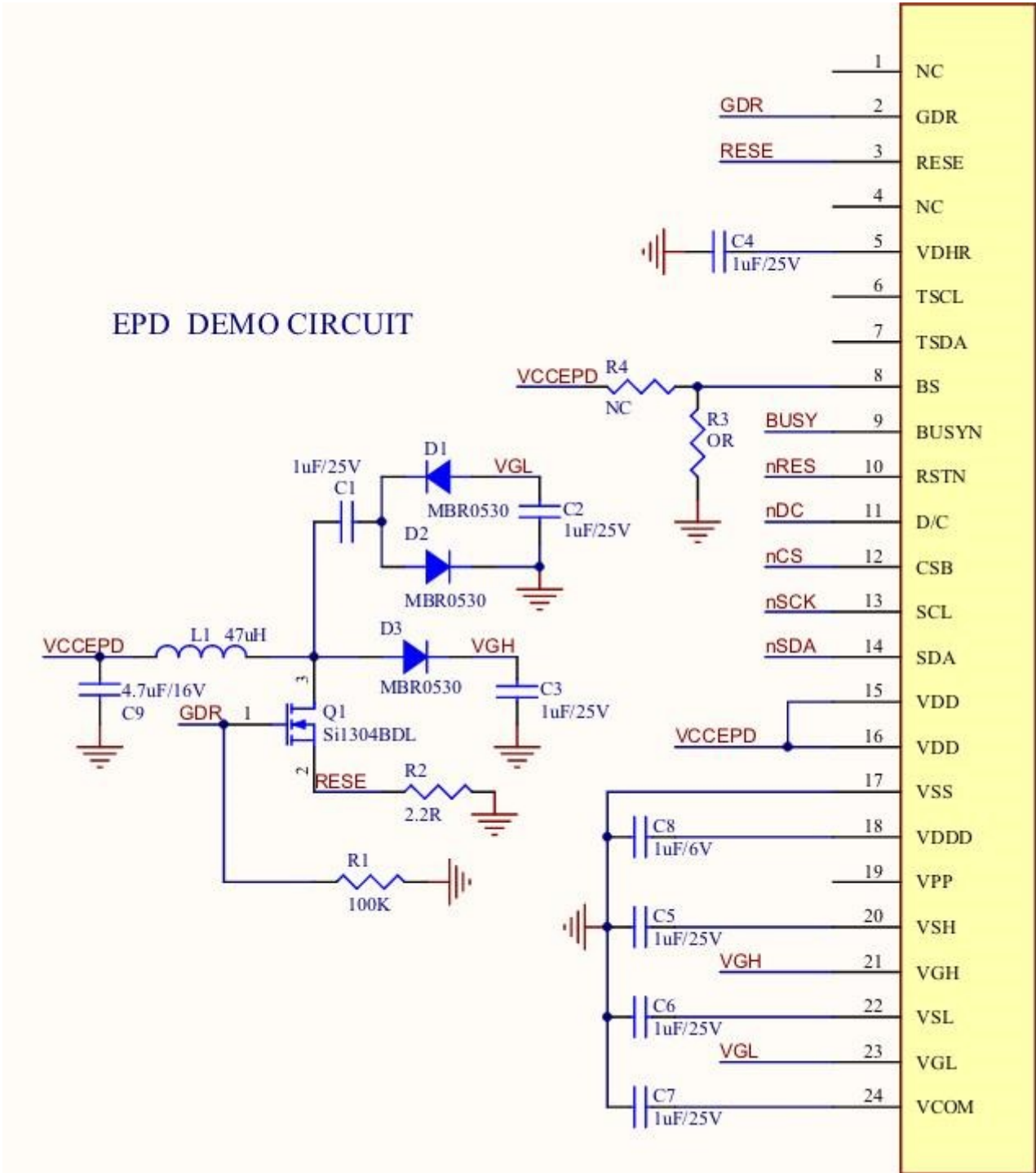
## 9 Reliability Test

| No. | Test                                     | Condition   | Method                   | Remark   |
|-----|--|---|--------------------------|--|
| 1   | HighTemperature Operation                | T = +50°C, RH = 30% for 240 hrs   | IEC 60 068-2-2Bp         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 2   | Low-Temperature Operation                | T = 0°C for 240 hrs   | IEC 60 068-2-2Ab         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 3   | High-Temperature Storage                 | T = +70°C, RH=23% for 240 hrs   | IEC 60 068-2-2Bp         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 4   | Low-Temperature Storage                  | T = -25°C for 240 hrs   | IEC 60 068-2-1Ab         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 5   | High-Temperature, HighHumidity Operation | T = +40°C, RH = 90% for 168 hrs   | IEC 60 068-2-3CA         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 6   | High Temperature, High- Humidity Storage | T = +60°C, RH=80% for 240hrs  | IEC 60 068-2-3CA         | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 7   | Thermal Shock                            | 1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles  | IEC 60 068-2-14          | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 8   | Package Vibration                        | 1.04G, Frequency:<br>10~500Hz<br>Direction: X,Y,Z<br>Duration: 1 hours in each direction                      | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 9   | Package Drop Impact                      | Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces<br>One drop for each | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 10  | Electrostatic Effect (nonoperating)      | Machine model +/- 250V, 0Ω, 200pF   | IEC 62179, IEC 62180     | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |

### 10 Block Diagram



### 11 Typical Application Circuit with SPI Interface





## 12 Inspection Standard

### 12.1 Appearances Inspection Standard

#### 12.1.1 Appearances Specification

his appearance inspection shall be applied to segment EPD modules.

#### 12.1.2 Inspection Conditions

Viewing Angle:  $\alpha = \pm 45^\circ$

Viewing Distance: 30cm $\pm$ 10cm

Ambient Luminance: 700~1000 Lux.

Supply Voltage: Typical value described on the Electrical Characteristics

Environment Ambient Temperature: 20 $\square$ ~25 $\square$

Environment Ambient Humidity: 40~70%RH

ESD should be controlled within  $\pm 200V$

#### 12.1.3 Inspection Level: Level II

Sampling table: GB/T 2828.1-2012 II, unless otherwise agreed in writing.

#### 12.1.4 Acceptance Quality Level (AQL) Major

Defect: 0.65 , Minor Defect: 1.5

#### 12.1.5 Classification of Defects

Defects are classified as either a major or a minor defect defined as below.

Major Defect :It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.

Minor Defect :It is a defect that will not result in functioning problem with deviation classified.

### 12.2 Quality Criteria

#### 12.2.1 Zone Definitions

A Zone: EPD Active Area (not including border)

B Zone: Out of Active Area

## 12.2.2 Appearances Criteria

As shown in the tables below. If any other items, standard values or applicable zones are required to be defined, a written agreement shall be signed, and otherwise a limited sample shall be made for reference.

**Major Defects:**

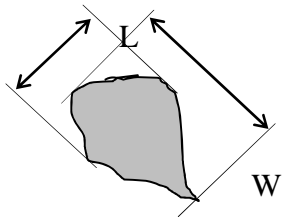
| Item             | Description                                   | Classification |
|------------------|---|----------------|
| No Display       | No display shown on screen due to malfunction | Major          |
| Line Missing     | Line missing                                  | Major          |
| Abnormal Display | Unusual pattern or function displayed         | Major          |
| TFT Broken       | TFT broken by external force                  | Major          |

**Minor Defects:**

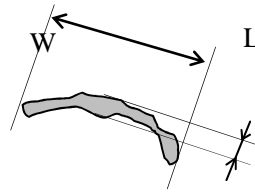
| Item        |   | Criteria  | Specific Zone |        |
|-------------|---|---|---------------|--------|
| Name        | Description   |   | A Zone        | B Zone |
| Dot defect  | Spot/<br>Air bubble/<br>Foreign material in<br>dot shape                  | $D \leq 0.30\text{mm}$  | Ignore        | Ignore |
|             |   | $0.30\text{mm} < D \leq 0.50\text{mm}$  | $\leq 5$      |        |
|             |   | $D > 0.50\text{mm}$   | 0             |        |
| Line defect | Scratch on top<br>surface/ Foreign<br>material in line or<br>spiral shape | $L \leq 1.0 \text{ mm} , W \leq 0.15\text{mm}$                                  | Ignore        | Ignore |
|             |   | $1.0\text{mm} < L \leq 5.0\text{mm} \ \& \ 0.15\text{mm} < W \leq 0.5\text{mm}$ | $\leq 4$      |        |
|             |   | $L > 5.0\text{mm} \ \text{or} \ W > 0.5\text{mm}$                               | 0             |        |
| Chipping    | Corner chip   | Not affect the display, not have diffuse or comminuted cracks                   |               |        |
|             | Edge chip   |   |               |        |
| Curl        | Curl for Panel  | $\leq 1.0 \text{ mm}$   |               |        |

**Remarks:**

Definitions of “line” and “dot”:

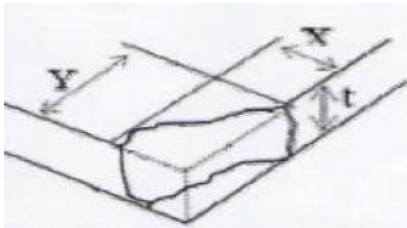


a. Line

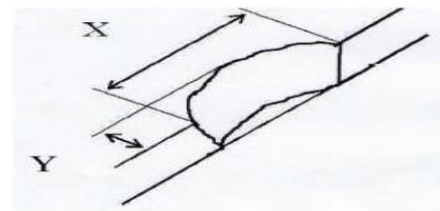


b. Dot

When  $L \leq 0.5\text{mm}$  or  $L < 4W$ , defined as a dot. Definitions of “Chipping”:



c. Corner chip



d. Edge chip