Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEE 172072A – W

2,0“
E-PAPER DISPLAY

Product Specification **Ver.: 3**

24.12.2013

DOCUMENT REVISION	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
0	30.03.2012	First Release.	LY	MH
1	15.10.2012	Items 1 were updated. The table 5 was updated.	LY	MH
2	12.09.2013	Items 1 were updated. The table 5 was updated.	LY	MH
3	24.12.2013	Items 1 to 2 were updated. The command table was updated.	LY	MH

CONTENTS

1. General Description

DEE 172072A – W is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.04" active area contains 172x72 pixels, and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

- ◆172×72 pixels display
- ◆White reflectance above 30%
- ◆Contrast ratio above 7:1
- ◆Ultra wide viewing angle
- ◆Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape, portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform stored in On-chip OTP
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I2C signal master interface to read extremely temperature sensor

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Parameter	Specifications	Unit	Remark
Screen Size	2.04	Inch	-
Display Resolution	172 x 72 (or 72 x 172)	Pixel	dpi:95
Active Area	20.16 x 48.16 (or 48.16 x 21.16)	mm	-
Pixel Pitch	0.280 x 0.280	mm	-
Pixel Configuration	Rectangle	-	-
Outline Dimension	29.20 x 59.20 x 1.18 (or 59.20 x 29.20 x 1.18)	mm	-

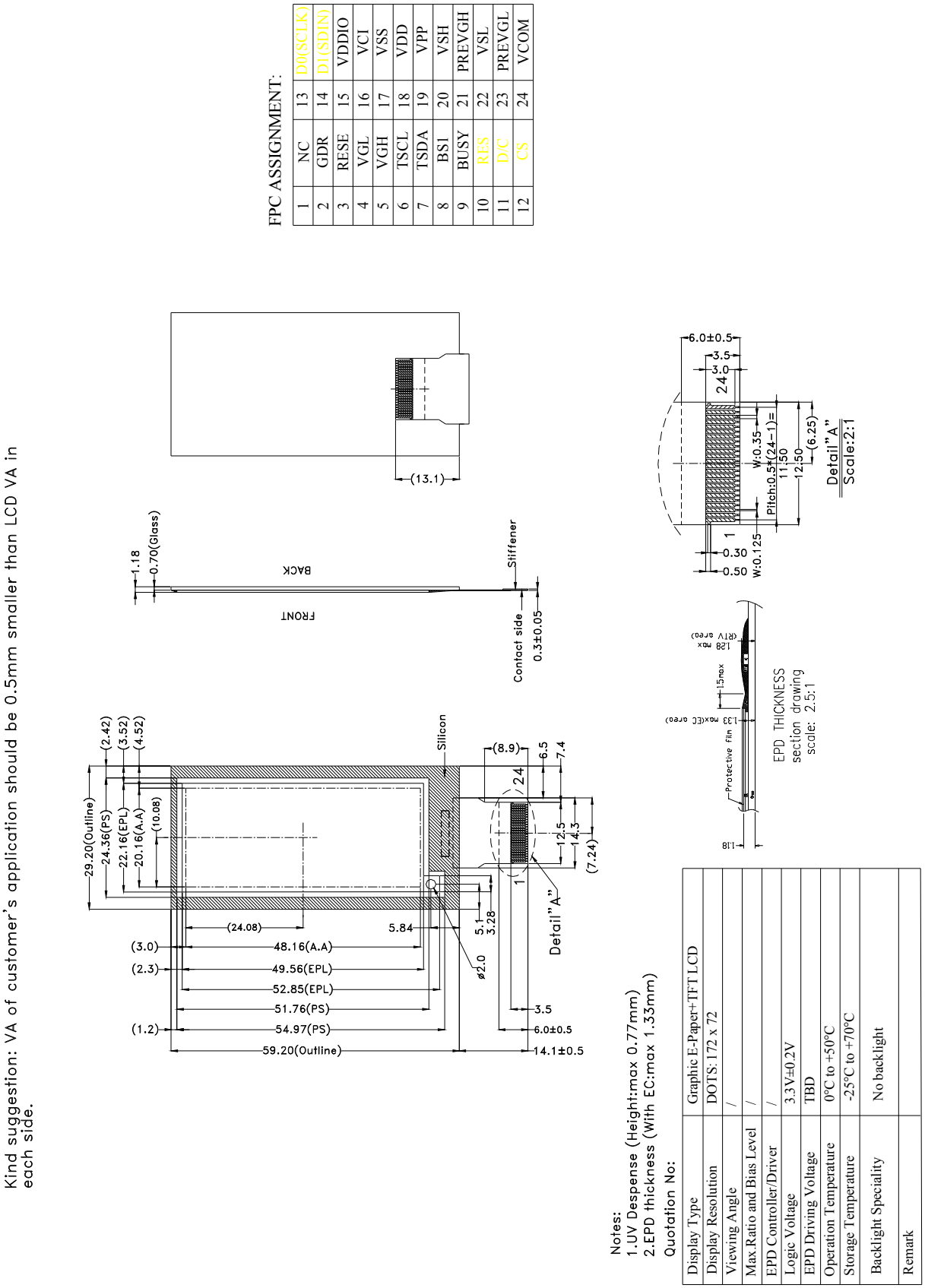


Figure 1: Module Specification

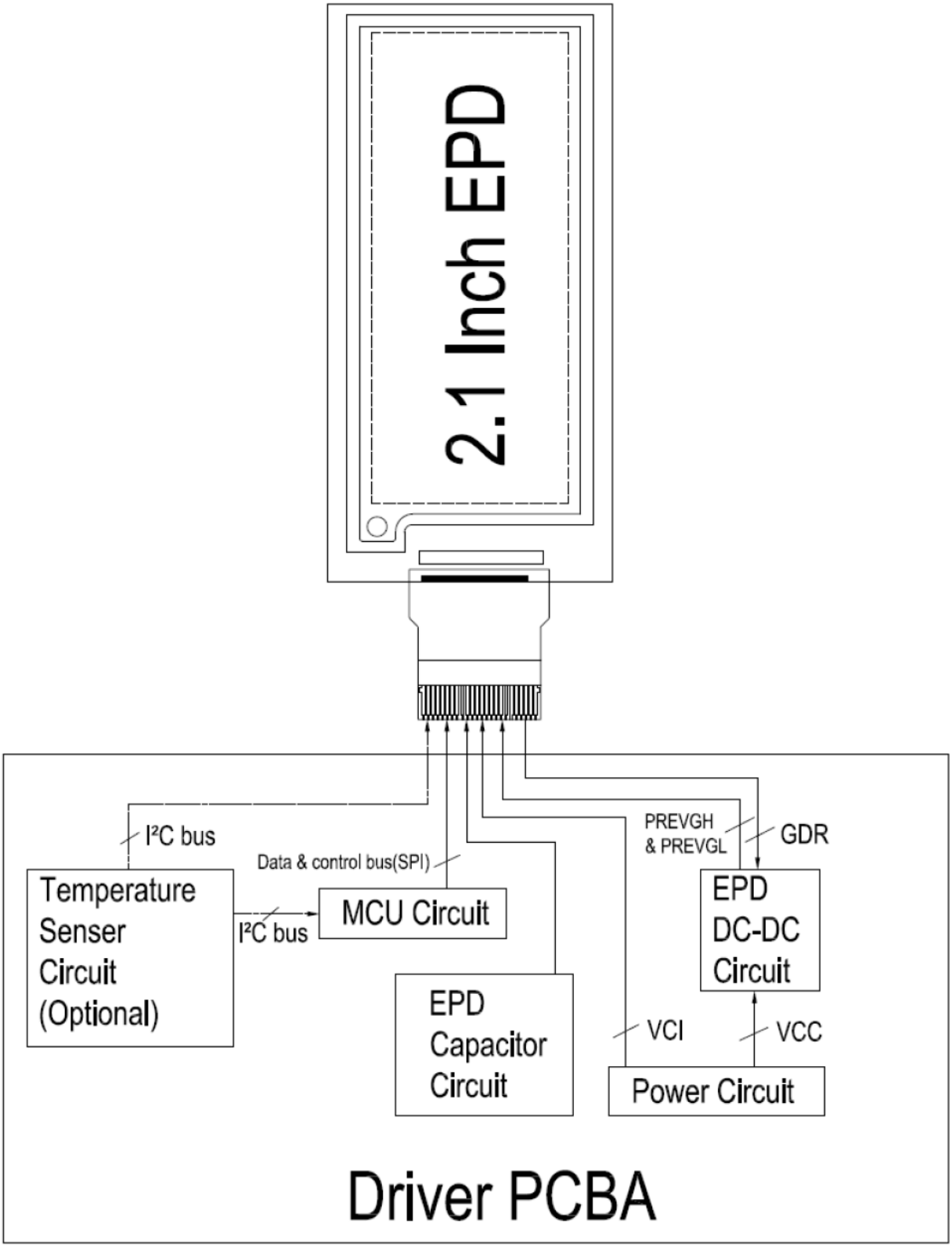


Figure 2: Block Diagram

3. Interface Signals

Pin #	Type	Single	Description	Remark
1	-	NC	Do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	-
3	O	RESE	Current Sense Input for the Control Loop	-
4	C	VGL	Negative Gate driving voltage	-
5	C	VGH	Positive Gate driving voltage	-
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	-
7	I/O	TSDA	I2C Interface to digital temperature sensor Data pin	-
8	I	BS1	Bus selection pin	Note 5
9	O	BUSY	Busy state output pin	Note 4
10	I	RES #	Reset	Note 3
11	I	D/C #	Data /Command control pin	Note 2
12	I	CS #	Chip Select input pin	Note 1
13	I/O	D0	serial clock pin (SPI)	-
14	I/O	D1	serial data pin (SPI)	-
15	C	VDDIO	Power for I/O logic pins. Connect to VCI.	-
16	I	VCI	Power Supply pin for the display driver chip	-
17	I	VSS	Ground	-
18	C	VDD	Main logic power supply pin	-
19	C	VPP	Power Supply for OTP Programming	-
20	C	VSH	Positive Source driving voltage	-
21	C	PREVGH	Power Supply pin for VGH and VSH	-
22	C	VSL	Negative Source driving voltage	-
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	-
24	C	VCOM	VCOM driving voltage	-

Note 1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW in parallel interface. When CS# is not in use, please connect to VCI or VSS.

Note 2: This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at [7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be interpreted as command.

Note 3: This pin is reset signal input. Active Low.

Note 4: This pin is busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. e.g., The chip would put Busy pin High when

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5: Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VCI	-0.5 to +3.6	V
Logic Input Voltage	VIN	-0.5 to VCI +0.5	V
Logic Output Voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp. Range	TOPR	0 to +50	℃
Storage Temp. Range	TSTG	-25 to +70	℃

5. Electrical Specifications

5.1 Panel DC Characteristics

The following specifications apply for: VSS = 0V, VCI = 3.0V, TA = 25□

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	VSS		-	-	0	-	V
Maximum image update Time at 25℃	-		-	-	1800	-	ms
Logic supply voltage	VCI	-	VCI	2.4	3.0	3.3	V
High level input voltage	VIH	-	-	0.8 VCI	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2 VCI	V
High level output voltage	VOH	IOH = -100uA	-	0.9 VCI	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	-	-	0.1 VCI	V
OTP Program voltage	VPP	-	VPP	-	7.5	-	V
Typical power panel	PTYP	-	-	-	24	36	mW
Standby power panel	PSTPY	-	-	-	0.006	-	mW
Typical operating current	Iopr_VCI	-	-	-	8.0	-	mA
Sleep mode current	Islp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data retain	VCI	-	35	50	uA
Deep sleep mode current	Idslp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data not retain	VCI	-	2	5	uA
Operation temperature range	TOPR	-	-	0	-	50	°C
Storage temperature range	TSTG	-	-	-20	-	70	°C

Notes:

1. The typical operating current is measured with following transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern.
2. The standby power is the consumed power when the panel controller is in standby mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by DISPLAY.

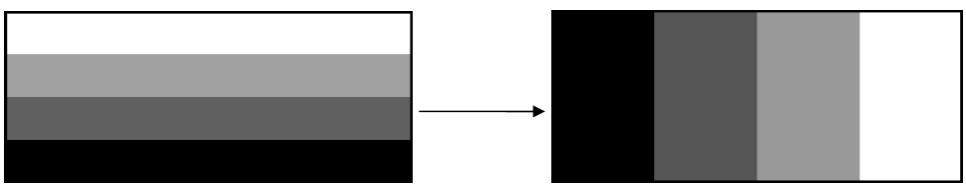


Figure: The typical power consumption measure pattern

5.2 Panel DC Characteristics (Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VDD operation voltage	VDD	-	VDD	1.7	1.8	1.9	V
VCOM output voltage	VCOM	-	VCOM	-4.0	-	+0.2	V
Gate output voltage	VGATE	-	G0-171	-20	-	+22	V
Gate output peak to peak voltage	VGATE(p-p)	-	G0-171	-	-	42	V
Positive Source output voltage	VSH	-	S0-71	+10	-	+17	V
Negative Source output voltage	VSL	-	S0-71	-	-VSH	-	V

5.3 Panel AC Characteristics

5.3.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

MCU interface assignment under different bus interface mode

Pin Name	Data/Connnand Interface		Control Signal		
Bus interface	**D1**	**D0**	**CS#**	**D/C#**	**RES#**
4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
3-wire SPI	SDIN	SCLK	CS#	L	RES#

5.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Control pins of 4-wire Serial interface

Function	CS#	D/C#	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0.

D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

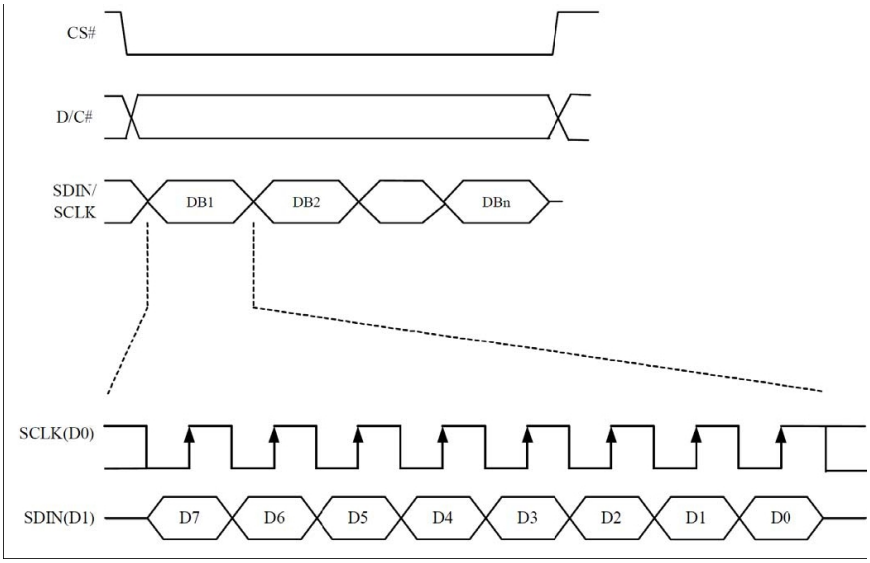


Figure: Write procedure in 4-wire SPI mode

5.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Control pins of 3-wire Serial interface

Function	CS#	D/C#	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

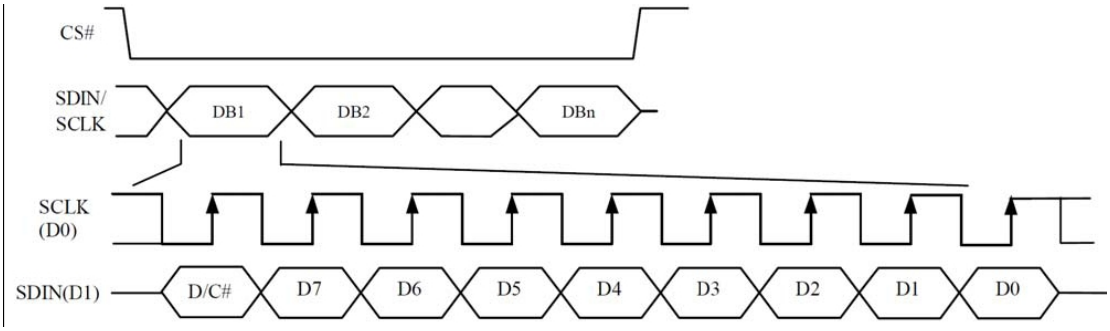


Figure: Write procedure in 3-wire SPI mode

5.3.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.3V	CL	0.95	1	1.05	MHz

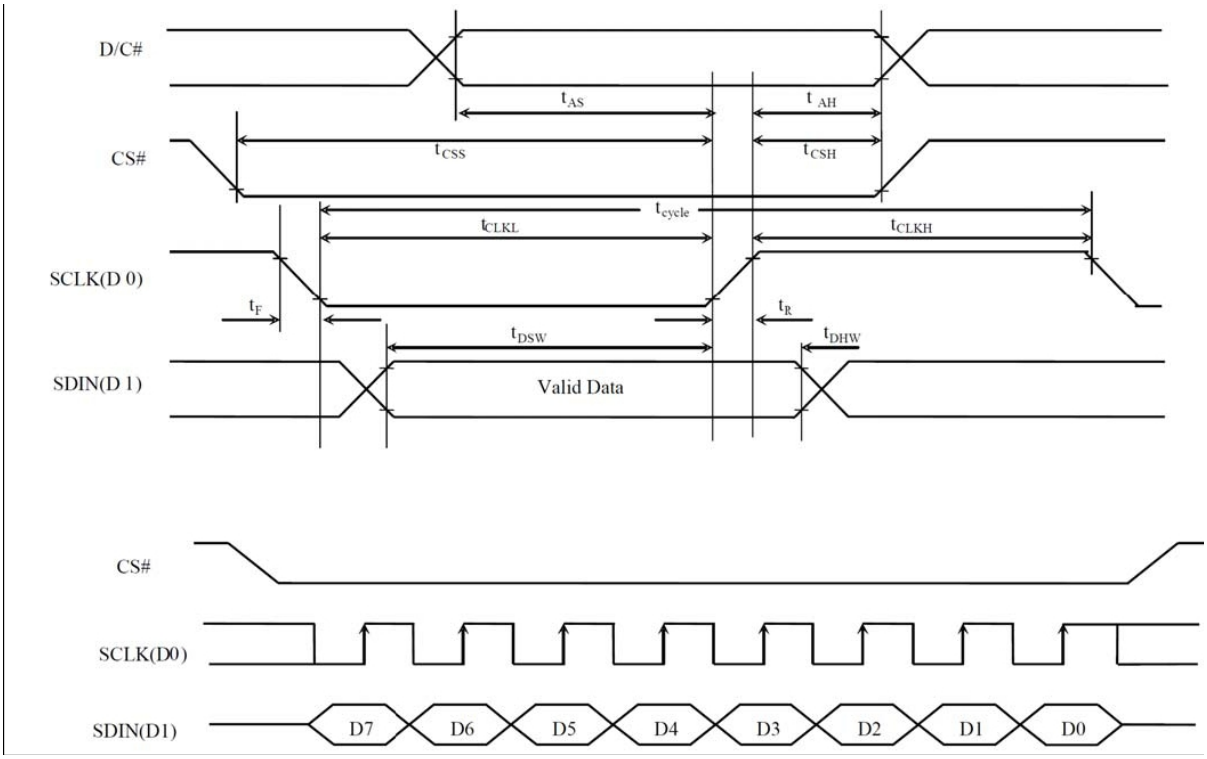


Figure: Serial interface characteristics

(V_{CI} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Table: Serial Interface Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
tcycle	Clock Cycle Time	250	-	-	ns
tAS	Address Setup Time	150	-	-	ns
tAH	Address Hold Time	150	-	-	ns
tCSS	Chip Select Setup Time	120	-	-	ns
tCSH	Chip Select Hold Time	60	-	-	ns
tDSW	Write Data Setup Time	50	-	-	ns
tDHW	Write Data Hold Time	15	-	-	ns
tCLKL	Clock Low Time	100	-	-	ns
tCLKH	Clock High Time	100	-	-	ns
tR	Rise Time [20% ~ 80%]	-	-	15	ns
tF	Fall Time [20% ~80%]	-	-	15	ns

5.4 Command Table

Fundamental Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
1	0	-	0	0	0	0	0	A_2	A_1	A_0	Status Read	Read Driver status on • A2: BUSY flag • A1,A0: Chip ID (01 as default)
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[7:0]: MUX setting as A[7:0] + 1 POR = B3h + 1 MUX B[2:0]: Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD='0', G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … [POR] GD='1', G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0, G0, G1, G2, G3…G179 (left and right gate interlaced) [POR] SM=1, G0, G2, G4 …G178, G1, G3, …G179 B[0]: TB TB = 0, scan from G0 to G179 [POR] TB = 1, scan from G179 to G0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	02	0	0	0	0	0	0	1	0	Reserve	
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[7:4]: VGH, 15 to 22V in 0.5V step
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												VGH 0000 15.0 0001 15.5 0010 16.0 0011 16.5 0100 17.0 0101 17.5 0110 18.0 0111 18.5 1000 19.0 1001 19.5 1010 20.0 1011 20.5 1100 21.0 1101 21.5 1110 22.0 [POR] Others N/A A[3:0]: VGL, -15 to -20V in 0.5V step VGL default at -20V VGL 0000 -15.0 0001 -15.5 0010 -16.0 0011 -16.5 0100 -17.0 0101 -17.5 0110 -18.0 0111 -18.5 1000 -19.0 1001 -19.5 1010 -20.0 [POR] Others N/A
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude A[3:0]: VSH/VSL 10V to 17V in 0.5V step VSH/VSL 0000 10.0 0001 10.5 0010 11.0 0011 11.5 0100 12.0 0101 12.5 0110 13.0 0111 13.5 1000 14.0 1001 14.5 1010 15.0 [POR] 1011 15.5 1100 16.0 1101 16.5 1110 17.0 Others N/A
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	05	0	0	0	0	0	1	0	1	Reserve	

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	position	gate driver. The valid range is from 0 to 179. TB=0: SCN [7:0] = A[7:0] 00h [POR] TB=1: SCN [7:0] = 179 - A[7:0] 00h [POR]
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A_0		A[0] : Description 0 [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0]: Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2]: Set the direction in which the address counter is updated automatically after data are written to the RAM. A[2] = 0, the address counter is updated in the X direction. [POR] A[2] = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command
0	0	13	0	0	0	1	0	0	1	1	Reserve	
0	0	14	0	0	0	1	0	1	0	0	Reserve	
0	0	15	0	0	0	1	0	1	0	1	Reserve	
0	0	16	0	0	0	1	0	1	1	0	Reserve	
0	0	17	0	0	0	1	0	1	1	1	Reserve	
0	0	18	0	0	0	1	1	0	0	0	Reserve	
0	0	19	0	0	0	1	1	0	0	1	Reserve	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	1B	0	0	0	1	1	1	0	1	Temperature Sensor Control (Read from	Read from temperature register. X[7:0] – MSByte
1	1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		

Note:If the module enter deep sleep mode, it must execute hardware RESET function to exit the deep sleep mode.

Fundamental Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
1	1		Y_7	Y_6	Y_5	Y_4	0	0	0	0	temperature register)	Y[7:4] – LSByte
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to temperature sensor)	Write Command to temperature sensor A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	1D	0	0	0	1	1	1	0	1	Temperature Sensor Control (Load temperature register with temperature sensor reading)	Load temperature register with temperature sensor reading BUSY=H for whole loading period The command required CLKEN=1.
0	0	1E	0	0	0	1	1	1	1	0	Reserve	
0	0	1F	0	0	0	1	1	1	1	1	Reserve	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update	Option for Display Update

Fundamental Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Control 1</td><td>Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A [7]
1 Enable bypass
0 Disable bypass [POR]

A[5:4] value will be used as for bypass
00 [POR]

A[3:0] Initial Update Option - Source Control

<table>
<tr><th></th><th>GSC A[3:2]</th><th>GSD A[1:0]</th></tr>
<tr><td>0000</td><td>GS0</td><td>GS0</td></tr>
<tr><td>0001</td><td>GS0</td><td>GS1</td></tr>
<tr><td>0010</td><td>GS0</td><td>GS2</td></tr>
<tr><td>0011 [POR]</td><td>GS0</td><td>GS3</td></tr>
<tr><td>0100</td><td>GS1</td><td>GS0</td></tr>
<tr><td>0101</td><td>GS1</td><td>GS1</td></tr>
<tr><td>0110</td><td>GS1</td><td>GS2</td></tr>
<tr><td>0111</td><td>GS1</td><td>GS3</td></tr>
<tr><td>1000</td><td>GS2</td><td>GS0</td></tr>
<tr><td>1001</td><td>GS2</td><td>GS1</td></tr>
<tr><td>1010</td><td>GS2</td><td>GS2</td></tr>
<tr><td>1011</td><td>GS2</td><td>GS3</td></tr>
<tr><td>1100</td><td>GS3</td><td>GS0</td></tr>
<tr><td>1101</td><td>GS3</td><td>GS1</td></tr>
<tr><td>1110</td><td>GS3</td><td>GS2</td></tr>
<tr><td>1111</td><td>GS3</td><td>GS3</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update</td><td>Display Update Sequence Option:</td></tr>
</table>

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control 2	Enable the stage for Master Activation Parameter (in Hex) Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then INIITIAL DISPLAY Then PATTERN DISPLAY Then Disable CP Then Disable OSC — FF [POR] Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then PATTERN DISPLAY Then Disable CP Then Disable OSC — F7 To Enable Clock Signal (CLKEN=1) — 80 To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1) — C0 To INITIAL DISPLAY + PATTEN DISPLAY — 0C To INITIAL DISPLAY — 08 To DISPLAY PATTEN — 04 To Disable CP, then Disable Clock Signal (CLKEN=1, CPEN=1) — 03 To Disable Clock Signal (CLKEN=1) — 01 Remark: CLKEN=1: If CLS=VDDIO then Enable OSC If CLS=VSS then Enable External Clock CLKEN=0: If CLS=VDDIO then Disable OSC AND INTERNAL CLOCK Signal = VSS,
0	0	23	0	0	1	0	0	0	1	1	Reserve	
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	25	0	0	1	0	0	1	0	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly.
0	0	26	0	0	1	0	0	1	1	0	Reserve	
0	0	27	0	0	1	0	0	1	1	1	Reserve	

Fundamental Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds 0x09(10Seconds) [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2B	0	0	1	0	1	0	1	1	Reserve	
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2D	0	0	1	0	1	1	0	1	Read OTP Registers	Read register reading to MCU A [7:0] Spare OTP Option B [7:0] VCOM Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	2E	0	0	1	0	1	1	1	0	Reserve	
0	0	2F	0	0	1	0	1	1	1	1	Reserve	
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	31	0	0	1	1	0	0	0	1	Reserve	
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [720 bits]
0 0 0 ... 0 0	1 1 1 ... 1 1		LUT [90 bytes]									
0	0	33	0	0	1	1	0	0	1	1	Read LUT register	Read from LUT register (excluding temperature data) [720 bits]
1 1 1 ... 1 1	1 1 1 ... 1 1		LUT [90 bytes]									
0	0	34	0	0	1	1	0	1	0	0	Reserve	
0	0	35	0	0	1	1	0	1	0	1	Reserve	
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R36h]
0	0	37	0	0	1	1	0	1	1	1	OTP selection	Write the OTP Selection:

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	A[7]=1 spare VCOM OTP A[6] VCOM_Status A[5]=1 spare WS OTP A[4] WS_Status A3:A0 are reserved OTP bit. User can treat the bits as Version Control.
0	0	38	0	0	1	1	1	0	0	0	Reserve	
0	0	39	0	0	1	1	1	0	0	1	Reserve	
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0]: Number of dummy line period in term of TGate 4 [POR] Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] Line width in us 0000 60 0001 64 0010 68 0011 72 0100 78 0101 84 0110 90 0111 98 1000 108 [POR] 1001 120 1010 136 1011 154 1100 180 1101 216 1110 272 1111 362 Remark: Default value will give 50Hz Frame frequency under 4 dummy line pulse setting.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform	Select border waveform for VBD

Fundamental Command Table

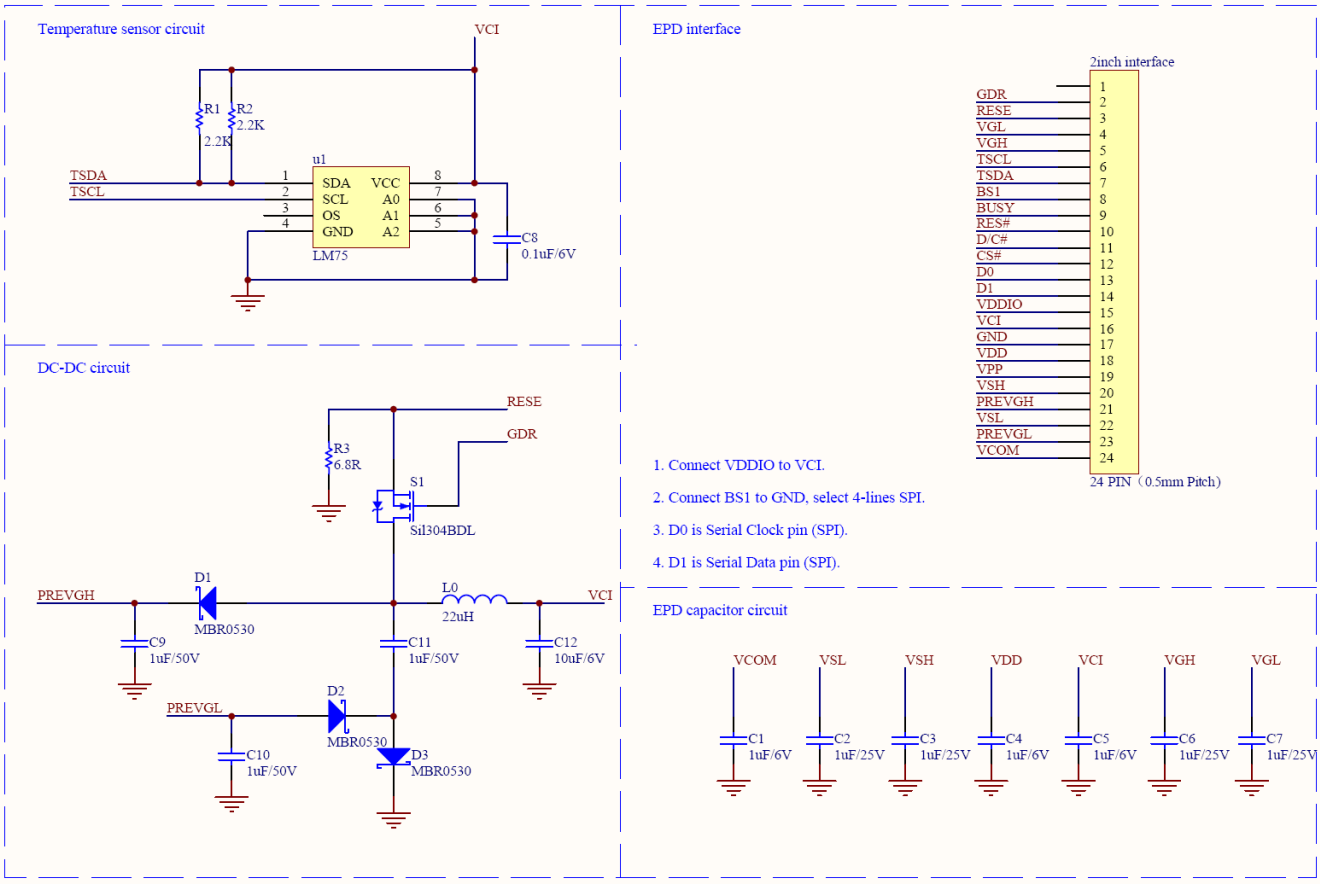
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD 00 VSS 01 VSH 10 VSL 11[POR] HiZ A [3:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) 0000 GS0 GS0 0001 GS0 GS1 0010 GS0 GS2 0011 [POR] GS0 GS3 0100 GS1 GS0 0101 GS1 GS1 0110 GS1 GS2 0111 GS1 GS3 1000 GS2 GS0 1001 GS2 GS1 1010 GS2 GS2 1011 GS2 GS3 1100 GS3 GS0 1101 GS3 GS1 1110 GS3 GS2 1111 GS3 GS3
0	0	3D	0	0	1	1	1	1	0	1	Reserve	
0	0	3E	0	0	1	1	1	1	1	0	Reserve	
0	0	3F	0	0	1	1	1	1	1	1	Reserve	
0	0	40	0	1	0	0	0	0	0	0	Reserve	
0	0	41	0	1	0	0	0	0	0	1	Reserve	
0	0	42	0	1	0	0	0	0	1	0	Reserve	
0	0	43	0	1	0	0	0	0	1	1	Reserve	
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		address unit A[7:0]: XStart, POR = 00h B[7:0]: XEnd, POR = 1Fh
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: YStart, POR = 00h B[7:0]: YEnd, POR = B3h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	46	0	1	0	0	0	1	1	0	Reserve	
0	0	47	0	1	0	0	0	1	1	1	Reserve	
0	0	48	0	1	0	0	1	0	0	0	Reserve	
0	0	49	0	1	0	0	1	0	0	1	Reserve	
0	0	4A	0	1	0	0	1	0	1	0	Reserve	
0	0	4B	0	1	0	0	1	0	1	1	Reserve	
0	0	4C	0	1	0	0	1	1	0	0	Reserve	
0	0	4D	0	1	0	0	1	1	0	1	Reserve	
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) POR is 0
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) POR is 0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	F0	1	1	1	1	0	0	0	0	Booster Feedback Selection	Set Booster Feedback selection 0x1F = Internal Feedback is used POR is 0x1F
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

5.5 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-	0.657	3.610	mW	-
Power consumption in standby mode	-	-	-	TBD	mW	-

5.6 Reference Circuit



6. Command Description

6.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		1	0	1	1	0	0	1	1
W	1						GD	SM	TB
POR							0	0	0

MUX[7:0]: Specify number of lines for the driver: MUX[7:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 180MUX.

GD: Selects the 1st output Gate This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed, Output pin assignment sequence is shown as below (for 180 MUX ratio):

	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW90
G1	ROW1	ROW0	ROW90	ROW0
G2	ROW2	ROW3	ROW1	ROW91
G3	ROW3	ROW2	ROW91	ROW1
:	:	:	:	:
G88	ROW88	ROW89	ROW44	ROW134
G89	ROW89	ROW88	ROW134	ROW44
G90	ROW90	ROW91	ROW45	ROW135
G91	ROW91	ROW90	ROW135	ROW45
:	:	:	:	:
G176	ROW176	ROW177	ROW88	ROW178
G177	ROW177	ROW176	ROW178	ROW88
G178	ROW178	ROW179	ROW89	ROW179
G179	ROW179	ROW178	ROW179	ROW89

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB=0) or from bottom to up (TB=1).

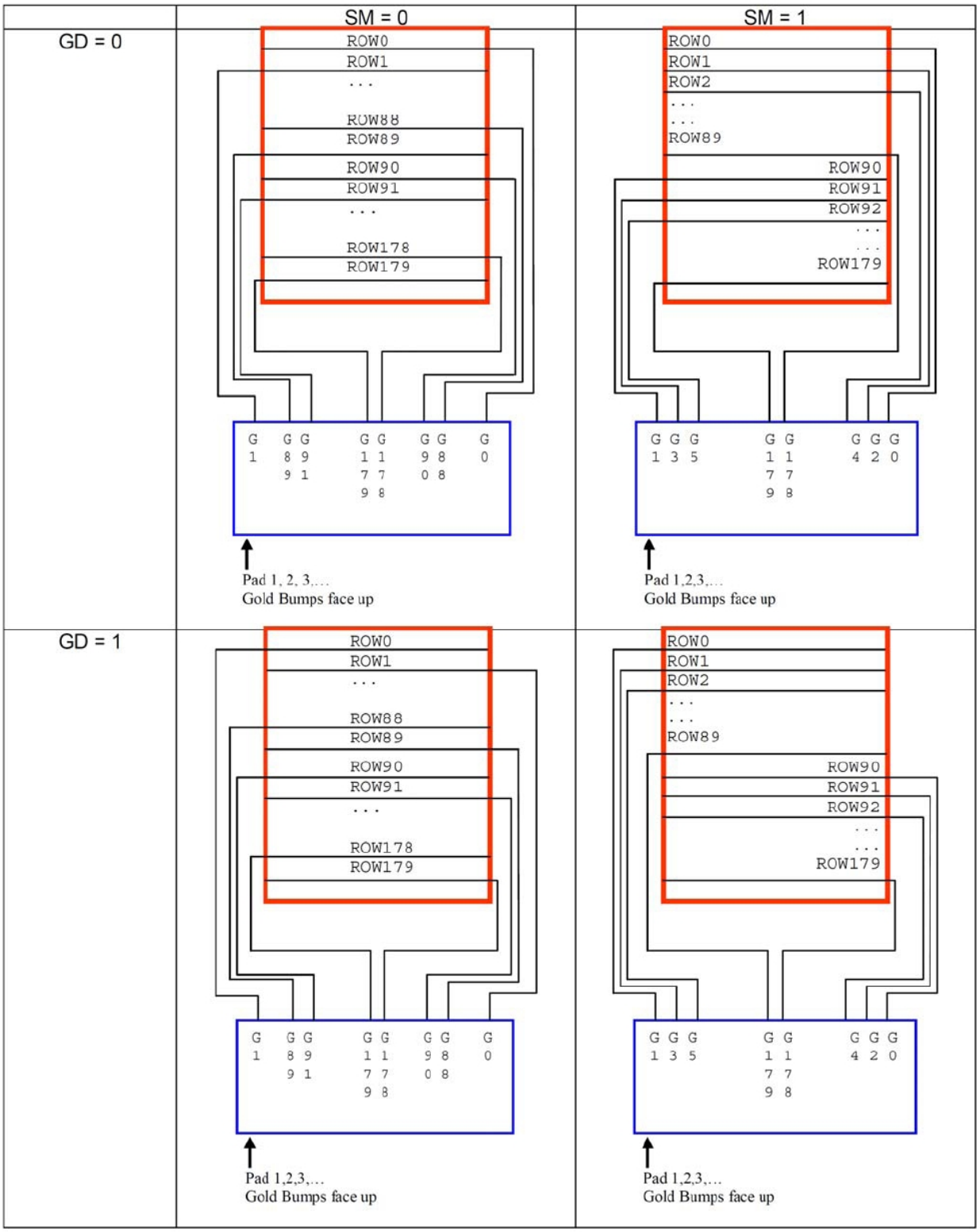


Figure: Output pin assignment on different Scan Mode Setting

6.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 179. Figure 8-2 shows an example using this command of this command when MUX ratio =180 and MUX ratio = 90. “ROW” means the graphic display data RAM row.

	MUX ratio (01h) = 179	MUX ratio (01h) = 89	MUX ratio (01h) = 89
GATE Pin	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 45
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G43	:	:	-
G44	:	:	-
G45	:	:	ROW45
G46	:	:	ROW46
:	:	:	:
:	:	:	:
G88	ROW88	ROW88	:
G89	ROW89	ROW89	:
G90	ROW90	-	:
G91	ROW91	-	:
:	:	:	:
:	:	:	:
G133	:	:	ROW133
G134	:	:	ROW134
G135	:	:	-
G136	:	:	-
:	:	:	:
:	:	:	:
G176	ROW176	-	-
G177	ROW177	-	-
G178	ROW178	-	-
G179	ROW179	-	-

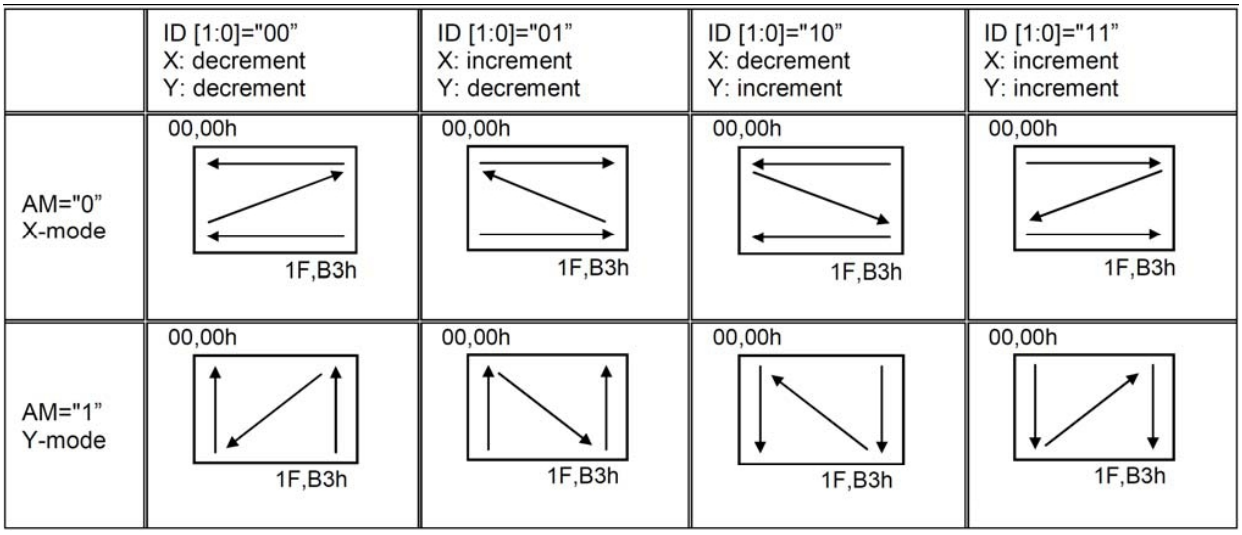
6.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

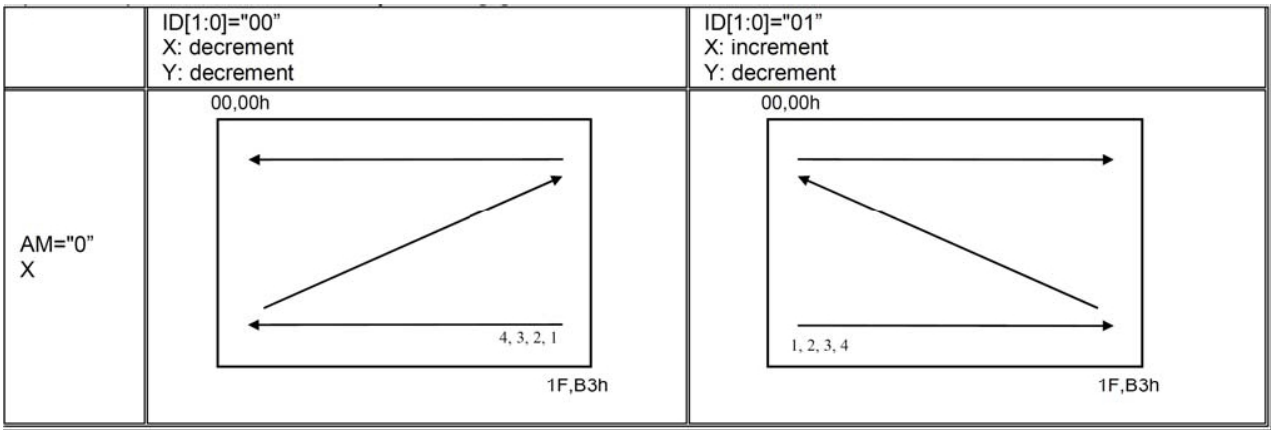
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	0	0

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the RAM when ID[1:0] = "1". The address counter is automatically decremented by 1, after data are written to the RAM when ID[1:0] = "0". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the RAM is set with AM bits.

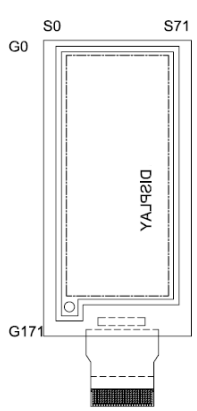
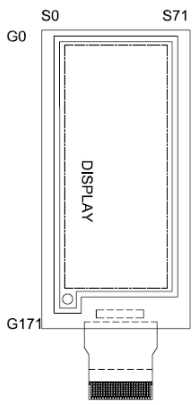
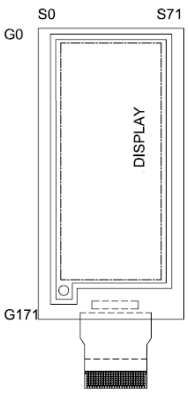
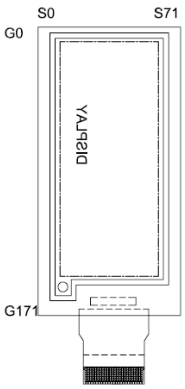
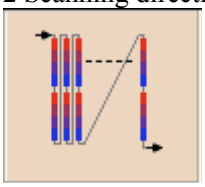
AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.



The pixel sequence are defined by the ID [0]



The totally image display style setting is shown as below table:

REG#	Style 1	Style 2	Style 3	Style 4
11h	0x03	0x02	0x01	0x00
44h	0x00	0x11	0x00	0x11
	0x11	0x00	0x11	0x00
45h	0x00	0x00	0xAB	.0xAB
	0xAB	0xAB	0x00	0x00
4Eh	0x00	0x11	0x00	0x11
4Fh	0x00	0x00	0xAB	0xAB
Image display sample				
Display data distilling format setting	1 Original image:  2 Scanning direction: vertical scan mode  3 Image display mode: Reversal display  4 The max. width :172 The max. height :72 5 Output gray: 4 gray			

6.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	1	1	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 4 times address unit. Data are written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write. It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 1Fh. The windows is followed by the control setting of Data Entry Setting (R11h).

6.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	1	0	1	0	0	1	1

YSA[7:0]/YEA[7:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data are written to the RAM within the area determined by the addresses specified by YSA [7:0] and YEA [7:0]. These addresses must be set before the RAM write. It allows YEA [7:0] ≤ YSA [7:0]. The settings follow the condition on 00h ≤ YSA [7:0], YEA [7:0] ≤ B3h. The windows is followed by the control setting of Data Entry Setting (R11h).

6.6 Set RAM Address Counter (4Eh-4Fh)

REG#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).

YAD[7:0]: Make initial settings for the RAM Y address in the address counter (AC).

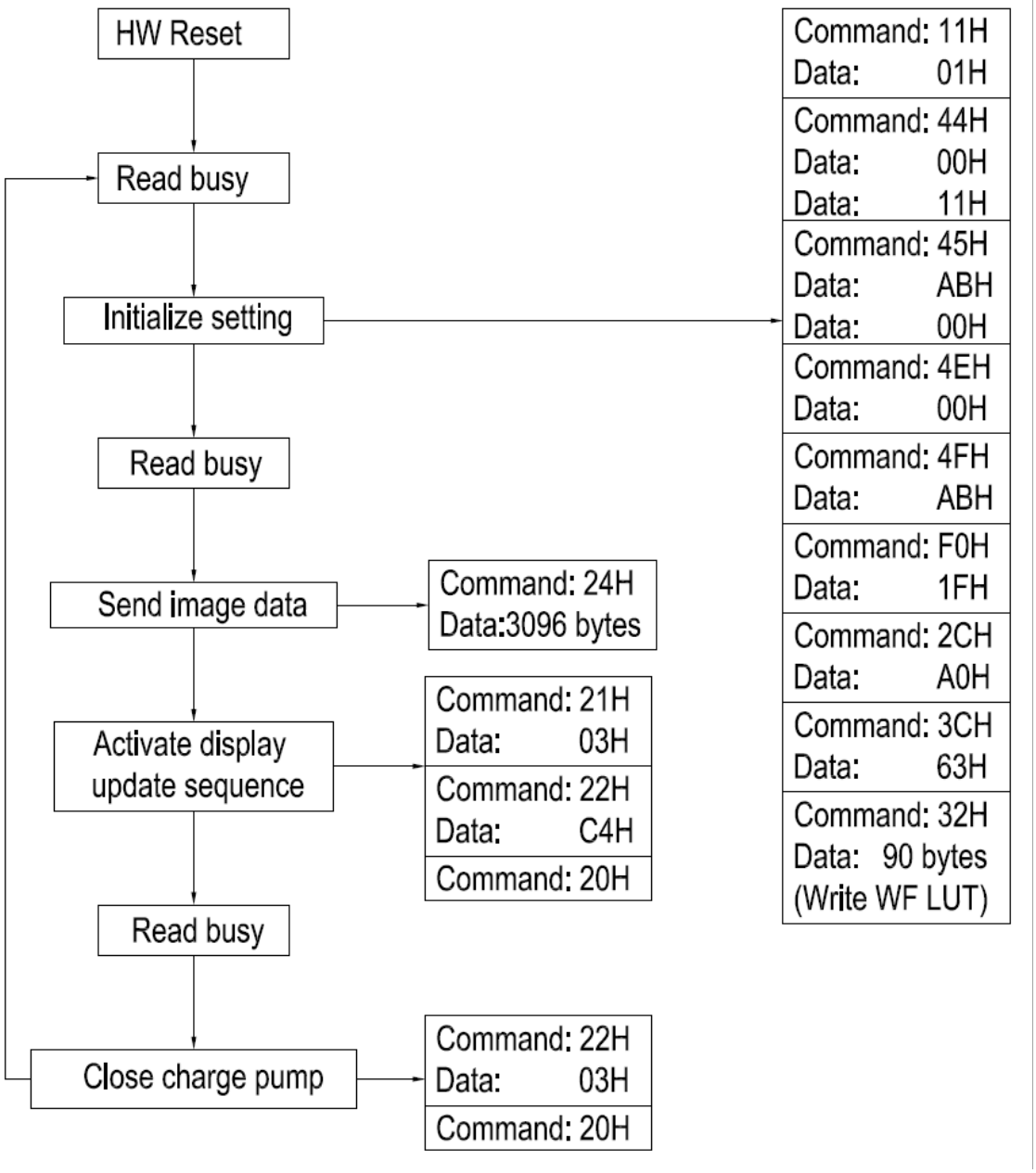
After RAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new RAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AD, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

7. Typical Operating Sequence

7.1 Normal Display

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	HW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH / VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Select Border waveform	
4		-	Data operations	
	User	C 11	Command: Data Entry mode	
	User	C 44	Command: X RAM address start /end	
	User	C 45	Command: Y RAM address start /end	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write display data to RAM	
			Ram Content for Display	
5	User	C F0 D 1F	Command: Set Internal Feedback Selection	
6	User	C 20	Command: Display update	
	IC	-	Booster and regulators turn on	
	IC	-	Load temperature register with sensor reading	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
7	User	-	IC power off	

7.2 The Normal Flow Chart for Display One Screen (WF LUT Mode)



7.3 Waveform Setting OTP Program

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
4	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
5	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
6	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait BUSY = L	
7	User	C 36	Program OTP selection register	
	User	-	Wait BUSY = L	
8	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT (11 entries + Temperature range) must be written at the same time	
	User	C 4E D 00 C 4F D 00	Command: Initial Ram address counter	
9	User	C 30	Waveform Setting OTP programming	
	IC	-	BUSY pin pull H	
	IC	-	Check the OTP Selection	
	IC	-	IC control OTP programming time, and transfer data to selected OTP	
	IC	-	BUSY pin pull L	
	User	-	Wait BUSY = L	
10	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait BUSY = L	
11	User		IC power off	

7.4 VCOM OTP Program

Sequence	Action by	Command	Action description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
3	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
4	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
5	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait until BUSY = L	
6	User	C 36	Program OTP selection register	
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
7		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Panel configuration (MUX, Source, Gate scanning direction)	
	User	C 03	Command: VGH / VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C F0 D 1F	Command: Set Internal Feedback Selection	
	User	C 32	VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Booster on and High voltage ready	
	User	-	Wait until BUSY = L	
8	User	C 28	Command: Enter VCOM sensing mode	
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	Wait for 10s	According to R29h
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	

9	User	C 22 D 02 C 20	Command: Booster and High voltage disable	
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: VCOM OTP program	
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

OTP Selection bit:

Set on R37h, and read from R2Dh, A[7:6] used for VCOM and A[5:4] used for OTP

A[7:6] / [5:4]	**Description**
00	It indicates fresh device, OTP read and program would be made on Default OTP set. User required setting and programming the bits into 01.
01	It indicates default OTP programmed device, OTP read would be made on Default OTP set. User require setting and programming the bits into 11.
11	It indicates SPARE OTP programmed device, only OTP read would be made on SPARE OTP set. User should stop the OTP programming if 11 is found at OTP checking stage.

8. Optical characteristics

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

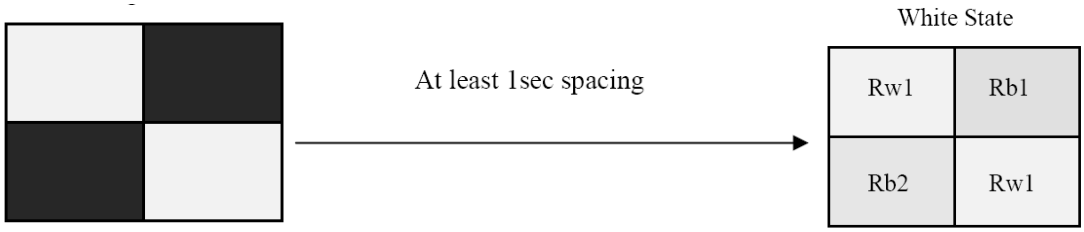
Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		7:1	8:1	-	-	11-2
Tupdate	Image update time	at 25 °C	-	1800	-	ms	-
Ghosting	Image sticking		-2.0	1.0	2.0	-	11-3

Notes: 1. Luminance meter: Eye-One Pro Spectrophotometer.

2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3. Ghosting Testing:

3-1. Testing Pattern



3-2. Refresh process：Init ---- GC White ---- 4 checkerboard Pattern GC ---- GC White.

3-3. Measuring the reflectance of all 4 checkerboard areas when final white state by Eye-one device.

3-4. Rw: reflectance of area transited from white state

Rb: reflectance of area transited from dark (black) state

3-5. Calculating averages of WS-to-WS and DS-to-WS transitions:

Rw(ave)=(Rw1+Rw2)/2，Rb(ave)=(Rb1+Rb2)/2，G=Rw(ave)-Rb(ave).

9 Appearance Inspection Standard

9.1 Major Defects

Defect Type	Description
No display	Not able to display any image
Line defect	Complete line(s) missing or unusual appear when display
Abnormal display	Unusual pattern or function when display

9.2 Minor Defects

Environmental condition		Temperature / Humidity	Environmental iliumination	Distance	Time	Angle
		20°C -25°C 40%RH-55%RH	700-1000Lux	200-300mm	20 sec	Up/down 30 degree (Rotation)
appearance Inspection standard	NO.	Defect type	Check	Acceptable	A Zone	B Zone
	1	Spot (B/W spot, dent in glass or protection sheet , foreign mat. Swell. Dot defect) (unwork)	By eye and gauge	D≦0.2mm	Ignore	OK
				0.2mm<D≦0.3mm	≦4（two spot spacing greater than 20mm）	
				0.3mm<D≦0.35mm	N≦1	
				D>0.35mm	NG	
	2	Scratch or line defect (scratch or foreign mat. Protection sheet) (unwork)	By eye and gauge	L≦0.5mm & W≦0.2mm	Ignore	
				0.5 mm< L≦ 3mm & 0.2mm<W≦0.3mm	≦2（the center of two line spacing greater than 30mm）	
				L>3.0mm or W>0.3mm	NG	
	3	Air bubble	By eye and gauge	D1/D2≦0.2mm	Ignore	
				0.2mm<D1/D2≦0.5mm	N≦3	
				D1/D2>0.5mm	NG	
	4	Stab	By eye	No hurt PET	NG	

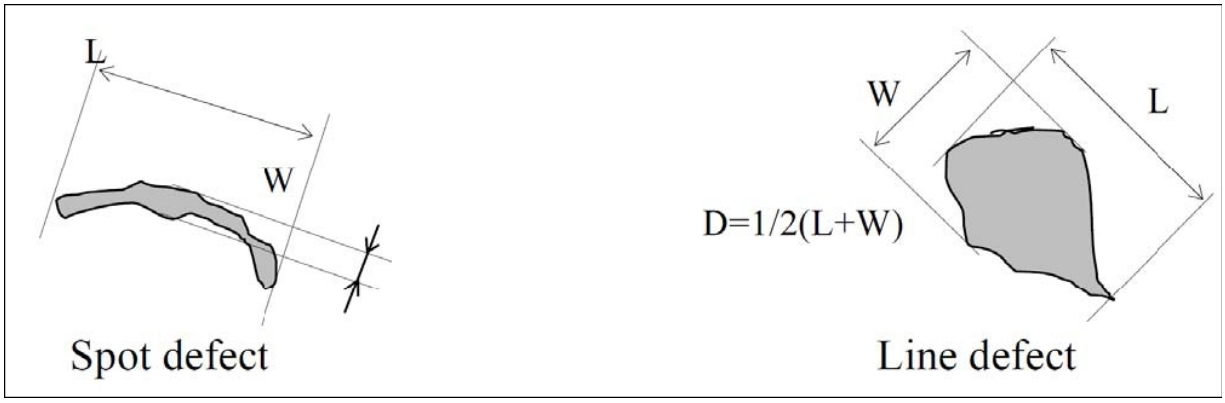
Note: 1. Spot size is based on microscope 10x~100x

2. Spot define: That only can be seen under WS, BS or GS defects.

3. A Zone: Active area(defined in specification)

B Zone: Border area from A Zone edge

9.3 Spot and Line Defect Test and Calculation



9.4 Spot and Line Test Standard

When L≦0.5mm, test as point.

When L< 4W, test as point.

9.5 Air Bubble Defect Test and Calculation

10. Handling, safety and environmental requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

11. Reliability test

	Test	Condition	method	Remark
1	High-Temperature Operation	T = 50℃,30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70℃, 23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40℃,RH=90%for168hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60℃,RH=80%for240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→ +70℃,100 cycles 30mins 30mins Test in white pattern	IEC 60 068-2-14	
8	UV exposure Resistance	765 W/m2 for 1688 hrs,40℃	IEC 60 068-2-5 Sa	
9	Electrostatic Effect (non-operating)	Machine mode +/- 250V, 0Ω,200pF	IEC62179, IEC62180	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: The protective film must be removed before temperature test.