

Display Elektronik GmbH

DATA SHEET

*TFT MODULE*

**DEM 080160A VMH-PW-N**

**0,96“ TFT**

Product Specification

Ver.: 6

19.05.2022

**Revision History**

<b>VERSION</b>	<b>DATE</b>	<b>REVISED PAGE NO.</b>	<b>Note</b>
0	25.06.2018		First Issue
1	19.09.2018		Modify Contour Drawing
2	16.07.2019		Modify Backlight
3	10.04.2020		Add Power ON/OFF Sequence & Reset Timing & Initial Code Modify Electrical Characteristics & Color Chromaticity
4	06.08.2020		Add Inspection Specification
5	15.07.2021		Correct Initial Code for Reference
6	19.05.2022		Modify Contour Drawing



# Contents

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2. General Specification
3. Interface
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## **1. Summary**

DEM 080160A VMH-PW-N is a color active matrix thin film transistor (TFT) liquid crystal empty cell. This model is composed of amorphous silicon TFT as a switching device. It is a transmissive IPS type display operating in the normally black mode.

This TFT LCD has a 0.96-inch diagonally measured active display area with 80 x 160 dot (80 horizontal by 160 vertical pixel) resolution. Each pixel is divided into Red, Green, Blue dots which are arranged in vertical stripes.

## **2. General Specifications**

- n Size: 0.96 Inch
- n Dot Matrix: 80 x RGB x 160 Dots
- n Module Dimension: 13.50 x 27.95 x 1.54 mm
- n Active Area: 10.80 x 21.70 mm
- n Dot Pitch: 0.135 x 0.1356 mm
- n LCD Type: TFT, IPS, Normally Black, Transmissive
- n Viewing Angle: Full View, 80°/80°/80°/80°
- n Aspect Ratio: 1:2
- n IC: ST7735S (Sitronix)
- n Interface: SPI
- n Backlight Type: LED, Normally White
- n With /Without TP: No Touch
- n Surface: Glare

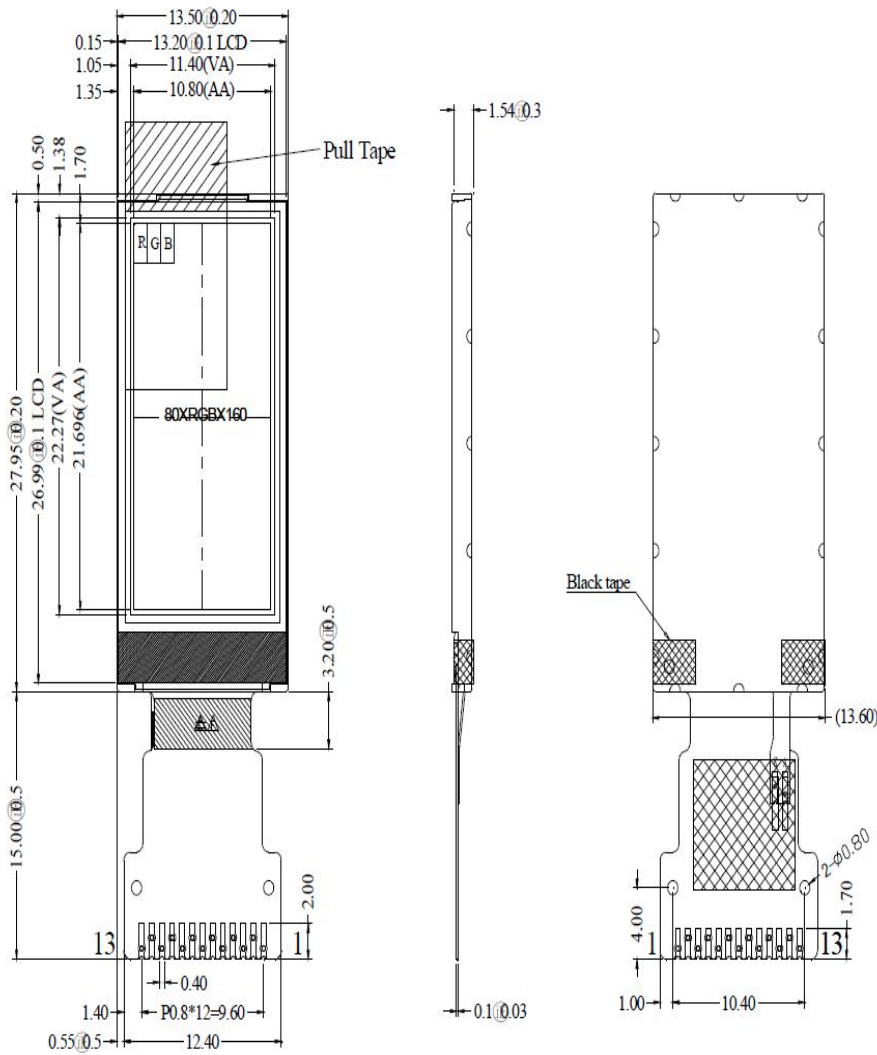
\*Color tone slight changed by temperature and driving voltage.

### 3. Interface

#### 3.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1	SPI4W	SPI4W='0', 3-wire SPI. SPI4W='1', 4-wire SPI.	-
2	NC	No Connection	-
3	SDA	Serial Interface Data	-
4	SCL	Serial Interface Clock	-
5	RS	Data/Command Selection Pin (4-Wire SPI use)	-
6	RES	Reset Pin (Low Active)	-
7	CS	Chip Selection Pin (Low Active)	-
8	GND	Ground	-
9	NC	No Connection	-
10	VCC	Power Supply.	-
11	LEDK	Backlight Cathode	-
12	LEDA	Backlight Anode	-
13	GND	Ground	-

### 4. Counter Drawing



PIN NO.	SYMBOL
1	SPI4W
2	NC
3	SDA
4	SCL
5	RS
6	RES
7	CS
8	GND
9	NC
10	VCC
11	LEDK
12	LEDA
13	GND

The non-specified tolerance of dimension is ±0.3 mm.

Note: FPC for soldering.

## **5. Absolute Maximum Ratings**

<b>Item</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Operating Temperature	T <sub>OP</sub>	-20	-	+70	°C
Storage Temperature	T <sub>ST</sub>	-30	-	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

1. Temp. □60°C, 90% RH MAX. Temp. > 60°C,  
Absolute humidity shall be less than 90% RH at 60°C.



## 6. Electrical Characteristics

### 6.1. Operating conditions:

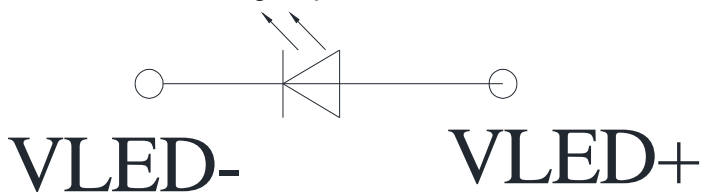
Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply LCM Current	ICC	-	-	2	mA

Note: To avoid power supply noise, please avoid using driving conditions close to min. or max. value.

### 6.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I <sub>LED</sub>	-	20	-	mA	
LED Voltage	V <sub>LED</sub>	2.8	3.0	3.3	V	Note 1
LED Lifetime (25°C)		-	50000	-	Hr	Note 2,3,4

Note 1: There are 1 groups LED



## Circuit diagram

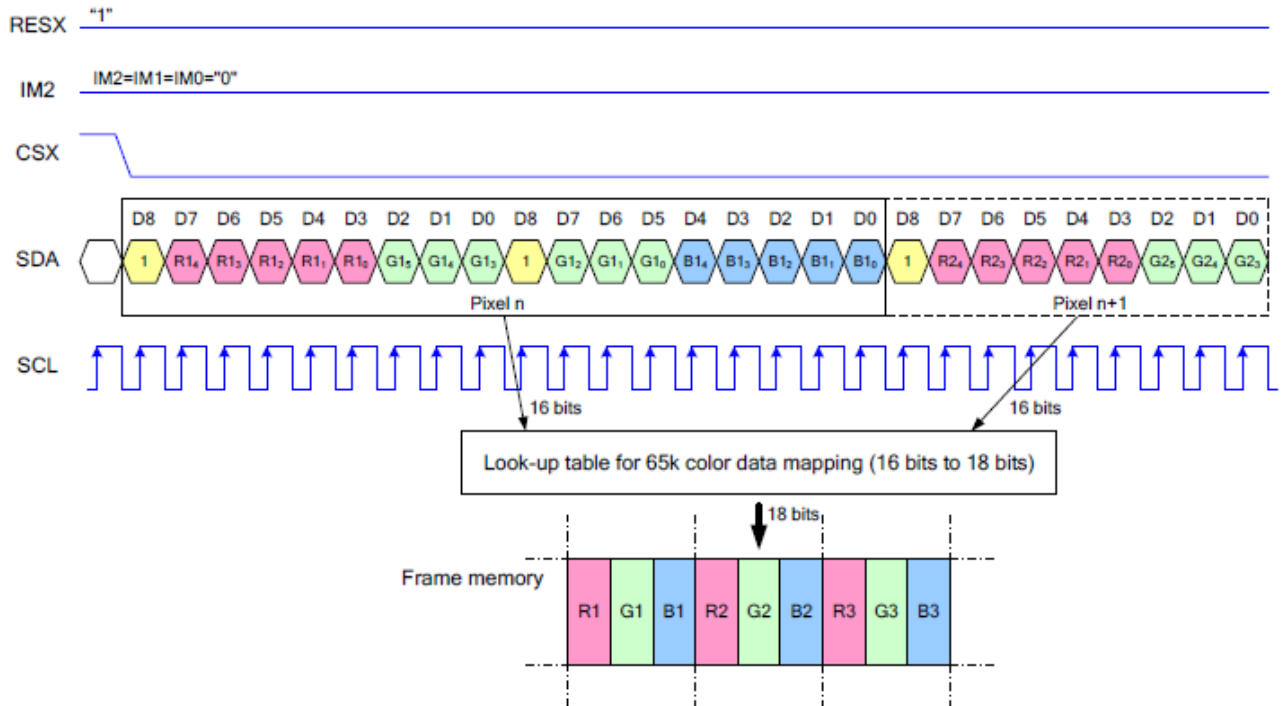
Note 2: Ta = 25°C

Note 3: Brightness to be decreased to 50% of the initial value

Note 4: The single LED lamp case

# 7. Data Color Coding

## 7.1. 3-Wire SPI Mode: RGB 5-6-5-Bit Input, 65k-Colors, 3AH="05h"

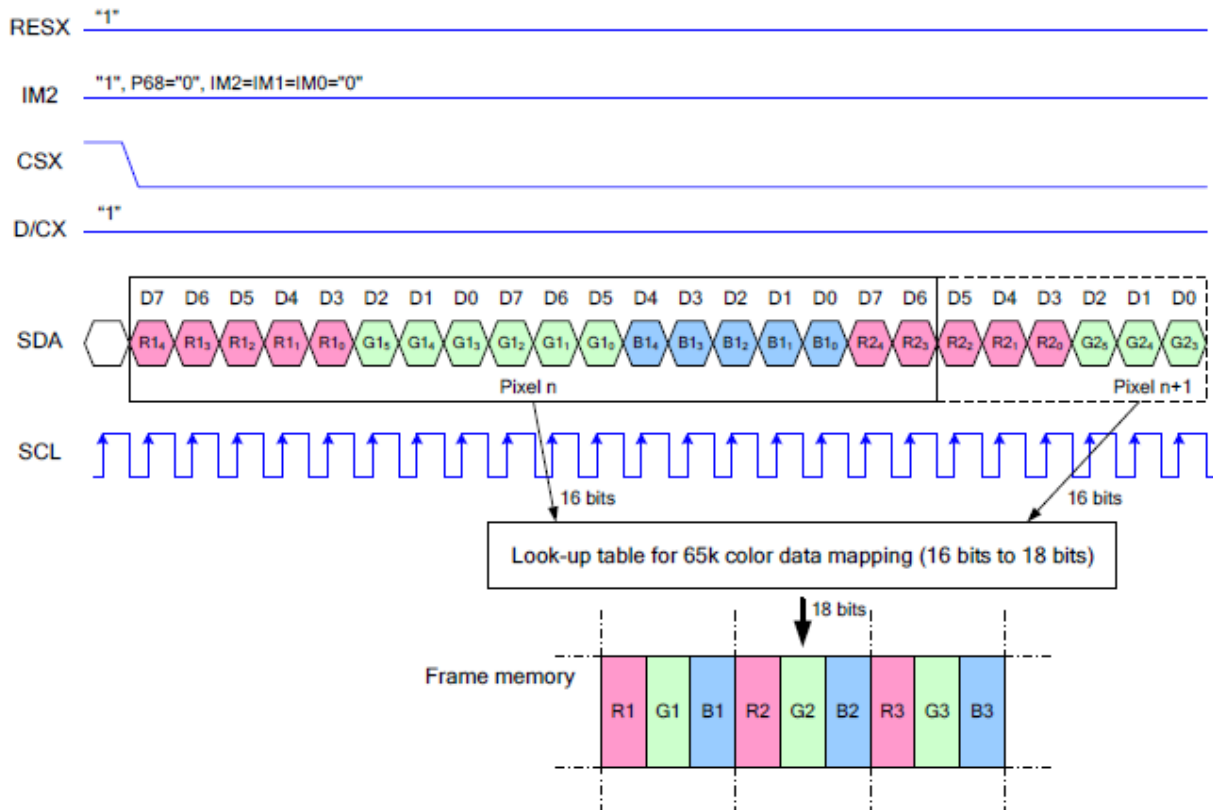


Note 1: Pixel Data with the 16-Bit Color Depth Information

Note 2: The most significant Bits are: Rx4, Gx5 and Bx4

Note 3: The least significant Bits are: Rx0, Gx0 and Bx0

7.2. 4-Wire SPI Mode: RGB 5-6-5-Bit Input, 65k-Colors, 3AH="05h"

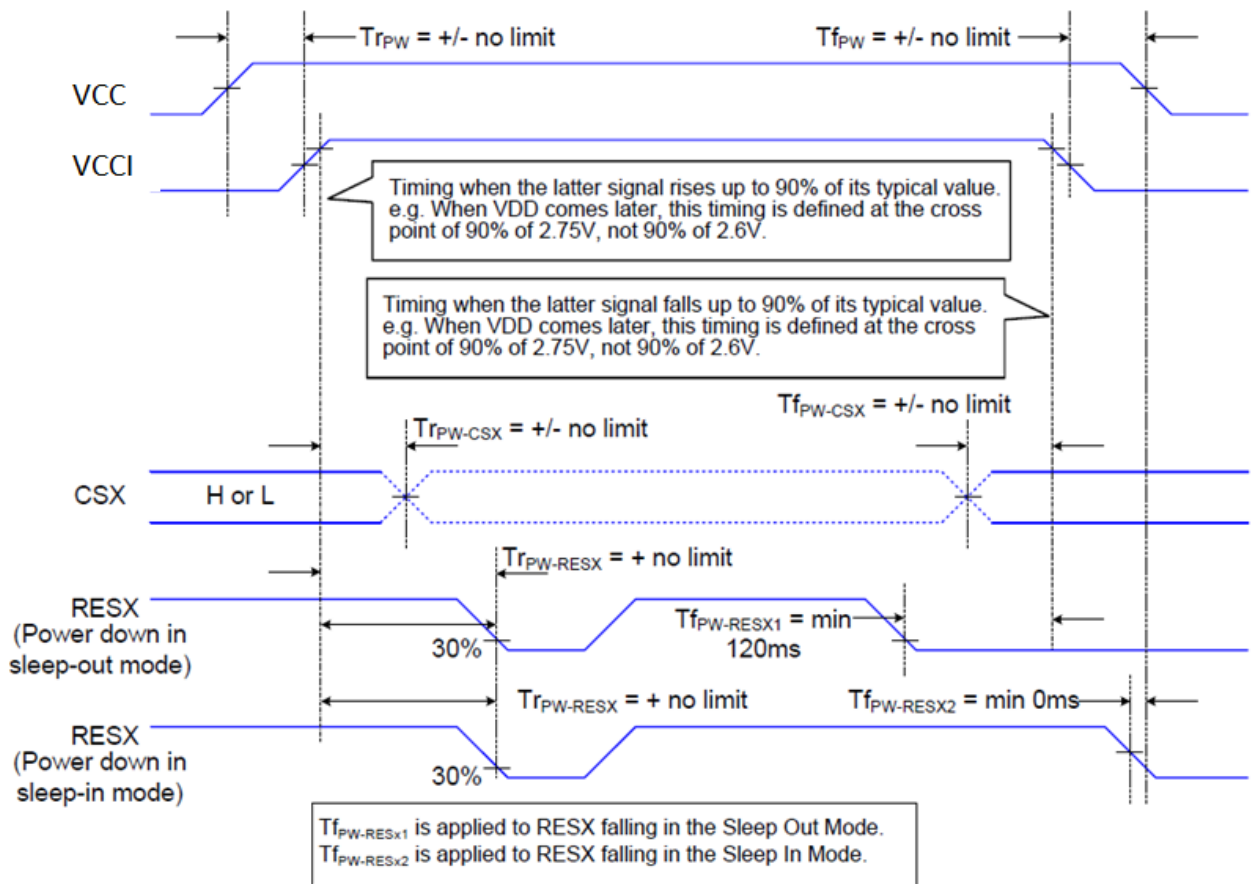


Note 1. Pixel Data with the 16-Bit Color Depth Information

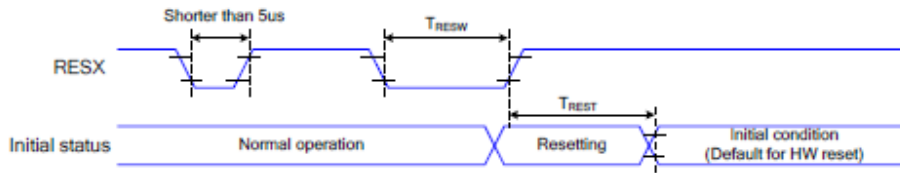
Note 2. The most significant Bits are: Rx4, Gx5 and Bx4

Note 3. The least significant Bits are: Rx0, Gx0 and Bx0

## 8. Power ON/OFF Sequence



## 9. Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5	ms
				120	ms

Table 14 Reset Timing

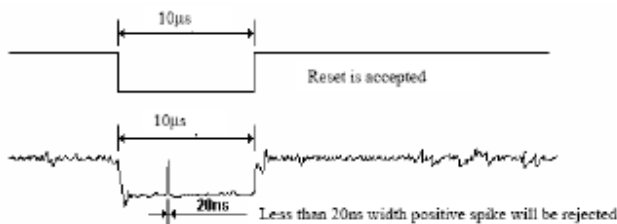
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

### 10. Optical Characteristics

Item	Symbol	Condition.	Min	Typ.	Max.	Unit	Remark	
Response Time	Tr	$\theta=0^\circ, \phi=0^\circ$	-	30	40	.ms	Note 3	
	Tf							
Contrast Ratio	CR	At optimized viewing angle	-	800	-	-	Note 4	
Color Chromaticity	White	Wx	$\theta=0^\circ, \phi=0$	0.255	0.305	0.355	Note 2,6,7	
		Wy		0.275	0.325	0.375		
Viewing Angle	Hor.	$\Theta_R$	$CR \geq 10$	-	80	-	Deg.	Note 1
		$\Theta_L$		-	80	-		
	Ver.	$\Phi_T$		-	80	-		
		$\Phi_B$		-	80	-		
Brightness	-	-	400	500	-	cd/m <sup>2</sup>	Center of display	
Uniformity	(U)	-	75	-	-	%	Note 5	

Ta=25±2°C

Note 1: Definition of viewing angle range

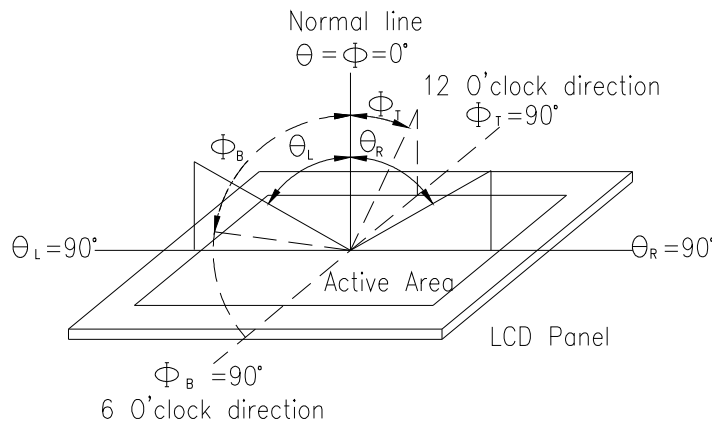


Fig.10.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

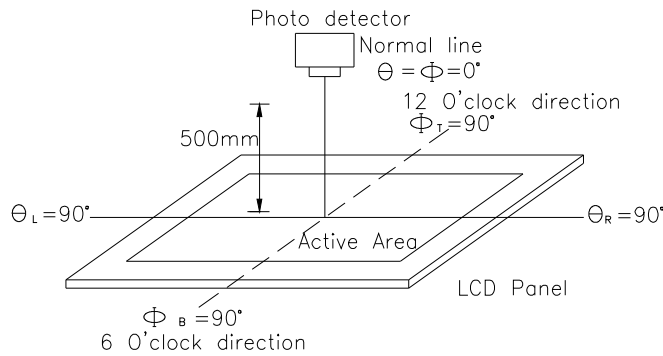
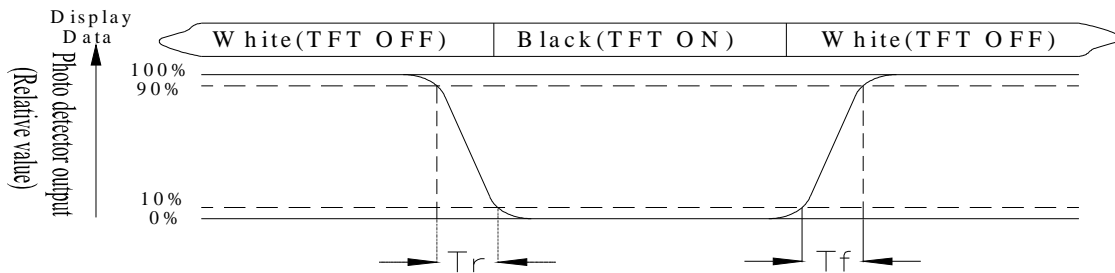


Fig. 10.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time,  $T_r$ , is the time between photo detector output intensity changed from 90% to 10%. And fall time,  $T_f$ , is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

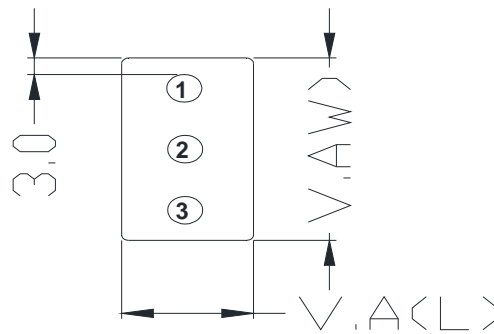
**Note 5: Definition of Luminance Uniformity**

Active area is divided into 3 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) =  $L_{min}/L_{max} \times 100\%$

L = Active area length

W = Active area width



**Fig10.3. Definition of uniformity**

**Note 6: Definition of color chromaticity (CIE 1931)**

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



# 11. Reliability

Content of Reliability Test (Wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature Storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1 ,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1 ,2
Thermal shock Resistance	The sample should be allowed stand the following 10 cycles of operation  <div style="text-align: center;"> <p style="margin: 0;">-20°C      25°C      70°C</p> <p style="margin: 0;">30min    5min    30min</p> <p style="margin: 0;">1 cycle</p> </div>	-20°C/70°C 10 cycles	—
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static Electricity Test	Endurance test applying the electric stress to the terminal.	VS=±600V(con tact),±800v(air), RS=330Ω CS=150pF 10 times	—

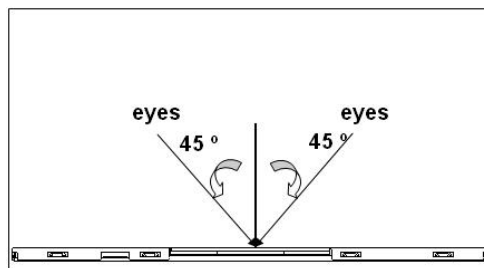
Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

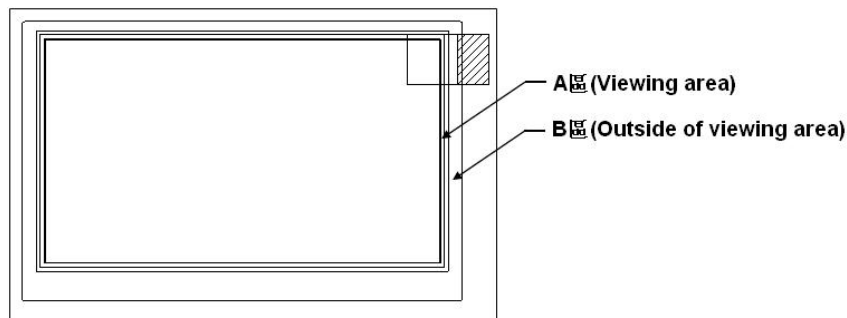
Note3: The packing have to including into the vibration testing.

## 12. Inspection Specification

1. Scope : TFT-LCD (The document shall be applied to TFT-LCD Module)
2. Inspection Standard : MIL-STD-105EII(MIL-STD-105E Table Normal Inspection Single Sampling Level II)
3. Defect Level : AQL : 0.65; AQL : 2.5(Major Defect AQL:0.65;Minor Defect AQL:2.5)
4. Test conditions:
  - (1) Temperature : 15°C~25°C ; (Humidity) : 55 ±15%
  - (2) Visual inspection : 500 Lux : 20cm~30cm (Illumination : More than 500 Lux; Inspection Distance: 20cm~30cm)
  - (3) Electrical inspection : 100Lux~300Lux ; 20cm~30cm(Illumination : 100Lux~300Lux; Inspection Distance: 20cm~30cm)
  - (4) Visual angle : 45 °(The test direction is base on about around 45° of Vertical line )



- (5) Definition of area:



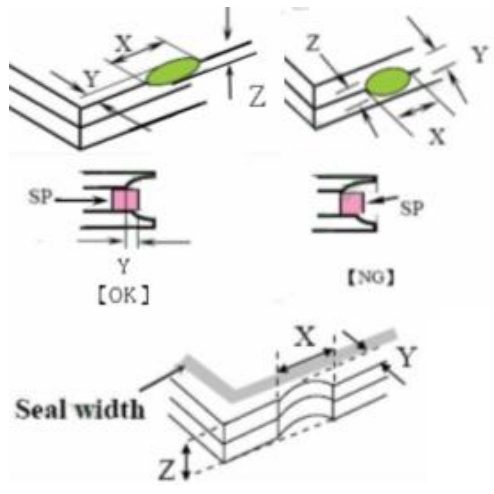
5. Pixel Definition:

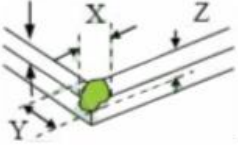
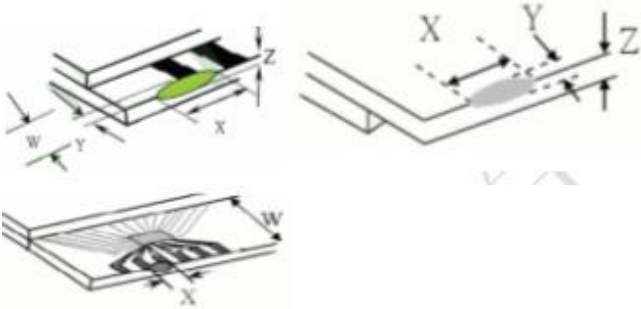
R	G	B	R	G	B	R	G	B		Dot Defect
R	G	B	R	G	B	R	G	B		Adjacent Dot Defect
R	G	B	R	G	B	R	G	B		Cluster

Note 1: If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as 1 defect.

Note 2: There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

5. Inspection Standard :

No	Inspection Item	Inspection Standard	Defect Level
1	Packing & Indicate	1.1. Mixed product types. 1.2. The part number is inconsistent with work order of production. 1.3. Assembled in inverse direction. 1.4. The quantity is inconsistent with work order of production.	Maj
2	Size	Product size and structure must meet the structure diagram	Maj
3	The crack of Glass	<p>Symbols:                      X:Symbols                      Y:The width of crack.                      Z:The thickness of crack.                      W:Terminal length                      T:The thickness of glass.                      a:LCD LCD side length.</p> <p>3.1.— General glass chip:                      3.1.1.Chip on panel surface and crack between panels;</p> 	Min

		<table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td><math>\leq a</math></td> <td>VA Crack can't enter viewing area</td> <td><math>\leq 1/2t</math></td> </tr> <tr> <td><math>\leq a</math></td> <td>SP – Crack can't exceed the half of SP width</td> <td><math>1/2t &lt; Z \leq 2t</math></td> </tr> </table> <p>3.1.2.邊角破損(Corner crack) :</p> 	X	Y	Z	$\leq a$	VA Crack can't enter viewing area	$\leq 1/2t$	$\leq a$	SP – Crack can't exceed the half of SP width	$1/2t < Z \leq 2t$													
X	Y	Z																						
$\leq a$	VA Crack can't enter viewing area	$\leq 1/2t$																						
$\leq a$	SP – Crack can't exceed the half of SP width	$1/2t < Z \leq 2t$																						
No	Inspection Item	Inspection Standard	Defect Level																					
3	The crack of Glass	<table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td><math>\leq 1/5a</math></td> <td>Crack can't enter viewing area</td> <td><math>\leq 1/2t</math></td> </tr> <tr> <td><math>\leq 1/5a</math></td> <td>SP – Crack can't exceed the half of SP width</td> <td><math>1/2t &lt; Z \leq 2t</math></td> </tr> </table> <p>3.2.Protrusion over terminal: 3.2.1.Chip on electrode pad:</p>  <table border="1"> <thead> <tr> <th>Position</th> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>Front</td> <td><math>\leq a</math></td> <td><math>\leq 1/2W</math></td> <td><math>\leq t</math></td> </tr> <tr> <td>Back</td> <td><math>\leq a</math></td> <td><math>\leq W</math></td> <td><math>\leq 1/2t</math></td> </tr> </tbody> </table>	X	Y	Z	$\leq 1/5a$	Crack can't enter viewing area	$\leq 1/2t$	$\leq 1/5a$	SP – Crack can't exceed the half of SP width	$1/2t < Z \leq 2t$	Position	X	Y	Z	Front	$\leq a$	$\leq 1/2W$	$\leq t$	Back	$\leq a$	$\leq W$	$\leq 1/2t$	Min
X	Y	Z																						
$\leq 1/5a$	Crack can't enter viewing area	$\leq 1/2t$																						
$\leq 1/5a$	SP – Crack can't exceed the half of SP width	$1/2t < Z \leq 2t$																						
Position	X	Y	Z																					
Front	$\leq a$	$\leq 1/2W$	$\leq t$																					
Back	$\leq a$	$\leq W$	$\leq 1/2t$																					

3.2.2.Non-conductive portion:

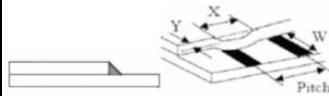


X	Y	Z
$\leq 1/3a$	$\leq W$	$\leq t$

Note:

ITO ITO 1/3 , If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

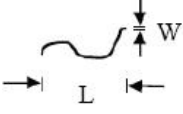
3.2.3.Glass remain:

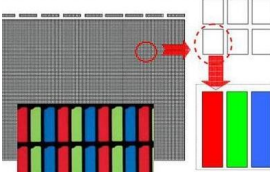


X	Y	Z
$\leq a$	$\leq 1/3W$	$\leq t$

No	Inspection item	Inspection Standard	Defect Level
----	-----------------	---------------------	--------------

4	Black or white dot Round type 	4.1 Round type(Non-display or display):	Min							
		<table border="1"> <thead> <tr> <th>Size</th> <th>Judging standard</th> <th>Acceptance(Q'ty)</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0.96"</td> <td><math>D \leq 0.1 \text{ mm}</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.10\text{mm} &lt; D \leq 0.4\text{mm}</math></td> <td><math>N \leq 3</math></td> </tr> <tr> <td><math>D &gt; 0.4\text{mm}</math></td> <td><math>N \leq 0</math></td> </tr> </tbody> </table> <p style="text-align: center;">distance <math>\geq 5\text{mm}</math></p>		Size	Judging standard	Acceptance(Q'ty)	0.96"	$D \leq 0.1 \text{ mm}$	Ignore	$0.10\text{mm} < D \leq 0.4\text{mm}$
Size	Judging standard	Acceptance(Q'ty)								
0.96"	$D \leq 0.1 \text{ mm}$	Ignore								
	$0.10\text{mm} < D \leq 0.4\text{mm}$	$N \leq 3$								
	$D > 0.4\text{mm}$	$N \leq 0$								

5	scratch、 contamination Line type 	5.1 Line type(Non-display or display):		Min													
		<table border="1"> <thead> <tr> <th>Size</th> <th colspan="2">Judging standard</th> <th>Acceptance(Q'ty)</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0.96"</td> <td>W</td> <td>L</td> <td rowspan="2">Ignore</td> </tr> <tr> <td><math>W \leq 0.03\text{mm}</math></td> <td>—</td> </tr> <tr> <td><math>0.03\text{mm} &lt; W \leq 0.05\text{mm}</math></td> <td><math>L \leq 5\text{mm}</math></td> <td><math>N \leq 4</math></td> </tr> <tr> <td><math>W &gt; 0.05\text{mm}</math></td> <td><math>L &gt; 5\text{mm}</math></td> <td><math>N \leq 0</math></td> </tr> </tbody> </table> <p style="text-align: center;">distance <math>\geq 5\text{mm}</math></p>	Size		Judging standard		Acceptance(Q'ty)	0.96"	W	L	Ignore	$W \leq 0.03\text{mm}$	—	$0.03\text{mm} < W \leq 0.05\text{mm}$	$L \leq 5\text{mm}$	$N \leq 4$	$W > 0.05\text{mm}$
Size	Judging standard		Acceptance(Q'ty)														
0.96"	W	L	Ignore														
	$W \leq 0.03\text{mm}$	—															
	$0.03\text{mm} < W \leq 0.05\text{mm}$	$L \leq 5\text{mm}$	$N \leq 4$														
$W > 0.05\text{mm}$	$L > 5\text{mm}$	$N \leq 0$															
6	POL Polarizer Bubble	area	Judging standard	Acceptance(Q'ty)	Min												
		A 區 (Viewing area)	$D < 0.2 \text{ mm}$	Ignore													
			$0.2\text{mm} < D \leq 0.3\text{mm}$	$N \leq 3$													
			$0.3\text{mm} < D \leq 0.5\text{mm}$	$N \leq 1$													
			$0.5\text{mm} < D$	$N \leq 0$													
B (Outside of viewing area)	—	Ignore															
No	Inspection item	Inspection Standard		Defect Level													
7	POL The folding and peeled off in polarizer	The folding and peeled off in polarizer are not acceptable.		Min													
8	Brightness and uniformity、 Chroma	Shall be in accordance with the drawings and specification requirements specifications.		Maj													
9	MURA	(5% ND Filter) 50%															

10	Electrical Testing	<ol style="list-style-type: none"> <li>1. Missing line character and icon.</li> <li>2. No function or no display.</li> <li>3. Display malfunction.</li> <li>4. LCD (LCD viewing angle defect.</li> <li>5. Current consumption exceeds product specifications.</li> </ol>	Maj																			
11	<p>Bright dot, Dark dot On-display</p> <p>Pixel : 3 dot in 1 pixel</p> 	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="width: 10%;">Size</th> <th style="width: 10%;">Item</th> <th style="width: 50%;">Judging standard</th> <th style="width: 30%;">Acceptance(Q'ty)</th> </tr> </thead> <tbody> <tr> <td rowspan="4" style="vertical-align: middle;">0.96"</td> <td rowspan="2" style="vertical-align: middle;">Bright dot</td> <td style="text-align: center;"><math>D \leq 1/2 \text{ Dot}</math></td> <td style="text-align: center;">Ignore</td> </tr> <tr> <td style="text-align: center;"><math>1/2 \text{ Dot} &lt; D \leq 1 \text{ Dot}</math></td> <td style="text-align: center;"><math>N \leq 1</math></td> </tr> <tr> <td rowspan="2" style="vertical-align: middle;">Dark dot</td> <td style="text-align: center;"><math>D \leq 1/2 \text{ Dot}</math></td> <td style="text-align: center;">Ignore</td> </tr> <tr> <td style="text-align: center;"><math>1/2 \text{ Dot} &lt; D \leq 1 \text{ Dot}</math></td> <td style="text-align: center;"><math>N \leq 2</math></td> </tr> <tr> <td colspan="3" style="text-align: center;">Total</td> <td style="text-align: center;"><math>N \leq 2</math></td> </tr> </tbody> </table> <p style="color: purple;">Dark and bright dot is defined more than 50% area of one dot.</p>	Size	Item	Judging standard	Acceptance(Q'ty)	0.96"	Bright dot	$D \leq 1/2 \text{ Dot}$	Ignore	$1/2 \text{ Dot} < D \leq 1 \text{ Dot}$	$N \leq 1$	Dark dot	$D \leq 1/2 \text{ Dot}$	Ignore	$1/2 \text{ Dot} < D \leq 1 \text{ Dot}$	$N \leq 2$	Total			$N \leq 2$	Min
Size	Item	Judging standard	Acceptance(Q'ty)																			
0.96"	Bright dot	$D \leq 1/2 \text{ Dot}$	Ignore																			
		$1/2 \text{ Dot} < D \leq 1 \text{ Dot}$	$N \leq 1$																			
	Dark dot	$D \leq 1/2 \text{ Dot}$	Ignore																			
		$1/2 \text{ Dot} < D \leq 1 \text{ Dot}$	$N \leq 2$																			
Total			$N \leq 2$																			

### 13. Initial Code for Reference

GATE = 160;  
SOURCE = 80;

//RESET

```
SPI_RST = 1; //RA0
delay1(10);
SPI_RST = 0;
delay1(1000);
SPI_RST = 1;
delay1(10);
```

//20180302 Brian add

```
//Sleep out
SPI_0096A_WrCmd(0x11); //Sleep out
delay(120);
```

//ST7735S Frame Rate Setting in normal mode: fosc/

```
((RTNA*2)+40)*(LINE+FPA+BPA+2)=80
SPI_0096A_WrCmd(0XB1); // fosc=850KHz
SPI_0096A_WriteData(0X05); // RTNA=5
SPI_0096A_WriteData(0X3C); //20180612 // FPA=58
SPI_0096A_WriteData(0X3C); //20180612 // BPA=58
```

//ST7735S Frame Rate Setting in idle mode: fosc/ ((RTNB\*2)+40)\*(LINE+FPB+BPB+2)=80

```
SPI_0096A_WrCmd(0XB2); // fosc=850KHz
SPI_0096A_WriteData(0X05); // RTNB=5
SPI_0096A_WriteData(0X3C); //20180612 // FPB=58
SPI_0096A_WriteData(0X3C); //20180612 // BPB=58
```

//ST7735S Frame Rate Setting in parital mode (dot inverson): fosc/

((RTNC\*2)+40)\*(LINE+FPC+BPC+2)=80

//ST7735S Frame Rate Setting in parital mode (column inverson): fosc/

```
((RTNC*2)+40)*(LINE+FPC+BPC+2)=80
SPI_0096A_WrCmd(0XB3); // fosc=850KHz
SPI_0096A_WriteData(0X05); // RTNC=5
SPI_0096A_WriteData(0X3C); //20180612 // FPC=58
SPI_0096A_WriteData(0X3C); //20180612 // BPC=58
SPI_0096A_WriteData(0X05); // RTND=5
SPI_0096A_WriteData(0X3C); //20180612 // FPD=58
SPI_0096A_WriteData(0X3C); //20180612 // BPD=58
```

//ST7735S Display Inversion Control

```
SPI_0096A_WrCmd(0XB4); // Dot inversion: 20184019 modify
from Sitronix initial code
SPI_0096A_WriteData(0X07); // 0xB4[2]=Inversion setting in
normal mode
```

// 0xB4[1]=Inversion setting in



idle mode

// 0xB4[0]=Inversion setting in

partial mode

//ST7735S Power on Sequence

```

SPI_0096A_WrCmd(0XC0); // power control 1
SPI_0096A_WriteData(0XE9); //20180612 //
{Par.3[0],Par.1[4:0]}=VRHP[5:0]=2→GVDD=4.6, Par.1[7:5]=AVDD [2:0]=6→AVDD=5.1
SPI_0096A_WriteData(0X09); //20180612 //
{Par.3[1],Par.2[4:0]}=VRHN[5:0]=2→GVCL=-4.6
SPI_0096A_WriteData(0X04); // Par.3[7:6]=MODE[1:0]=2X

```

```

SPI_0096A_WrCmd(0XC1); // power control 2
SPI_0096A_WriteData(0XC5); //20180612 // Par.1
[1:0]=VGHBT[1:0]=0→VGH=2*AVDD+VGH25-0.5

```

// Par.1

[3:2]=VGLSEL[1:0]=0→VGL=-7.5

// Par.1

[7:6]=VGLSEL[1:0]=3→VGH25=2.4

```

SPI_0096A_WrCmd(0XC2); // power control 3
SPI_0096A_WriteData(0X0D); //20180612 // (Sitronix initial) {Par.1
[7:6],Par.2[7:0]=DCA[9:0]=00000000'b→Booster set up cycle BCLK/1 BCLK/3 BCLK/1
BCLK/1 BCLK/1 in normal mode
SPI_0096A_WriteData(0X00); // Par.1[5:3]=SAPA[2:0]=001'b→ OP
current is small in normal mode // Par.1[2:0]=APA[2:0]=001'b→

```

OP current is Large in normal mode

```

SPI_0096A_WrCmd(0XC3); // power control 4
SPI_0096A_WriteData(0X8D); //20180612 // (Sitronix initial){Par.1
[7:6],Par.2[7:0]=DCB[9:0]=1001101010'b→Booster set up cycle BCLK/2 BCLK/1 BCLK/2
BCLK/2 BCLK/2 in idle mode
SPI_0096A_WriteData(0X6A); // Par.1[5:3]=SAPB[2:0]=001'b→ OP
current is small in idle mode // Par.1[2:0]=APB[2:0]=011'b→

```

OP current is Medium in idle mode

```

SPI_0096A_WrCmd(0XC4); // power control 5
SPI_0096A_WriteData(0X8D); //20180612 // (Sitronix initial){Par.1
[7:6],Par.2[7:0]=DCC[9:0]=1011101110'b→Booster set up cycle BCLK/2 BCLK/2 BCLK/2
BCLK/4 BCLK/2 in partial mode
SPI_0096A_WriteData(0XEE); // Par.1[5:3]=SAPC[2:0]=001'b→
OP current is small in partial mode

```

// ST7735S VCOM

SPI\_0096A\_WrCmd(0XC5); // VCOM setting value

SPI\_0096A\_WriteData(0X15); //20180612 // 0XC5[5:0]=010010'b  
→ VCOM=-0.875

// ST7735 Memory data access control: add from Sitronix initial code  
SPI\_0096A\_WrCmd(0X36); // VCOM setting value  
SPI\_0096A\_WriteData(0XC8);  
//ST7735 Display Inversion on  
SPI\_0096A\_WrCmd(0X21);

// ST7735 Gamma Sequence  
SPI\_0096A\_WrCmd(0XE0); // Gamma setting value (Positive  
Polarity)  
SPI\_0096A\_WriteData(0X07); //20180612 //  
Par.1[5:0]=VRF0P[5:0]=000011'b (Variable Resistor VRHP)  
SPI\_0096A\_WriteData(0X0E); //20180612 //  
Par.2[5:0]=VOS0P[5:0]=011011'b (Variable Resistor VRLP)  
SPI\_0096A\_WriteData(0X08); //20180612 //  
Par.3[5:0]=PK0P[5:0]=010010'b (Voltage of V3 grayscale)  
SPI\_0096A\_WriteData(0X07); //20180612 //  
Par.4[5:0]=PK1P[5:0]=010001'b (Voltage of V4 grayscale)  
SPI\_0096A\_WriteData(0X10); //20180612 //  
Par.5[5:0]=PK2P[5:0]=111111'b (Voltage of V12 grayscale)  
SPI\_0096A\_WriteData(0X07); //20180612 //  
Par.6[5:0]=PK3P[5:0]=111010'b (Voltage of V20 grayscale)  
SPI\_0096A\_WriteData(0X02); //20180612 //  
Par.7[5:0]=PK4P[5:0]=111010'b (Voltage of V28 grayscale)  
SPI\_0096A\_WriteData(0X07); //20180612 //  
Par.8[5:0]=PK5P[5:0]=110100'b (Voltage of V36 grayscale)  
SPI\_0096A\_WriteData(0X09); //20180612 //  
Par.9[5:0]=PK6P[5:0]=101111'b (Voltage of V44 grayscale)  
SPI\_0096A\_WriteData(0X0F); //20180612 //  
Par.10[5:0]=PK7P[5:0]=101011'b (Voltage of V52 grayscale)  
SPI\_0096A\_WriteData(0X25); //20180612 //  
Par.11[5:0]=PK8P[5:0]=110000'b (Voltage of V56 grayscale)  
SPI\_0096A\_WriteData(0X36); //20180612 //  
Par.12[5:0]=PK9P[5:0]=111010'b (Voltage of V60 grayscale)  
SPI\_0096A\_WriteData(0X00); //  
Par.13[5:0]=SELV0P[5:0]=000000'b (Voltage of V0 grayscale)  
SPI\_0096A\_WriteData(0X08); //20180612 //  
Par.14[5:0]=SELV1P[5:0]=000001'b (Voltage of V1 grayscale)  
SPI\_0096A\_WriteData(0X04); //20180612 //  
Par.15[5:0]=SELV62P[5:0]=000010'b (Voltage of V62 grayscale)  
SPI\_0096A\_WriteData(0X10); //20180612 //  
Par.16[5:0]=SELV63P[5:0]=001001'b (Voltage of V63 grayscale)

```
SPI_0096A_WrCmd(0XE1); // Gamma setting value
(Negative Polarity)
SPI_0096A_WriteData(0X0A); //20180612 //
Par.1[5:0]=VRF0N[5:0]=000011'b (Variable Resistor VRHN)
SPI_0096A_WriteData(0X0D); //20180612 //
Par.2[5:0]=VOS0N[5:0]=011011'b (Variable Resistor VRLN)
SPI_0096A_WriteData(0X08); //20180612 //
Par.3[5:0]=PK0N[5:0]=010010'b (Voltage of V3 grayscale)
SPI_0096A_WriteData(0X07); //20180612 //
Par.4[5:0]=PK1N[5:0]=010001'b (Voltage of V4 grayscale)
SPI_0096A_WriteData(0X0F); //20180612 //
Par.5[5:0]=PK2N[5:0]=110010'b (Voltage of V12 grayscale)
SPI_0096A_WriteData(0X07); //20180612 //
Par.6[5:0]=PK3N[5:0]=101111'b (Voltage of V20 grayscale)
SPI_0096A_WriteData(0X02); //20180612 //
Par.7[5:0]=PK4N[5:0]=101010'b (Voltage of V28 grayscale)
SPI_0096A_WriteData(0X07); //20180612 //
Par.8[5:0]=PK5N[5:0]=101111'b (Voltage of V36 grayscale)
SPI_0096A_WriteData(0X09); //20180612 //
Par.9[5:0]=PK6N[5:0]=101110'b (Voltage of V44 grayscale)
SPI_0096A_WriteData(0X0F); //20180612 //
Par.10[5:0]=PK7N[5:0]=101100'b (Voltage of V52 grayscale)
SPI_0096A_WriteData(0X25); //20180612 //
Par.11[5:0]=PK8N[5:0]=111001'b (Voltage of V56 grayscale)
SPI_0096A_WriteData(0X35); // Par.12[5:0]=PK9N[5:0]=111111'b
(Voltage of V60 grayscale)
SPI_0096A_WriteData(0X00); //
Par.13[5:0]=SELV0N[5:0]=000000'b (Voltage of V0 grayscale)
SPI_0096A_WriteData(0X09); //20180612 //
Par.14[5:0]=SELV1N[5:0]=000000'b (Voltage of V1 grayscale)
SPI_0096A_WriteData(0X04); //20180612 //
Par.15[5:0]=SELV62N[5:0]=000001'b (Voltage of V62 grayscale)
SPI_0096A_WriteData(0X10); //20180612 //
Par.16[5:0]=SELV63N[5:0]=001001'b (Voltage of V63 grayscale)

SPI_0096A_WrCmd(0XFC); // Enable Gate power save mode
SPI_0096A_WriteData(0XC0); //
0XFC[7:6]=GCV_Enable[1:0]=10'b→ Gate Pump Clock Frequency disable
//
0XFC[3:2]=CLK_Variable[1:0]=11'b→ Save Power Ability is Large
SPI_0096A_WrCmd(0X3A);
SPI_0096A_WriteData(0X05); // 65K Mode

SPI_0096A_WrCmd(0X2A);
SPI_0096A_WriteData(0X00); // 65K Mode
SPI_0096A_WriteData(0X1A); // 65K Mode
SPI_0096A_WriteData(0X00); // 65K Mode
SPI_0096A_WriteData(0X69); // 65K Mode
```

SPI\_0096A\_WrCmd(0X2B);  
SPI\_0096A\_WriteData(0X00); // 6  
SPI\_0096A\_WriteData(0X01); //  
SPI\_0096A\_WriteData(0X00); //  
SPI\_0096A\_WriteData(0XA0); //

SPI\_0096A\_WrCmd(0X29); // Display on