DISPLAY Elektronik GmbH

# DATA SHEET

## LCD MODULE

# DEM 240064B FGH-P(RGB)

*Product Specification* *Version : 5*

**18.12.2018**

# GENERAL SPECIFICATION

## MODULE NO. :

# DEM 240064B FGH-P(RGB)

CUSTOMER P/N:

| VERSION NO. | CHANGE DESCRIPTION | DATE |
|---|---|---|
| 0 | ORIGINAL VERSION | 28.10.2008 |
| 1 | CHANGE MODULE DRAWING AND LCD DRAWING | 31.10.2008 |
| 2 | ADD PRINT ON THE FPC | 04.11.2008 |
| 3 | Change the minimum voltage of BL on page 7 | 29.11.2018 |
| 4 | Change the backlight lifetime on page 7 | 12.12.2018 |
| 5 | Correct the BL power dissipation on page 7 | 18.12.2018 |
| | | |
| | | |
| | | |
| | | |
| | | |

PREPARED BY: CC DATE: 18.12.2018

APPROVED BY: MHO DATE: 18.12.2018

# CONTENTS

## 1. FUNCTIONS & FEATURES

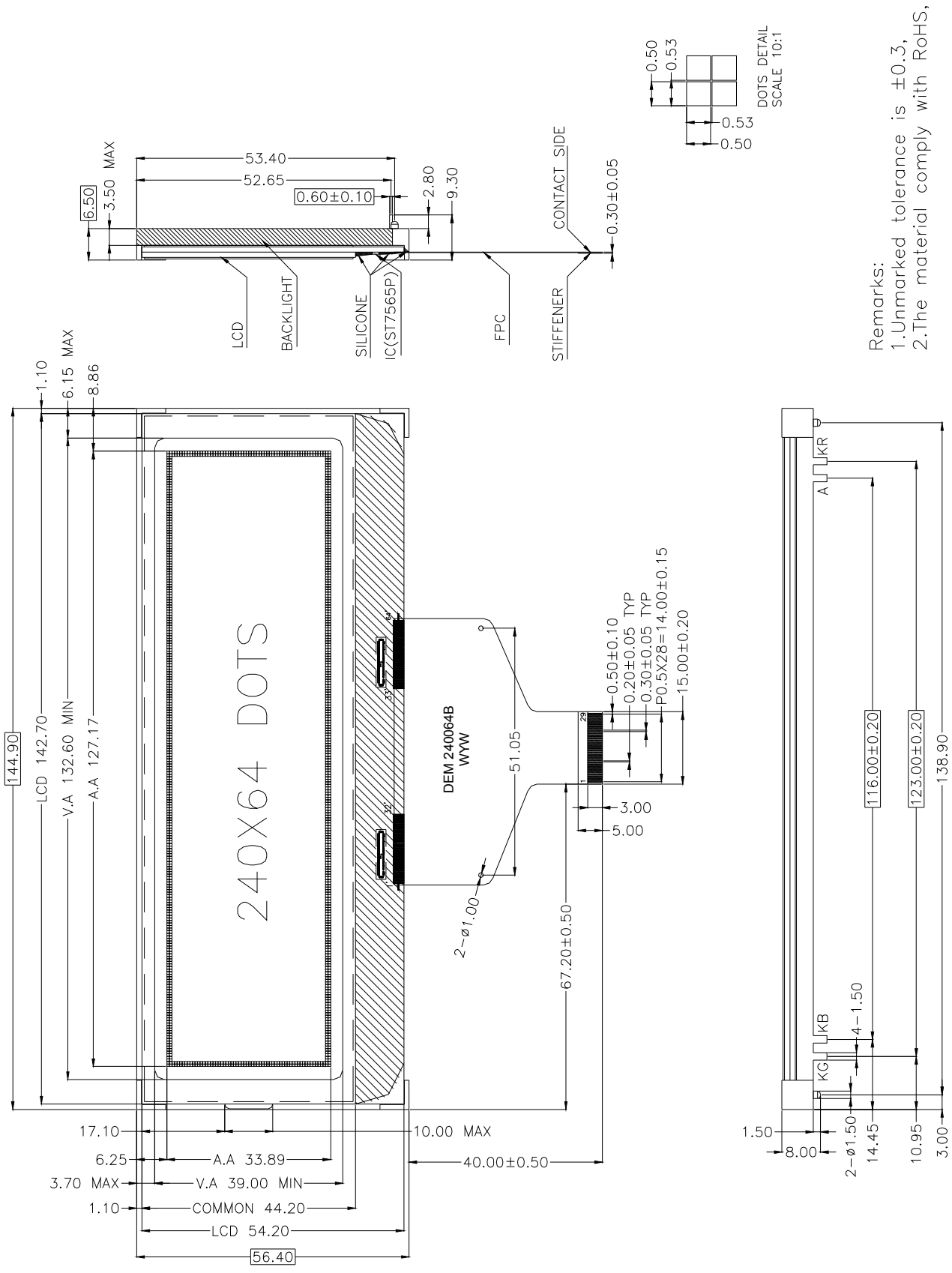
| MODULE | LCD TYPE | Remark |
|---|---|---|
| DEM 240064B FGH-P(RGB) | FSTN Transflective Positive Mode | --- |

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65 Duty Cycle, 1/9 Bias
- Power Supply Voltage : 3.3 Volt (typ.)
- LCD Operation Voltage : 11.0 Volt (typ.)
- Display Contents : 240 x 64 Dots
- Operating Temperature : -20°C ~ +70°C
- Storage Temperature : -30°C ~+80°C
- Backlight: : LED, Lightguide, RGB-Backlight
- LCD-Driver: : ST7565P (2x) Sitronix

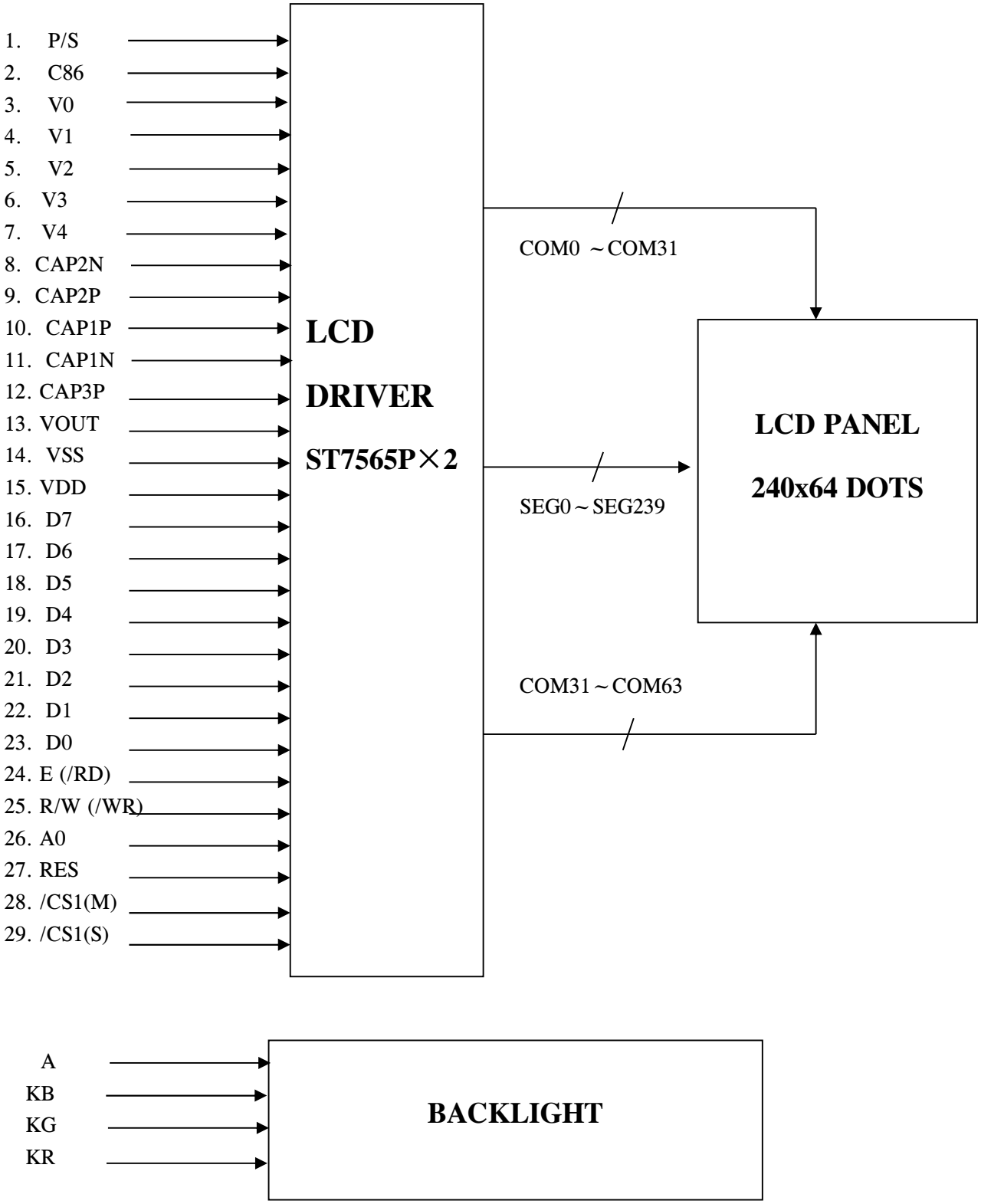
## 2. MECHANICAL SPECIFICATIONS

- Module Size : 144.90 x 56.40 x 6.50 mm
- Dot Size : 0.50 x 0.50 mm
- Dot Gap : 0.03 mm
- View Area Size : 132.60 x 39.00 mm

## 3. EXTERNAL DIMENSIONS



## 4. BLOCK DIAGRAM



## 5. PIN ASSIGNMENT

<table>
<tr><th>Pin No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>P/S</td><td>This is the parallel data input/serial data input switch terminal.<br>P/S = “H”: Parallel data input.<br>P/S = “L”: Serial data input.<br>The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>DATA/Command</th><th>Data</th><th>Read/Write</th><th>4-line SPI Clock</th></tr>
<tr><td>H</td><td>D/C(A0)</td><td>D0 to D7</td><td>/RD,/WR</td><td>×</td></tr>
<tr><td>L</td><td>D/C(A0)</td><td>SI(D7)</td><td>Write only</td><td>SCL(D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 fixed “H”.<br>/RD (E) and /WR (R/W) are fixed to either “H” or “L”.<br>With serial data input, It is impossible read data from RAM .</td></tr>
<tr><td>2</td><td>C86</td><td>This is the MPU interface switch terminal.<br>C86 = “H”: 6800 Series MPU interface.<br>C86 = “L”: 8080 MPU interface.</td></tr>
<tr><td>3</td><td>V0</td><td rowspan="5">This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.<br>V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss<br>When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr>
<tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr>
<tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr>
<tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr>
</table></td></tr>
<tr><td>4</td><td>V1</td></tr>
<tr><td>5</td><td>V2</td></tr>
<tr><td>6</td><td>V3</td></tr>
<tr><td>7</td><td>V4</td></tr>
<tr><td>8</td><td>CAP2N</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP2P terminal.</td></tr>
<tr><td>9</td><td>CAP2P</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP2N terminal.</td></tr>
<tr><td>10</td><td>CAP1P</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and CAP1N terminal.</td></tr>
<tr><td>11</td><td>CAP1N</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP1P terminal.</td></tr>
<tr><td>12</td><td>CAP3P</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP1N terminal.</td></tr>
<tr><td>13</td><td>VOUT</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and VSS or VDD.</td></tr>
<tr><td>14</td><td>VSS</td><td>0V pin connected to the system ground (GND)</td></tr>
<tr><td>15</td><td>VDD</td><td>Power supply for logic (+3.3V)</td></tr>
<tr><td>16</td><td>D7</td><td rowspan="8">This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.<br>When the serial interface is selected (P/S = “L”) :<br>D7: serial data input (SI ; D6 : the serial clock input (SCL).<br>D0 to D5 are set to high impedance.<br>When the chip select is not active, D0 to D7 are set to high impedance.</td></tr>
<tr><td>17</td><td>D6</td></tr>
<tr><td>18</td><td>D5</td></tr>
<tr><td>19</td><td>D4</td></tr>
<tr><td>20</td><td>D3</td></tr>
<tr><td>21</td><td>D2</td></tr>
<tr><td>22</td><td>D1</td></tr>
<tr><td>23</td><td>D0</td></tr>
</table>

| | | |
|---|---|---|
| 24 | E(/RD) | • When connected to an 8080 MPU, this is active LOW.<br>(E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is “L”.<br>• When connected to a 6800 Series MPU, this is active HIGH.<br>This is the 6800 Series MPU enable clock input terminal. |
| 25 | R/W(/WR) | • When connected to an 8080 MPU, this is active LOW.<br>(R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal.<br>• When connected to a 6800 Series MPU:<br>This is the read/write control signal input terminal.<br>When R/W = “H”: Read.<br>When R/W = “L”: Write. |
| 26 | A0 | This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.<br>A0 = “H”: Indicates that D0 to D7 are display data.<br>A0 = “L”: Indicates that D0 to D7 are control data. |
| 27 | /RES | When /RES is set to “L,” the settings are initialized.<br>The reset operation is performed by the /RES signal level. |
| 28 | /CS1(M) | This is the chip select signal. When /CS1 = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled. |
| 29 | /CS1(S) | |

## 6. BACKLIGHT ELECTRONIC/OPTICAL SPECIFICATION

Electronic/Optical Specifications:

### RED:

| | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_f$ | 2.9 | 3.2 | 3.4 | V | If=120 mA |
| Power Dissipation | $P_d$ | | | 0.408 | W | If=120 mA |
| Reverse Voltage | $V_R$ | | | 5 | V | |
| Reverse Current | $I_R$ | | | 0.8 | mA | $V_r$ = 5.0 V |
| Luminous Intensity | $I_V$ | TBD | 40 | TBD | $cd/m^2$ | If=120 mA |
| Luminous Uniformity | | 70 | | | % | If=120 mA |
| Emission Wavelength | $\lambda_P$ | 620 | | 630 | nm | $I_f$=15mA Ta=25° C Each chip |
| Life Time | 30Khrs | | | | | |

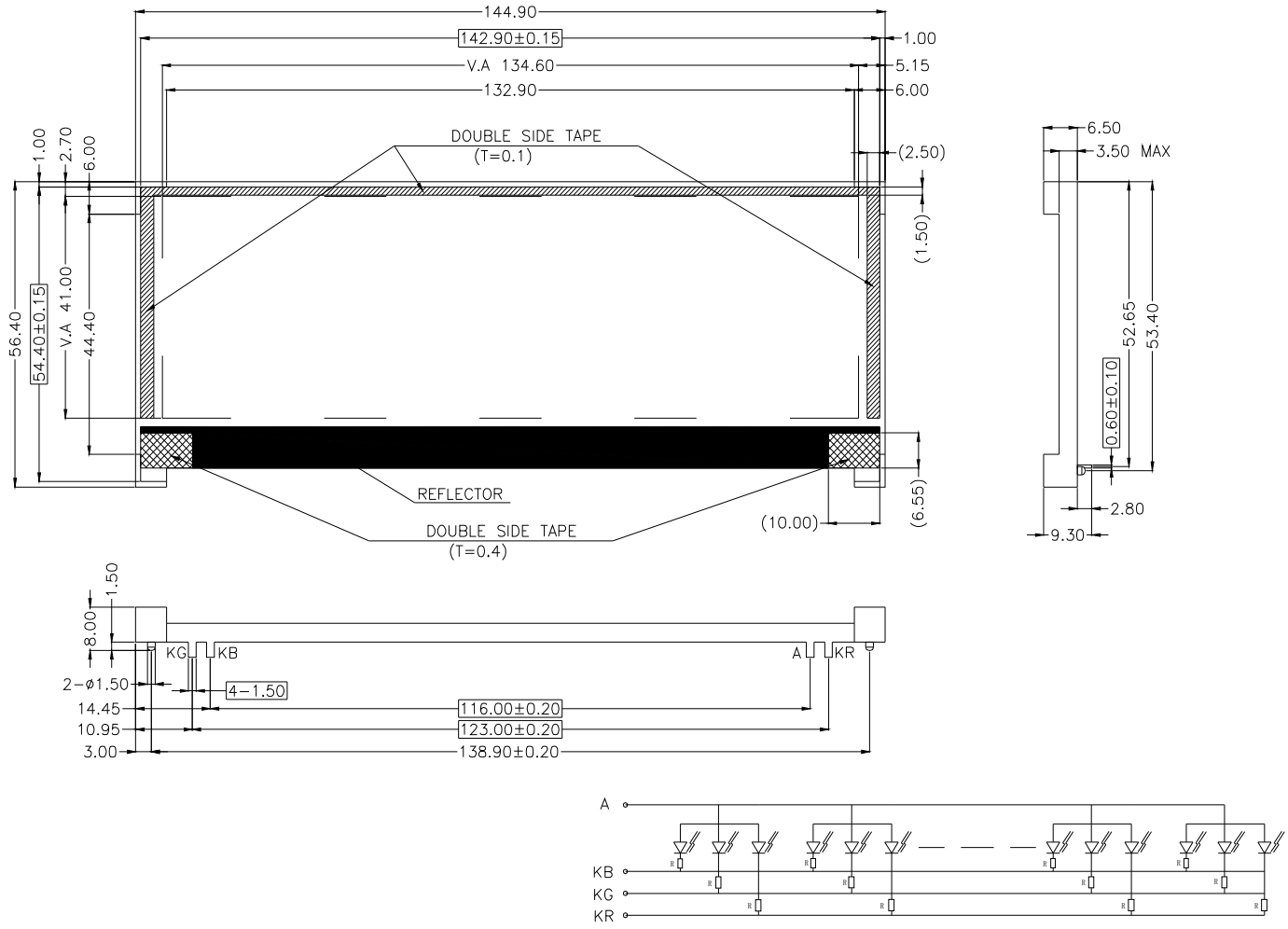
### BLUE:

| | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_f$ | 2.9 | 3.2 | 3.4 | V | If=120 mA |
| Power Dissipation | $P_d$ | | | 0.408 | W | If=120 mA |
| Reverse Voltage | $V_R$ | | | 5 | V | |
| Reverse Current | $I_R$ | | | 0.8 | mA | $V_r$ = 5.0 V |
| Luminous Intensity | $I_V$ | TBD | 20 | TBD | $cd/m^2$ | If=120 mA |
| Luminous Uniformity | | 70 | | | % | If=120 mA |
| Emission Wavelength | $\lambda_P$ | 465 | | 476 | nm | $I_f$=15mA Ta=25° C Each chip |
| Life Time | 30Khrs | | | | | |

### GREEN:

| | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_f$ | 2.9 | 3.2 | 3.4 | V | If=120 mA |
| Power Dissipation | $P_d$ | | | 0.408 | W | If=120 mA |
| Reverse Voltage | $V_R$ | | | 5 | V | |
| Reverse Current | $I_R$ | | | 0.8 | mA | $V_r$ = 5.0 V |
| Luminous Intensity | $I_V$ | TBD | 100 | TBD | $cd/m^2$ | If=120 mA |
| Luminous Uniformity | | 70 | | | % | If=120 mA |
| Emission Wavelength | $\lambda_P$ | 520 | | 530 | nm | $I_f$=15mA Ta=25° C Each chip |
| Life Time | 30Khrs | | | | | |

| | SYMBOL | RATINGS |
|---|---|---|
| Operating Temperature | Topr | -20° C to +70° C |
| | Tsty | -30° C to +80° C |




Remarks:
1.Unmarked tolerance is ±0.2,
2.The material comply with RoHS,
3.NO.OF SMT LED:8PCS

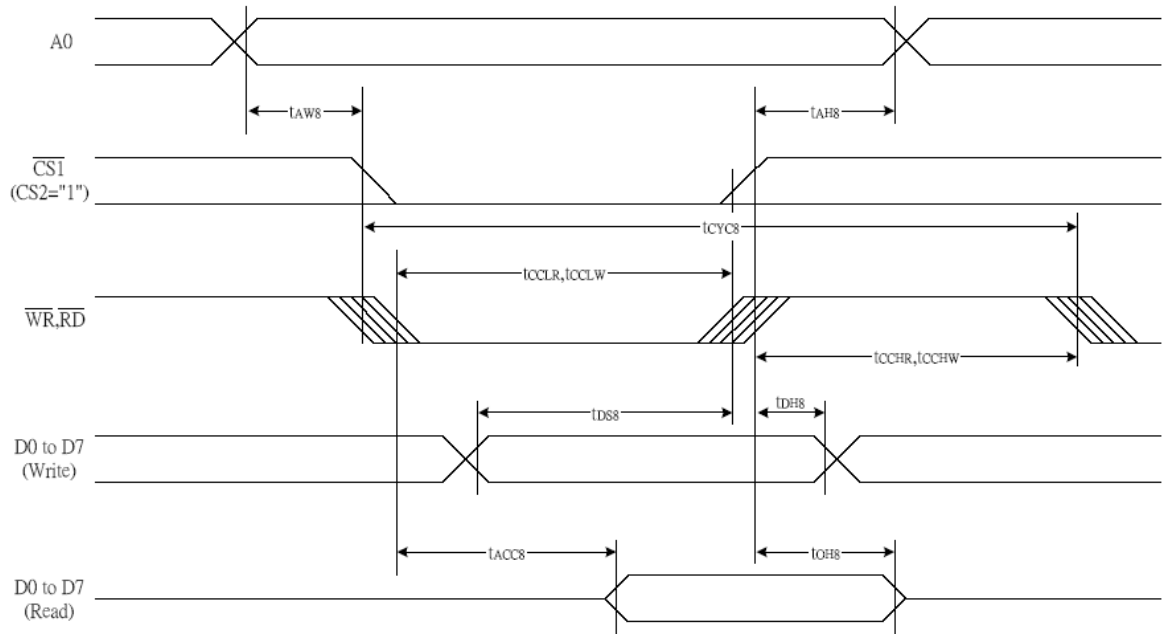
## 7. DC CHARACTERISTICS

($V_{DD}$=3.3V, Ta=25°C)

| ITEM | symbol | STANDARD VALUE | | | TEST CONDITION | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Operating Voltage (1) | $V_{DD}$ | 3.0 | 3.3 | 3.6 | | V |
| Operating Voltage (2) | $V_{LCD}$ | 10.5 | 11.0 | 11.5 | | |
| Current Consumption | $I_{DD}$ | --- | TBD | --- | $V_{DD}$=3.3V±0.3V<br>$V_{LCD}$ =11.0V | mA |

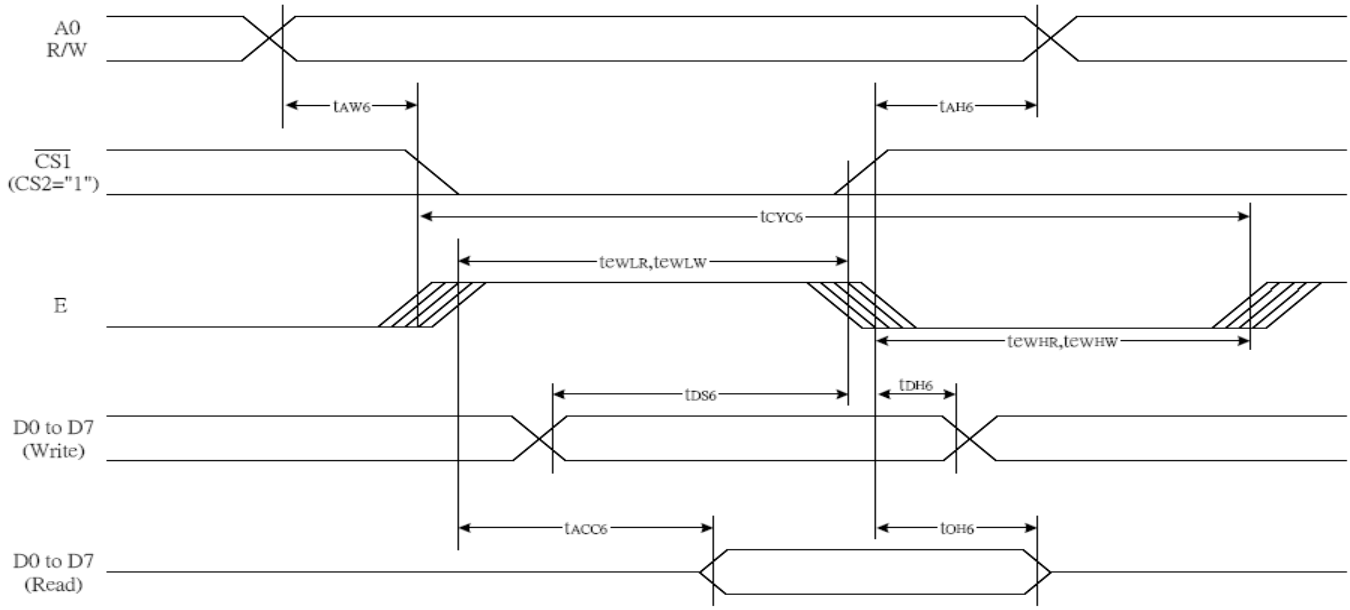
## 8. AC ELECTRICAL CHARACTERISTICS

8.1 System bus Read/Write characteristics for the 8080 series MPU



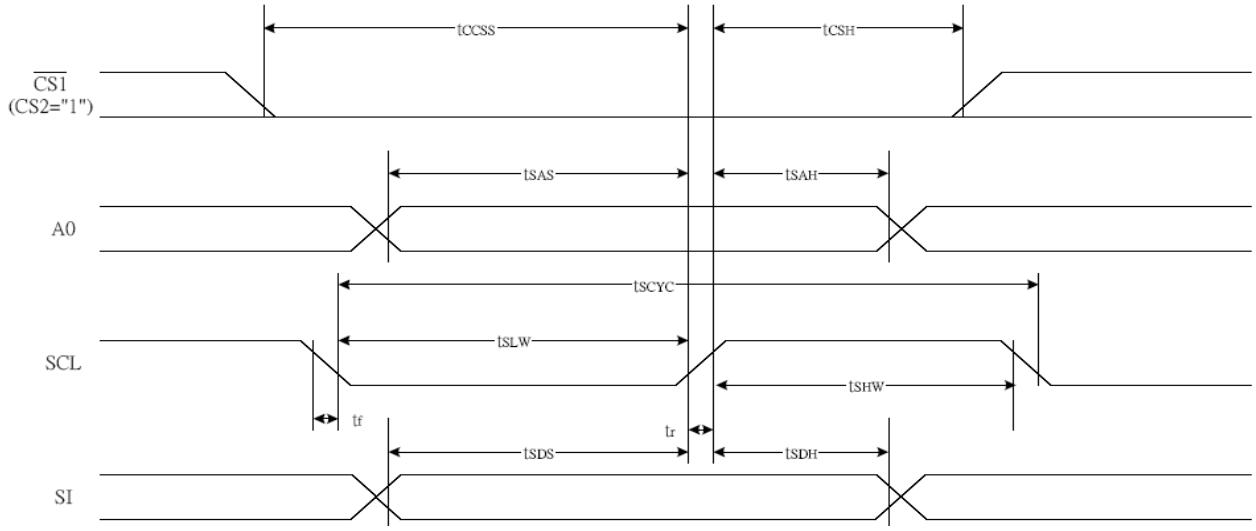

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0 | $t_{AH8}$ | | 0 | — | Ns |
| Address setup time | | $t_{AW8}$ | | 0 | — | |
| System cycle time | | $t_{CYC8}$ | | 240 | — | |
| Enable L pulse width (WRITE) | WR | $t_{CCLW}$ | | 80 | — | |
| Enable H pulse width (WRITE) | | $t_{CCHW}$ | | 80 | — | |
| Enable L pulse width (READ) | RD | $t_{CCLR}$ | | 140 | — | |
| Enable H pulse width (READ) | | $t_{CCHR}$ | | 80 | | |
| WRITE Data setup time | D0 to D7 | $t_{DS8}$ | | 40 | — | |
| WRITE Address hold time | | $t_{DH8}$ | | 0 | — | |
| READ access time | | $t_{ACC8}$ | $C_L$ = 100 pF | — | 70 | |
| READ Output disable time | | $t_{OH8}$ | $C_L$ = 100 pF | 5 | 50 | |

8. 2. System bus READ/WRITE characteristic for the 6800 series MPU



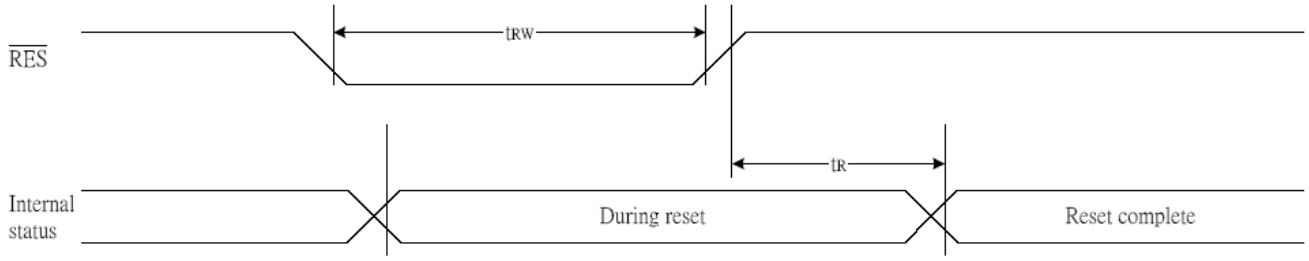

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0 | tAH6 | | 0 | — | ns |
| Address setup time | | tAW6 | | 0 | — | |
| System cycle time | | tCYC6 | | 240 | — | |
| Enable L pulse width (WRITE) | WR | tEWLW | | 80 | — | |
| Enable H pulse width (WRITE) | | tEWHW | | 80 | — | |
| Enable L pulse width (READ) | RD | tEWLR | | 80 | — | |
| Enable H pulse width (READ) | | tEWHR | | 140 | | |
| WRITE Data setup time | D0 to D7 | tDS6 | | 40 | — | |
| WRITE Address hold time | | tDH6 | | 0 | — | |
| READ access time | | tACC6 | CL = 100 pF | — | 70 | |
| READ Output disable time | | tOH6 | CL = 100 pF | 5 | 50 | |

8.3. Serial Interface



| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial Clock Period | SCL | Tscyc | | 50 | — | ns |
| SCL "H" pulse width | | Tshw | | 25 | — | |
| SCL "L" pulse width | | TSLW | | 25 | — | |
| Address setup time | A0 | TSAS | | 20 | — | |
| Address hold time | | Tsah | | 10 | — | |
| Data setup time | SI | Tsds | | 20 | — | |
| Data hold time | | TSDH | | 10 | — | |
| CS-SCL time | CS | Tcss | | 20 | — | |
| CS-SCL time | | Tcsh | | 40 | — | |

8.4 Reset Timing




| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Reset time | | tR | | — | — | 1.0 | us |
| Reset "L" pulse width | /RES | tRW | | 1.0 | — | — | us |

## 9. ABSOLUTE MAXIMUM RATINGS

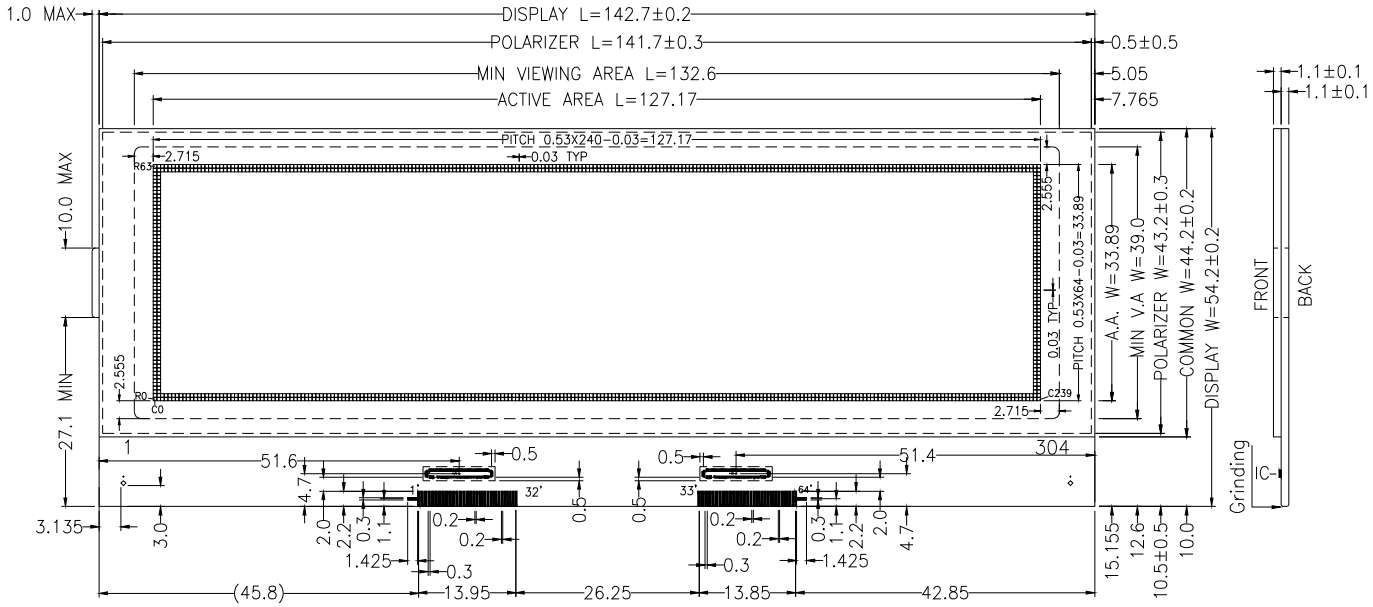
| Parameter | Symbol | Conditions | Unit |
|---|---|---|---|
| Power Supply Voltage | VDD | 0.3 ~ 3.6 | V |
| Power supply voltage (VDD standard) | VDD2 | 0.3 ~ 3.6 | V |
| Power supply voltage (VDD standard) | V0, VOUT | 0.3 ~ 14.5 | V |
| Power supply voltage (VDD standard) | V1, V2, V3, V4 | V0 to 0.3 | V |

## 10. COMMAND TABLE

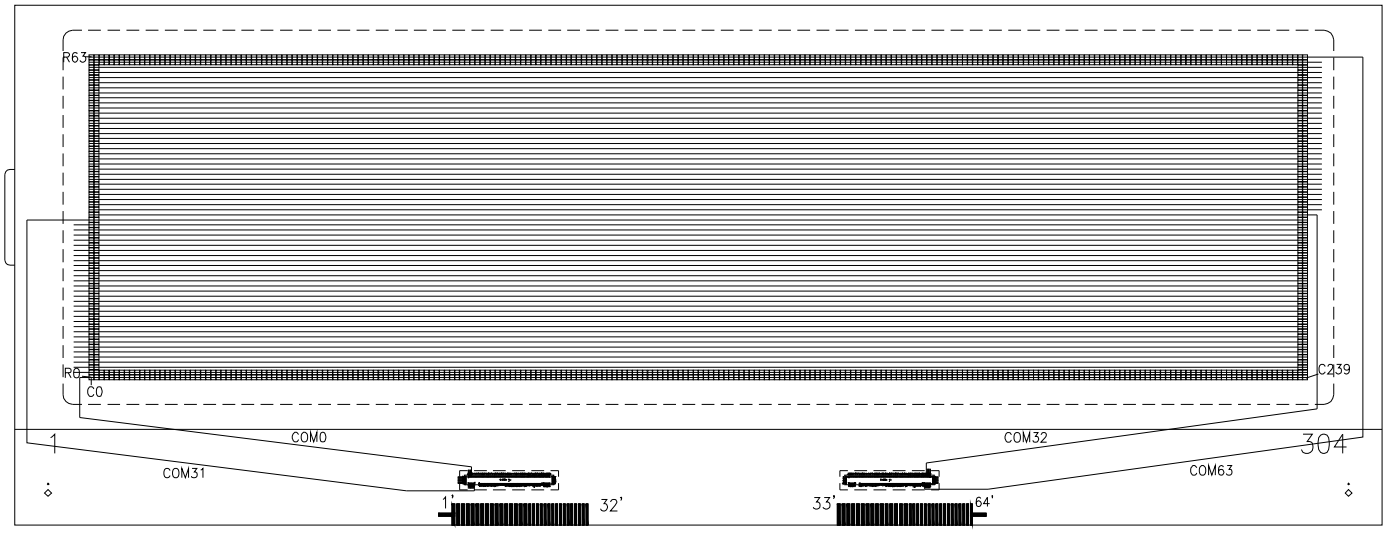
Table of ST7565P Commands (Note) *: disabled data

| Command | Command Code | | | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | /RD | /WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0<br>1 | LCD display ON/OFF<br>0: OFF, 1: ON |
| (2) Display start line set | 0 | 1 | 0 | 0 | 1 | Display start address | | | | | | Sets the display RAM display start line address |
| (3) Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page address | | | | Sets the display RAM page address |
| (4) Column address set upper bit<br>Column address set lower bit | 0<br>0 | 1<br>1 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>0 | 1<br>0 | Most significant column address<br>Least significant column address | | | | Sets the most significant 4 bits of the display RAM column address.<br>Sets the least significant 4 bits of the display RAM column address. |
| (5) Status read | 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 | Reads the status data |
| (6) Display data write | 1 | 1 | 0 | Write data | | | | | | | | Writes to the display RAM |
| (7) Display data read | 1 | 0 | 1 | Read data | | | | | | | | Reads from the display RAM |
| (8) ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0<br>1 | Sets the display RAM address SEG output correspondence<br>0: normal, 1: reverse |
| (9) Display normal/ reverse | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0<br>1 | Sets the LCD display normal/ reverse<br>0: normal, 1: reverse |
| (10) Display all points ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0<br>1 | Display all points<br>0: normal display<br>1: all points ON |
| (11) LCD bias set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0<br>1 | Sets the LCD drive voltage bias ratio<br>0: 1/9 bias, 1: 1/7 bias (ST7565P) |
| (12) Read/modify/write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Column address increment<br>At write: +1<br>At read: 0 |
| (13) End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clear read/modify/write |
| (14) Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Internal reset |
| (15) Common output mode select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0<br>1 | * | * | * | Select COM output scan direction<br>0: normal direction<br>1: reverse direction |
| (16) Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Operating mode | | | Select internal power supply operating mode |
| (17) $V_0$ voltage regulator internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Resistor ratio | | | Select internal resistor ratio(Rb/Ra) mode |
| (18) Electronic volume mode set<br>Electronic volume register set | 0 | 1 | 0 | 1<br>0 | 0<br>0 | 0<br>Electronic volume value | 0 | 0 | 0 | 0 | 1 | Set the $V_0$ output voltage electronic volume register |
| (19) Static indicator ON/OFF<br>Static indicator register set | 0 | 1 | 0 | 1<br>0 | 0<br>0 | 1<br>0 | 0<br>0 | 1<br>0 | 1<br>0 | 0<br>0 | 0<br>1<br>Mode | 0: OFF, 1: ON<br>Set the flashing mode |
| (20) Booster ratio set | 0 | 1 | 0 | 1<br>0 | 1<br>0 | 1<br>0 | 1<br>0 | 1<br>0 | 0<br>0 | 0<br>step-up value | 0 | select booster ratio<br>00: 2x,3x,4x<br>01: 5x<br>11: 6x |
| (21) Power saver | | | | | | | | | | | | Display OFF and display all points ON compound command |
| (22) NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Command for non-operation |
| (23) Test | 0 | 1 | 0 | 1 | 1 | 1 | 1 | * | * | * | * | Command for IC test. Do not use this command |

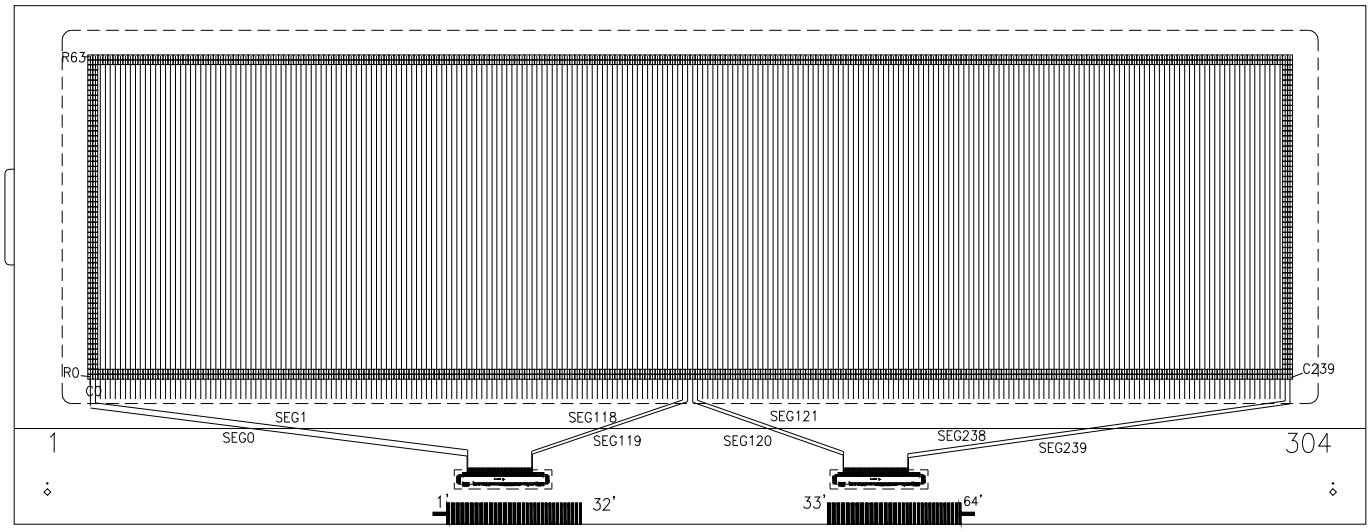
## 11. LCD ARTWORK



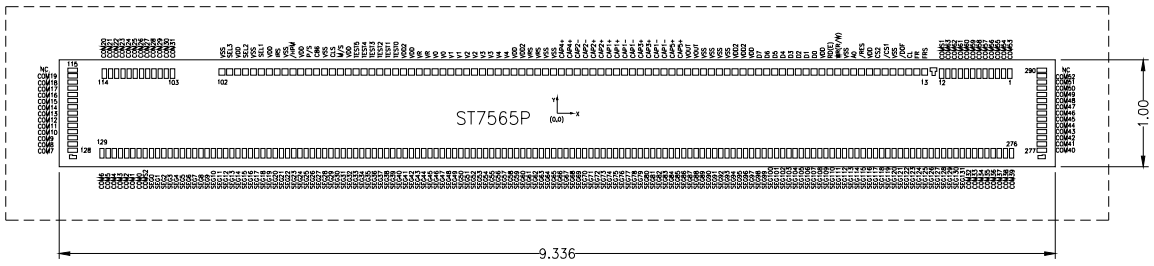

## 12. COMMON LAYOUT



## 13. SEGMENT LAYOUT




## 14. IC PAD CONFIGURATION



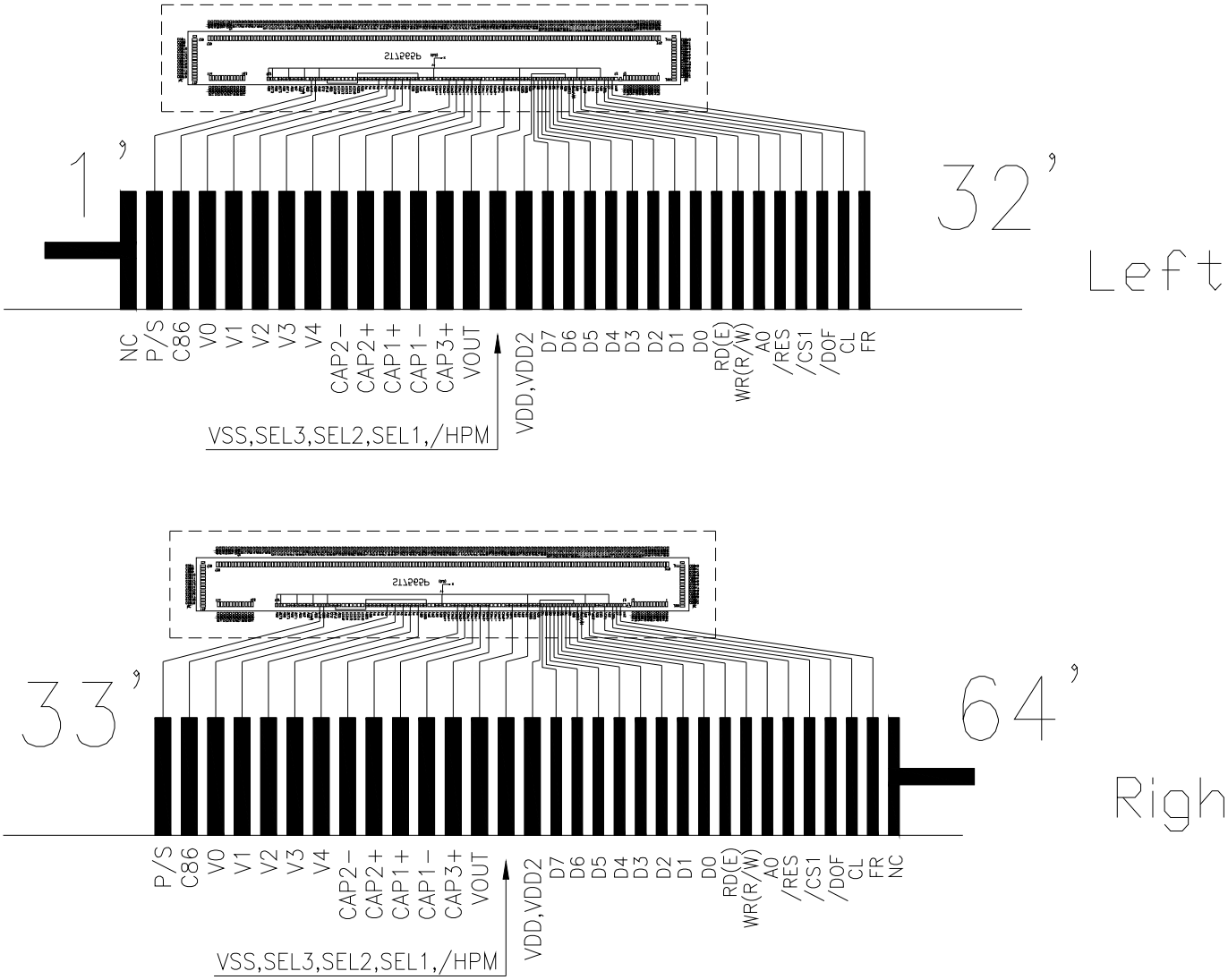

### Left

| PAD NO. | CONFIGURATION |
|---|---|
| 1' | NC |
| 2' | P/S |
| 3' | C86 |
| 4' | V0 |
| 5' | V1 |
| 6' | V2 |
| 7' | V3 |
| 8' | V4 |
| 9' | CAP2− |
| 10' | CAP2+ |
| 11' | CAP1+ |
| 12' | CAP1− |
| 13' | CAP3+ |
| 14' | VOUT |
| 15' | VSS,SEL3,SEL2, SEL1,/HPM |
| 16' | VDD,VDD2 |
| 17' | D7 |
| 18' | D6 |
| 19' | D5 |
| 20' | D4 |
| 21' | D3 |
| 22' | D2 |
| 23' | D1 |
| 24' | D0 |
| 25' | RD(E) |
| 26' | WR(R/W) |
| 27' | A0 |
| 28' | /RES |
| 29' | /CS1 |
| 30' | /DOF |
| 31' | CL |
| 32' | FR |

### Right

| PAD NO. | CONFIGURATION |
|---|---|
| 33' | P/S |
| 34' | C86 |
| 35' | V0 |
| 36' | V1 |
| 37' | V2 |
| 38' | V3 |
| 39' | V4 |
| 40' | CAP2− |
| 41' | CAP2+ |
| 42' | CAP1+ |
| 43' | CAP1− |
| 44' | CAP3+ |
| 45' | VOUT |
| 46' | VSS,SEL3,SEL2, SEL1,/HPM |
| 47' | VDD,VDD2 |
| 48' | D7 |
| 49' | D6 |
| 50' | D5 |
| 51' | D4 |
| 52' | D3 |
| 53' | D2 |
| 54' | D1 |
| 55' | D0 |
| 56' | RD(E) |
| 57' | WR(R/W) |
| 58' | A0 |
| 59' | /RES |
| 60' | /CS1 |
| 61' | /DOF |
| 62' | CL |
| 63' | FR |
| 64' | NC |

## 15. IC LAYOUT DRAWING



## 16. MODULE ACCEPT QUALITY LEVEL (AQL)

16.1 AQL Standard Value: Fatal Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

16.2 Curtailed Inspection Scheme

| Type | Batch Qty | inspection Qty | AQL value | pass | Reject |
|---|---|---|---|---|---|
| Module Product | 350PCS＜ 1000PCS | 125pcs | 0.1 | 0 | 1 |
| | | | 0.65 | 2 | 3 |
| | | | 2.5 | 7 | 8 |
| | 200PCS＜ 350PCS | 80pcs | 0.1 | 0 | 1 |
| | | | 0.65 | 1 | 2 |
| | | | 2.5 | 5 | 6 |
| | ＜200PCS | 32pcs | 0.1 | 0 | 1 |
| | | | 0.65 | 0 | 1 |
| | | | 2.5 | 4 | 5 |
| Module Sample | ＜200PCS | All inspected | / | / | The sample will be reject when the fateful defect＞2pcs or main defect＞5pcs. |
| | ＞200PCS | 125pcs | | | |

**Notes:** 1). Batch QTY is the production amount that Production department ship to QA department.
2). All of product will be inspected if the batch QTY less than inspected QTY.
3). Each batch fixed to be 500pcs.

## 17. RELIABILITY TEST

Operating life time: Longer than 50000 hours
(at room temperature without direct irradiation of sunlight)

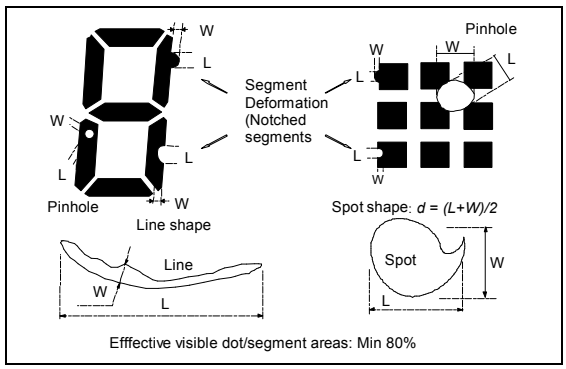
Reliability characteristics shall meet following requirements.

| TEMPERATURE TESTS | NORMAL GRADE |
|---|---|
| High Temperature Storage | +80°C x 96hrs (Without Polarizer) |
| Low Temperature Storage | -30°C x 96hrs |
| High Temperature Operation | +70°C x 96hrs |
| Low Temperature Operation | -20° C x 96hrs |
| High Temperature, High Humidity | +70°C x 95%RH x 96hrs (Without Polarizer) |
| Thermal Shock | -20°C x 30min. ↓ 10s 5Cycles +70°C x 30min. |
| Vibration Test | Frequency x Swing x Time 40Hz x 4mm x 4hrs |
| Drop Test | Drop height x Times 1.0m x 6 times |

## 18. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

a: Table for Cosmetic defects
(Note: nc = not counted).
Sizes and number of defects
(Max. Qty)

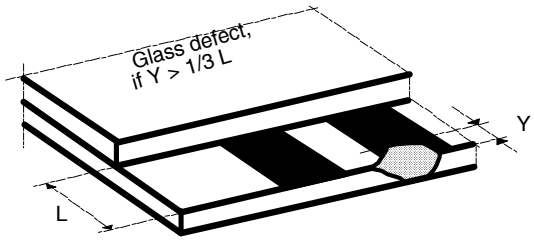



| Defect Type | Max. defect size [μm] d or L | W | Max. Quantity. |
|---|---|---|---|
| Black or White Spots | d ≤ 150 | | nc |
| | 150< d ≤ 300 | | 3 |
| Black or White Lines | -- | W ≤ 10 | nc |
| | L ≤ 3000 | W ≤ 30 | 2 |
| | L ≤ 2000 | W ≤ 50 | 2 |
| Pinhole | d ≤ 150<br>150< d ≤ 300 | | nc<br>1/segment |
| (Total defects) | | | (5) |
| Segment Deformation | | W ≤ 100 | nc |
| Bubble (e.g. under pola) | d ≤ 150 | | nc |
| | 200< d ≤ 400 | | 2 |

Examples/ Shapes

b: Glass defects

b1:Glass defects at contact ledge




b2:Glass chipping in other areas shall not be in conflict with the product's function.

## 19. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

## 20. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections