Display Elektronik GmbH

DATA SHEET

TFT MODULE

DEM 7201280A

VMH-PW-N (C-TOUCH)

5“ TFT + PCT

Product Specification **Ver.: 0**

28.11.2017

Revision History

VERSION	DATE	REVISED PAGE NO.	Note
0	28.11.2017		First Issue

Contents

1. Summary

2. General Specification

3. Interface

4. Counter Drawing

5. Absolute Maximum Ratings

6. Electrical Characteristics

7. DC Characteristics

8. AC Characteristics

9. Power ON/OFF Sequence

10. Optical Characteristics

11. Reliability

12. Touch Panel Information

1. Summary

This 5.0” TFT is a color active matrix thin film transistor (IPS) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 4.99 (16:9) inch diagonally measured active display area with HD (720 horizontal by 1280 vertical pixel) resolution. This module is a composed of a TFT_LCD module and follows RoHS.

2. General Specifications

- Size: 5.0 Inch
- Dot Matrix: 720 x RGB x 1280 Dots
- Module Dimension: 73.30 x 127.60 x 3.45 mm
- Active Area: 62.10 x 110.40 mm
- Dot Pitch: 0.08625 x 0.08625 mm
- LCD Type: IPS TFT, Normally Black, Transmissive
- Viewing Angle: 80/80/80/80
- Aspect Ratio: 16:9
- Backlight Type: LED ,Normally White
- Brightness: 200cd/m2 (in front of the touch)
- CTP IC: GT928 (Goodix)
- With / Without TP: With Capacitive Touch and I2C-Interface
- Surface: Glare

*Color tone slight changed by temperature and driving voltage.

3. Interface

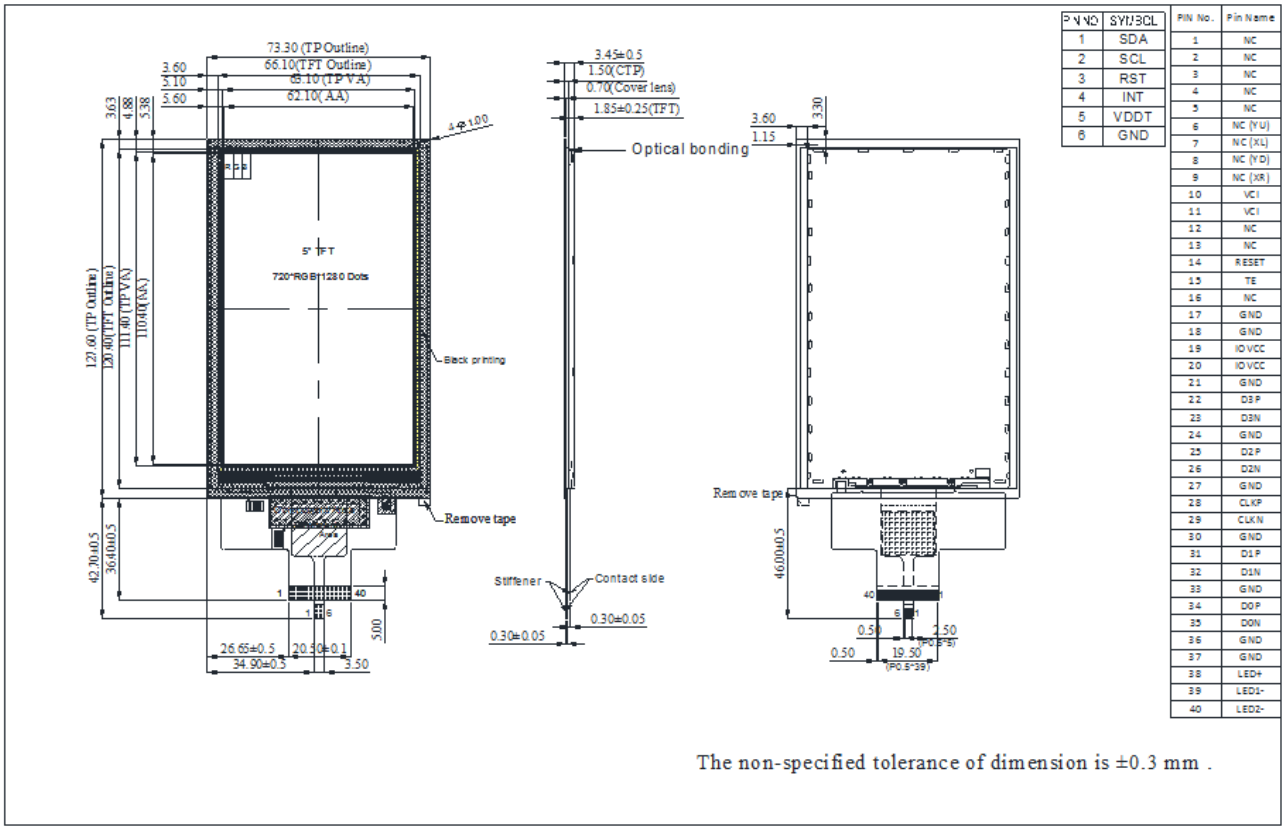
3.1. LCM PIN Definition

Pin	Symbol	Function	Remark
1	NC	No connection	
2	NC	No connection	
3	NC	No connection	
4	NC	No connection	
5	NC	No connection	
6	NC	No connection	
7	NC	No connection	
8	NC	No connection	
9	NC	No connection	
10-11	VCI	Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.6V	
12-13	NC	No connection	
14	RESET	The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. Fix to VDDI level when not in use.	
15	TE	Tearing effect output pin. Leave the pin open when not in use.	
16	NC	No connection	
17-18	GND	Power ground	
19-20	IOVCC	Power supply for analog circuits. Connect to an external power supply of 1.65V to 3.6V	
21	GND	Power ground	
22	D3P	MIPI DSI differential data pair. (Data lane 3)	
23	D3N		
24	GND	Power ground	
25	D2P	MIPI DSI differential data pair. (Data lane 2)	
26	D2N		
27	GND	Power ground	
28	CLKP	MIPI DSI differential clock pair	
29	CLKN		
30	GND	Power ground	
31	D1P	MIPI DSI differential data pair. (Data lane 1)	
32	D1N		
33	GND	Power ground	
34	D0P	MIPI DSI differential data pair. (Data lane 0)	
35	D0N		
36-37	GND	Power ground	
38	LED+	Power for LED backlight anode	
39	LED1-	Power for LED1 backlight cathode	
40	LED2-	Power for LED2 backlight cathode	

3.2. CTP PIN Definition

Pin	Symbol	Function	Remark
1	SDA	I2C data input and output	
2	SCL	I2C clock input	
3	RST	External Reset, Low is active	
4	INT	External interrupt to the host	
5	VDD	Power Supply : +3.3V	
6	GND	Ground for analog circuit	

4. Counter Drawing



PIN NO	SYMBOL
1	SDA
2	SCL
3	RST
4	INT
5	VDDT
6	GND

PIN No.	Pin Name
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC (YU)
7	NC (XL)
8	NC (YD)
9	NC (XR)
10	VCI
11	VCI
12	NC
13	NC
14	RESET
15	TE
16	NC
17	GND
18	GND
19	IOVCC
20	IOVCC
21	GND
22	D3P
23	D3N
24	GND
25	D2P
26	D2N
27	GND
28	CLKP
29	CLKN
30	GND
31	D1P
32	D1N
33	GND
34	D0P
35	D0N
36	GND
37	GND
38	LED+
39	LED1-
40	LED2-

5. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	°C
Storage Temperature	T_{ST}	-30	—	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60°C, 90% RH MAX. Temp. ＞60°C,
   Absolute Humidity shall be less than 90% RH at 60°C

6. Electrical Characteristics

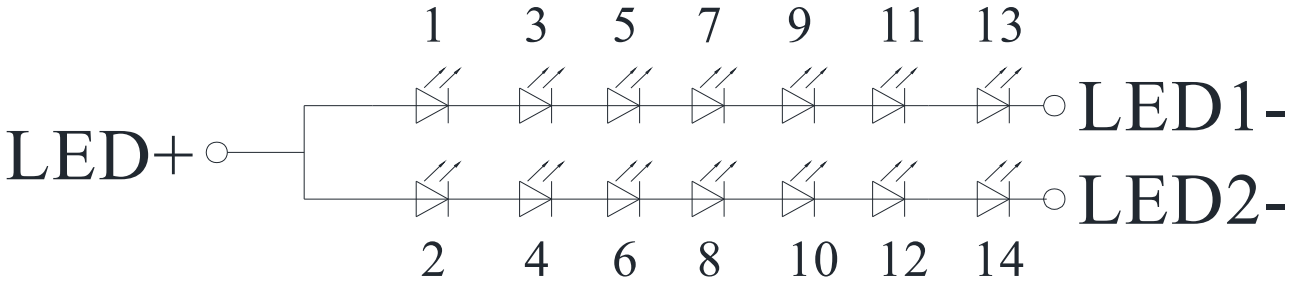
6.1. Typical Operation Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Supply for Analog Circuit	VCI	2.5	3.3	3.6	V	
Power Supply for Logic Circuit	IOVCC	1.65	1.8	3.6	V	
Supply Voltage for Touch Logic	VDDT	2.8	-	3.3	V	
Current for Driver	IDD	-	44	-	mA	VDD=3.3V Note1

6.2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	ILED	-	40	-	mA	
LED Voltage	VLED+	19.6	-	23.8	V	Note 1
LED Lifetime		30,000	-	-	Hr	Note 2,3,4

Note 1: There are 1 Groups LED



Note 2: Ta = 25°C
Note 3: Brightness to be decreased to 50% of the initial value
Note 4: The single LED lamp case7.3.

7. DC CHARATERISTICS

7.1. Basic Characteristics for Panel Driving

Parameter	Symbol	Rating			Unit	Condition	Note
		Min	Typ	Max			
Logic Low Level Input Voltage	V_{IL}	-0.3	-	0.3*IOVCC	V		Note1
Logic High Level Input Voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V		Note1
Logic Low Level Output Voltage (TE)	V_{OL}	0		0.2*IOVCC	V	I_{OL}= +1.0mA	Note1
Logic High Level Output Voltage (TE)	V_{OH}	0.8*IOVCC		IOVCC	V	I_{OH}= -1.0mA	Note1

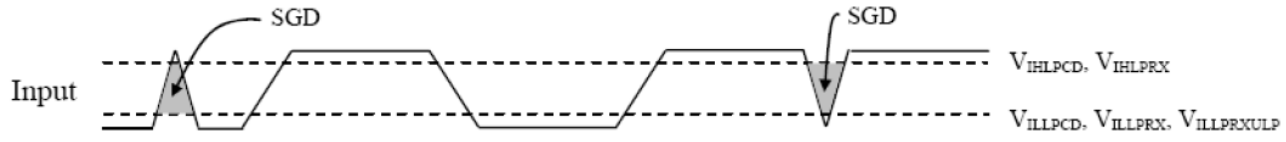
NOTE1:
Ta = -20°C to 70°C, VCI = 2.5V to 3.6V, IOVCC = 1.65V to 3.6V

7.2. DSI DC Characteristics

LP Mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

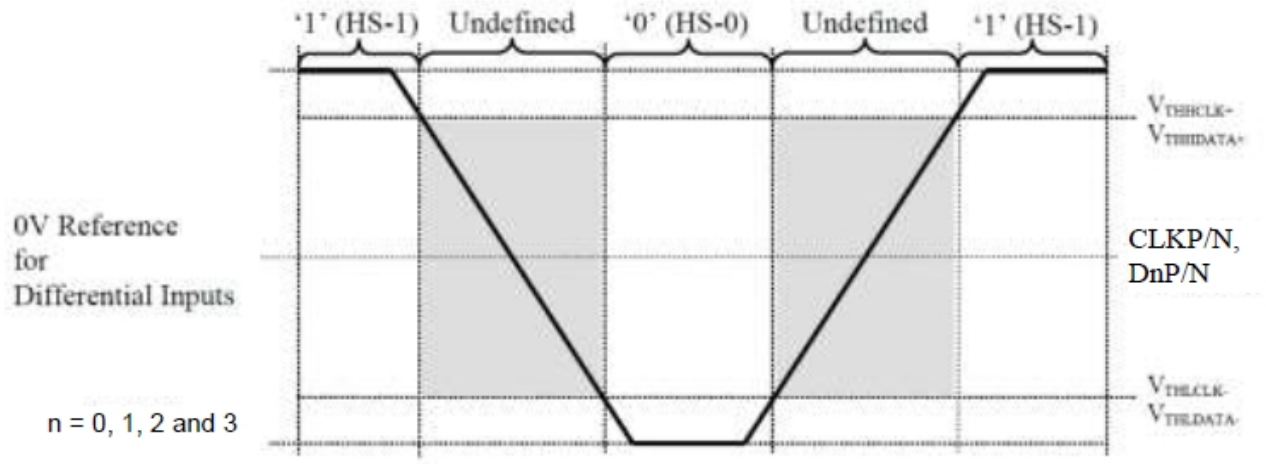
Spike/Glitch Rejection

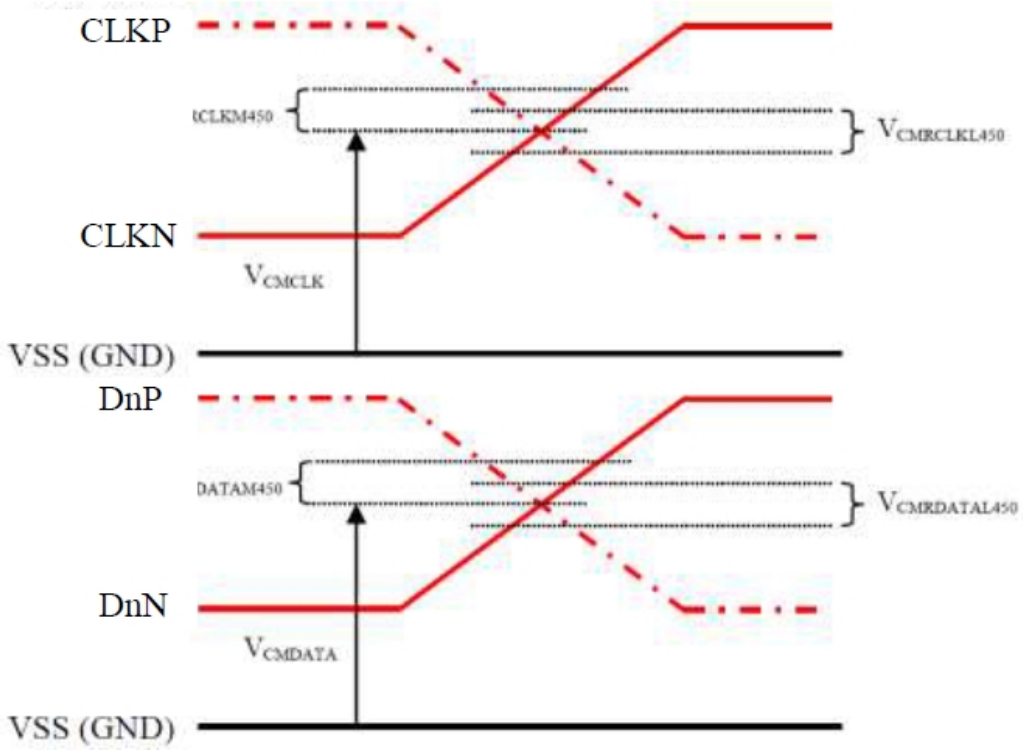


Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

High Speed Mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF



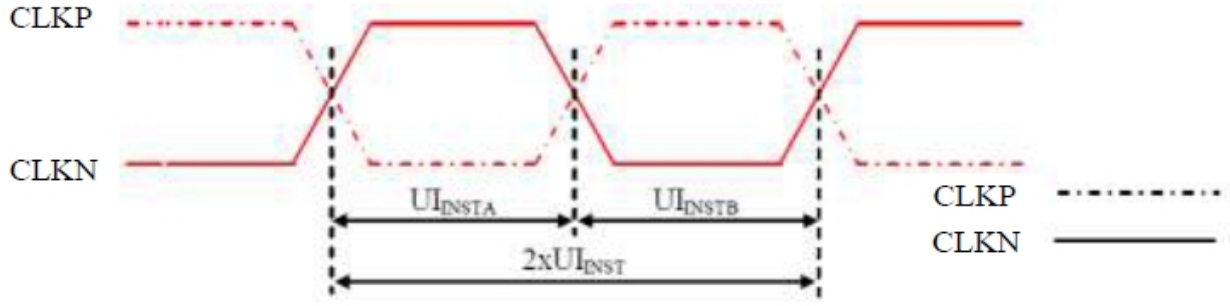


Note: *n = 0, 1, 2 and 3*

8. AC Characteristics

8.1. DSI Interface Timing Characteristics

8.1.1 High Speed Mode – Clock Channel Timing



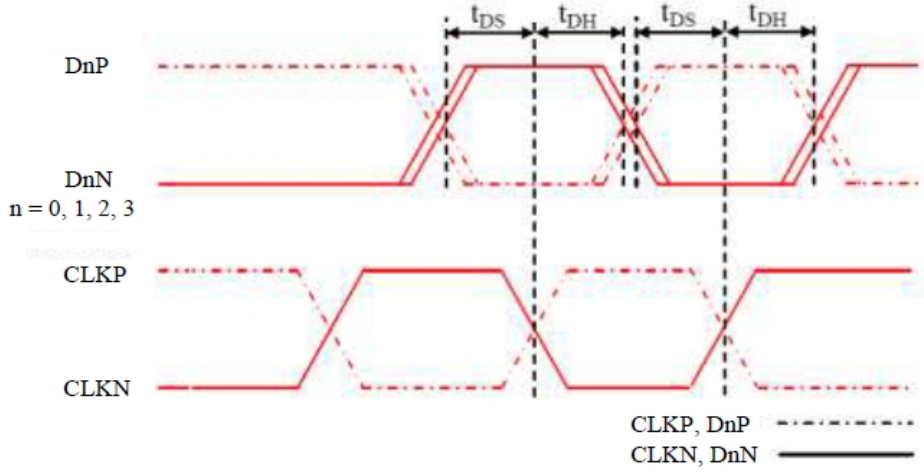
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

8.1.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

8.1.3 High Speed Mode – Rising and Falling Timings

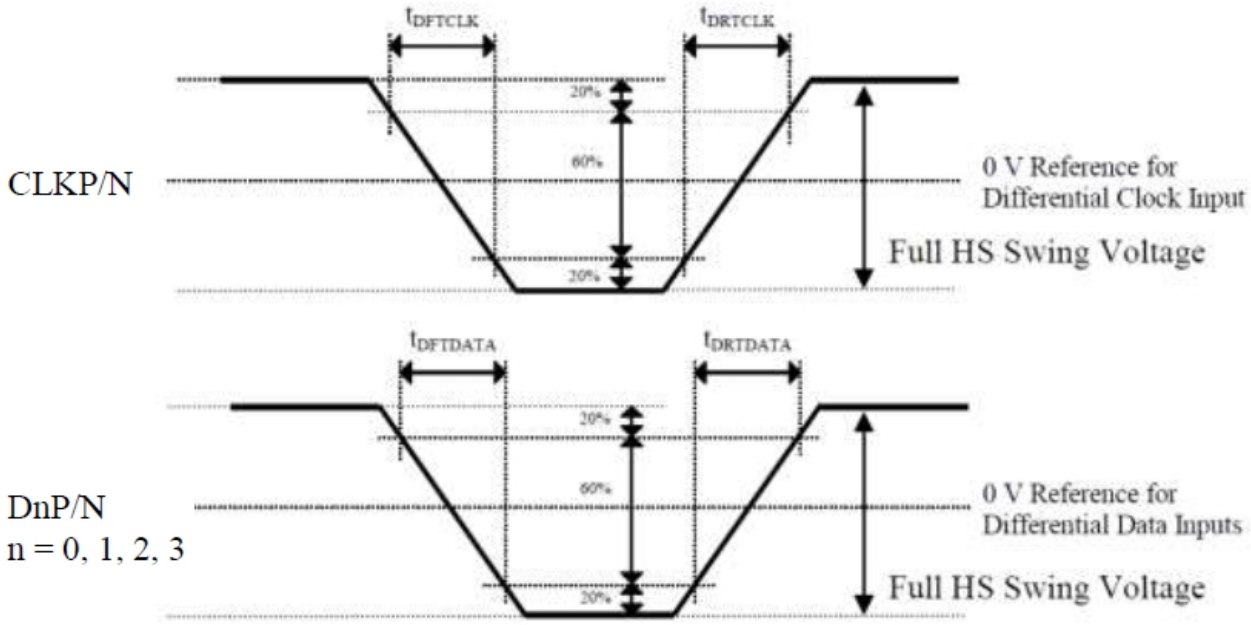
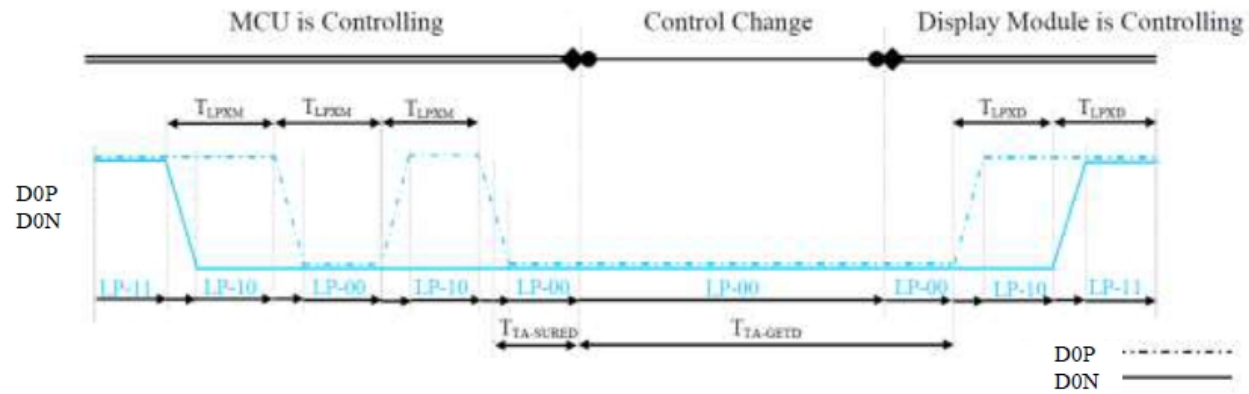


Table 41: Rise and Fall Timings on Clock and Data Channels

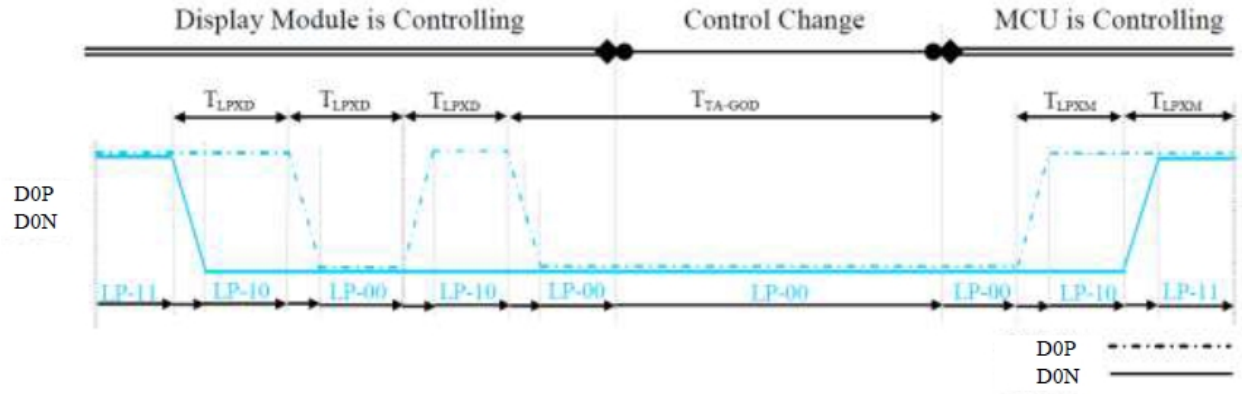
Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

8.1.4 Low Power Mode – Bus Turn Around



BTA from the MCU to Display Module

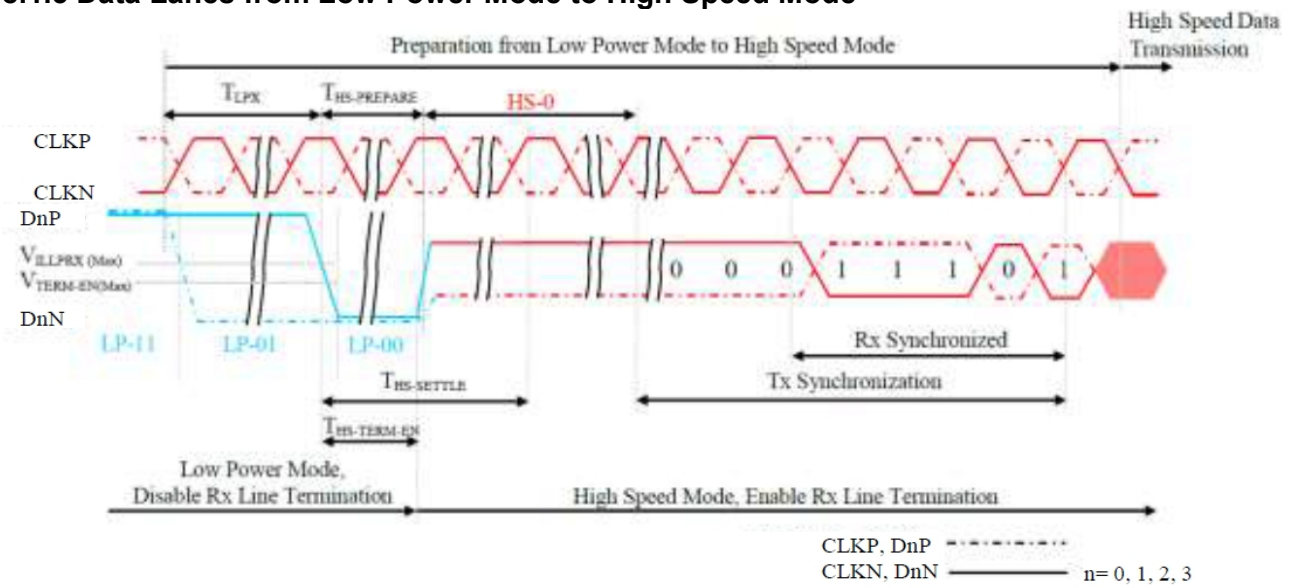


BTA from Display Module to the MCU

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

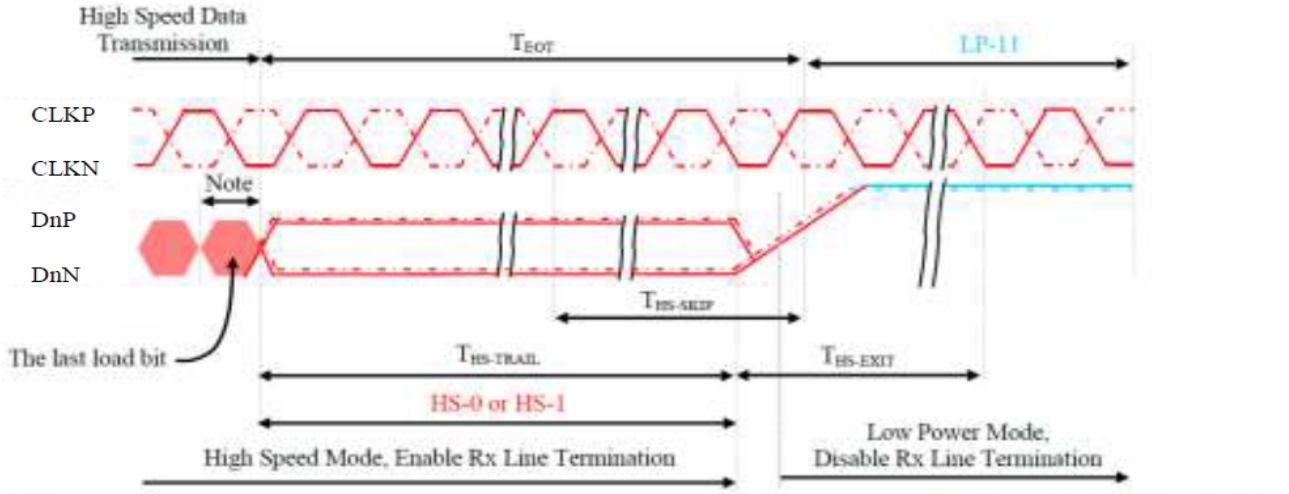
Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

8.1.5 Data Lanes from Low Power Mode to High Speed Mode



Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

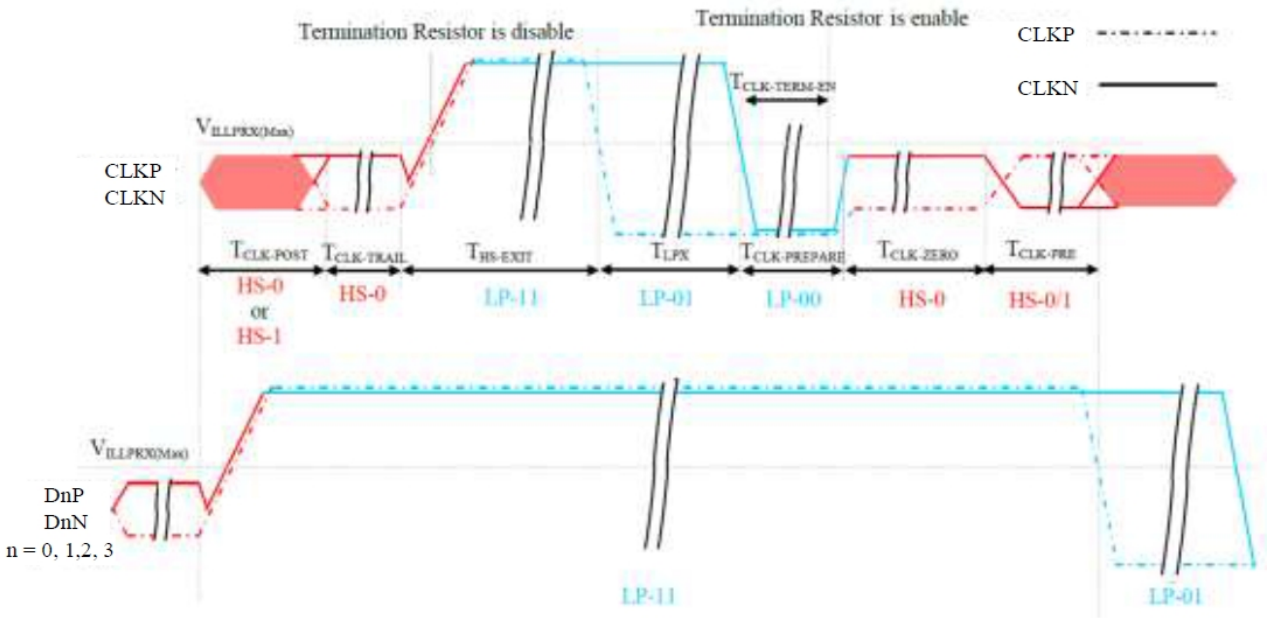
8.1.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

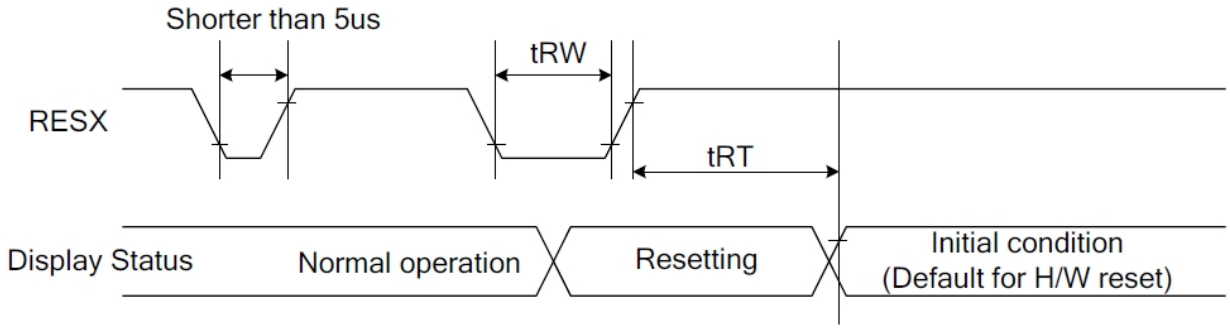
Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

8.1.7 Clock Lanes High Speed Mode to/from Low Power Mode Timing



Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

8.2. Reset Timing

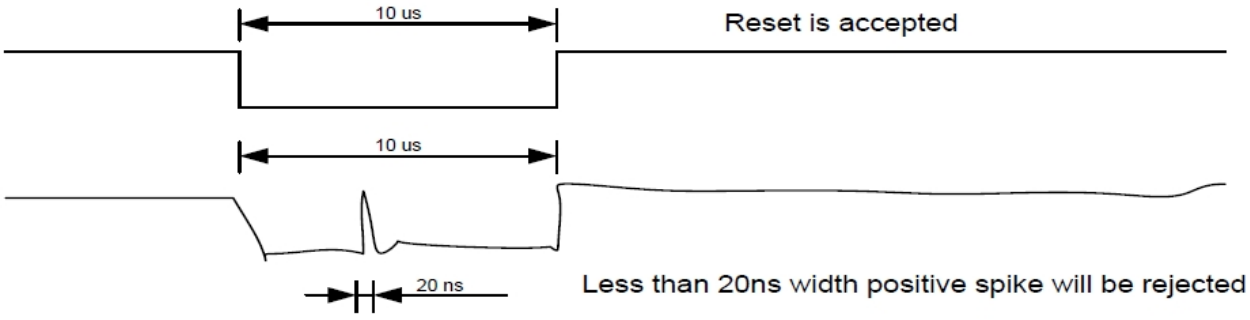


Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	

Notes:
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

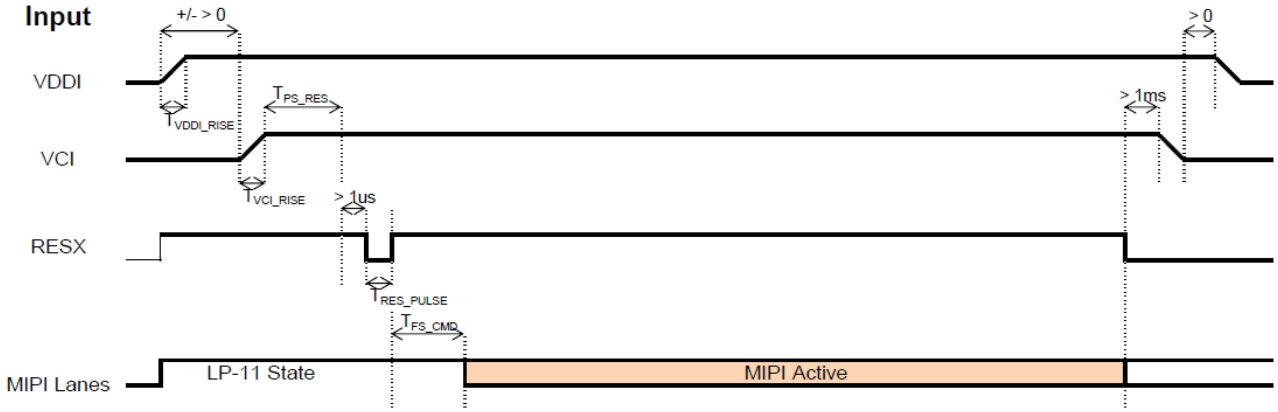
3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



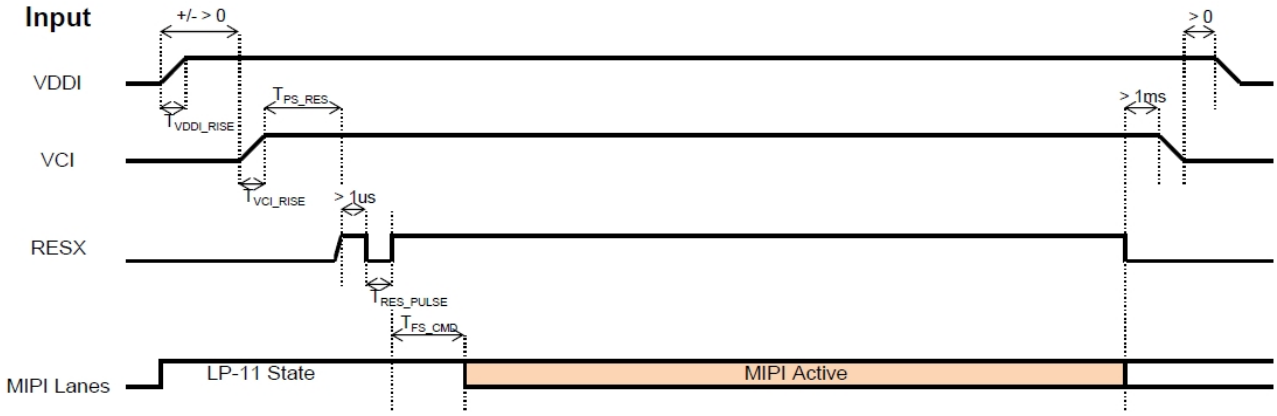
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9. Power ON/OFF Sequence

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

10. Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response Time		Tr	θ=0°、Φ=0°	-	10	15	.ms	Note 3,5
		Tf		-	20	25	.ms	
Contrast Ratio		CR	At optimized viewing angle	640	800	-	-	Note 4,5
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.283	0.303	0.323		Note 2,6,7
		Wy		0.303	0.323	0.343		
Viewing Angle	Hor.	ΘR	CR≧10	-	80	-	Deg.	Note 1
		ΘL		-	80	-		
	Ver.	ΦT		-	80	-		
		ΦB		-	80	-		
Brightness		-	-	200	-	-	cd/m^2	Center of display

Ta=25°C±2°C

Note 1: Definition of viewing angle range

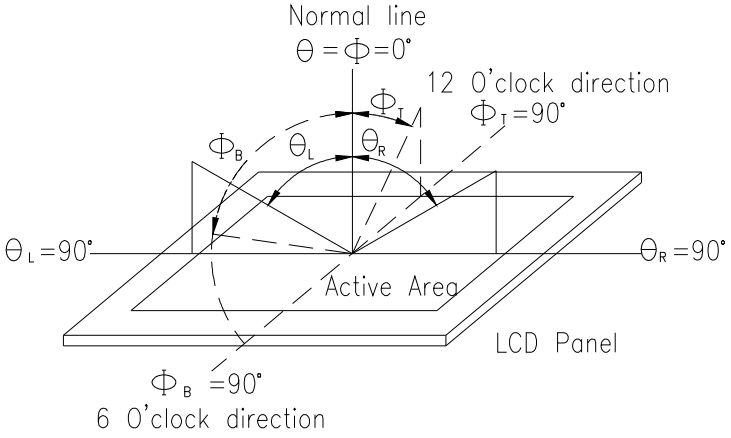


Fig. 11.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

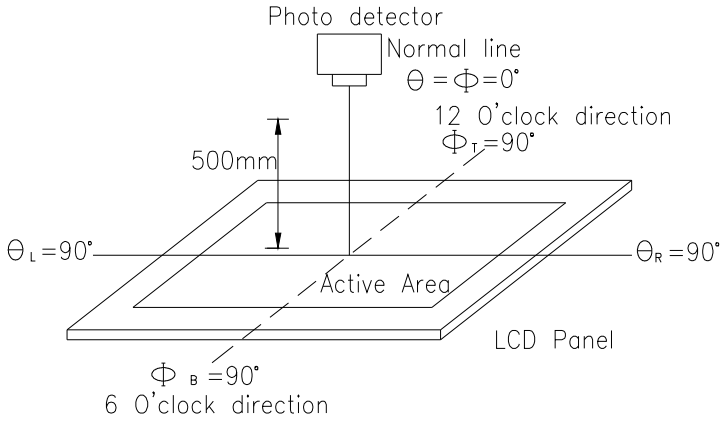
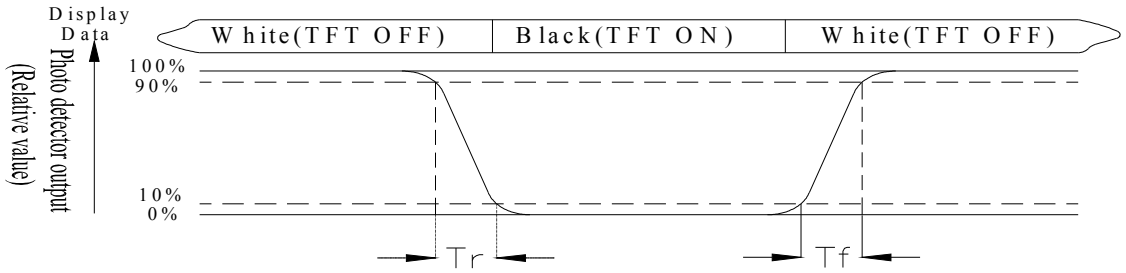


Fig. 11.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

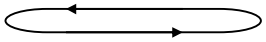
Note 5: White Vi = Vi50 ± 1.5V
Black Vi = Vi50 ± 2.0V
"±" means that the analog input signal swings in phase with VCOM signal.
"±" means that the analog input signal swings out of phase with VCOM signal.
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

11. Reliability

Content of Reliability Test (Wide temperature, -20°C~+70°C)

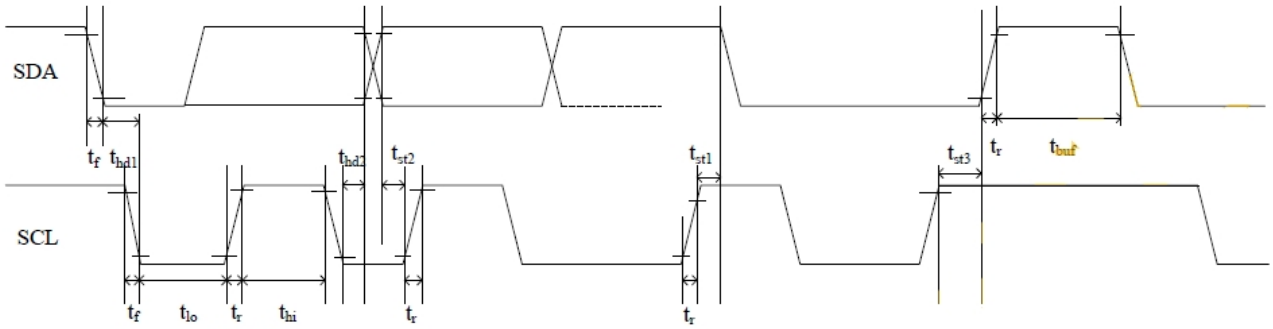
Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	+70°C 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60□,90%RH max	+60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20°C +25°C +70°C  30min 5min 30min 1 cycle	-20°C/+70°C 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(Contact), ±800V(Air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.

12. Touch Panel Information

12.1. I2C Communication

GT928 provides standard I2C interface for communication. In the system, GT928 always works in slave mode, all communications are initiated by master, and the baud rate can be up to 400K bps. The definition of I2C timing is as following:



Test condition1: 1.8V communication interface, 400Kbps, pull up resistor is 2K ohm

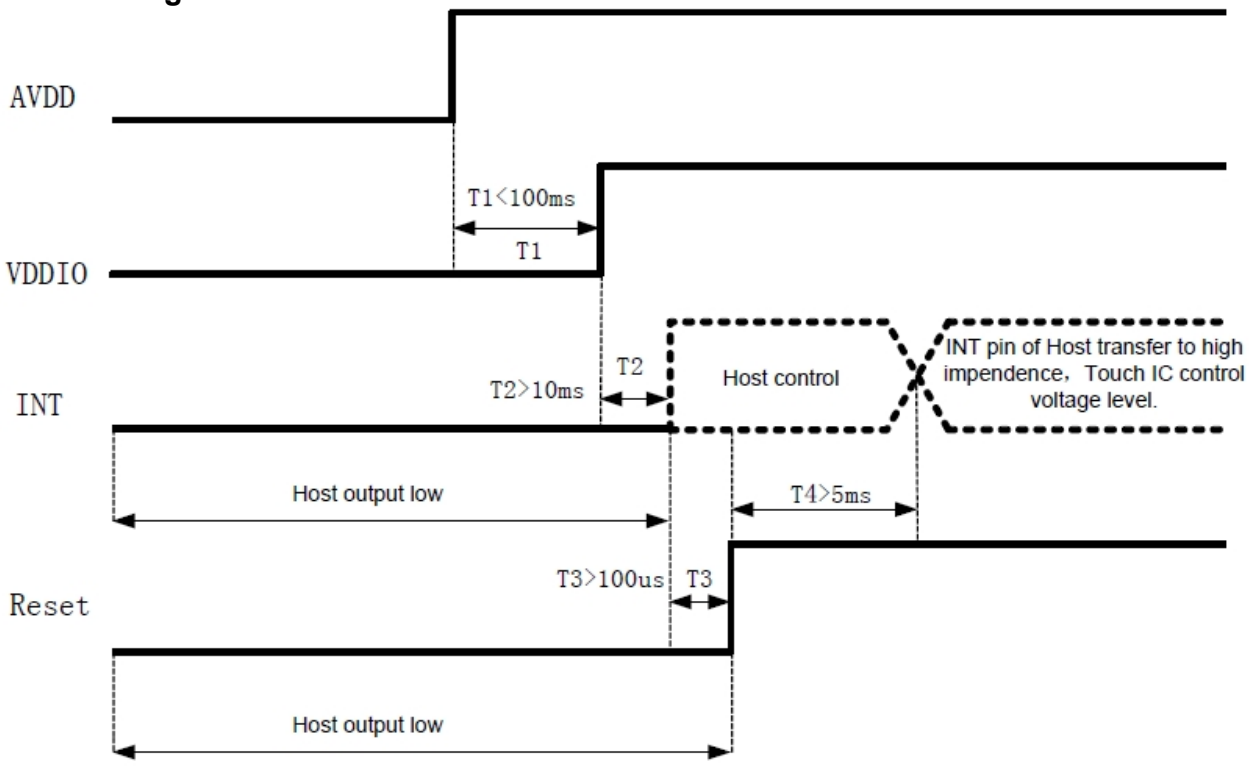
Parameter	Symbol	Min.	Max.	Unit
SCL low period	Tlo	0.9	-	us
SCL high period	Thi	0.8	-	us
SCL setup time for START condition	tst1	0.4	-	us
SCL setup time for STOP condition	tst3	0.4	-	us
SCL hold time for START condition	thd1	0.3	-	us
SDA setup time	tst2	0.4	-	us
SDA hold time	thd2	0.4	-	us

Test condition2: 3.3V communication interface, 400Kbps, pull up resistor is 2K ohm

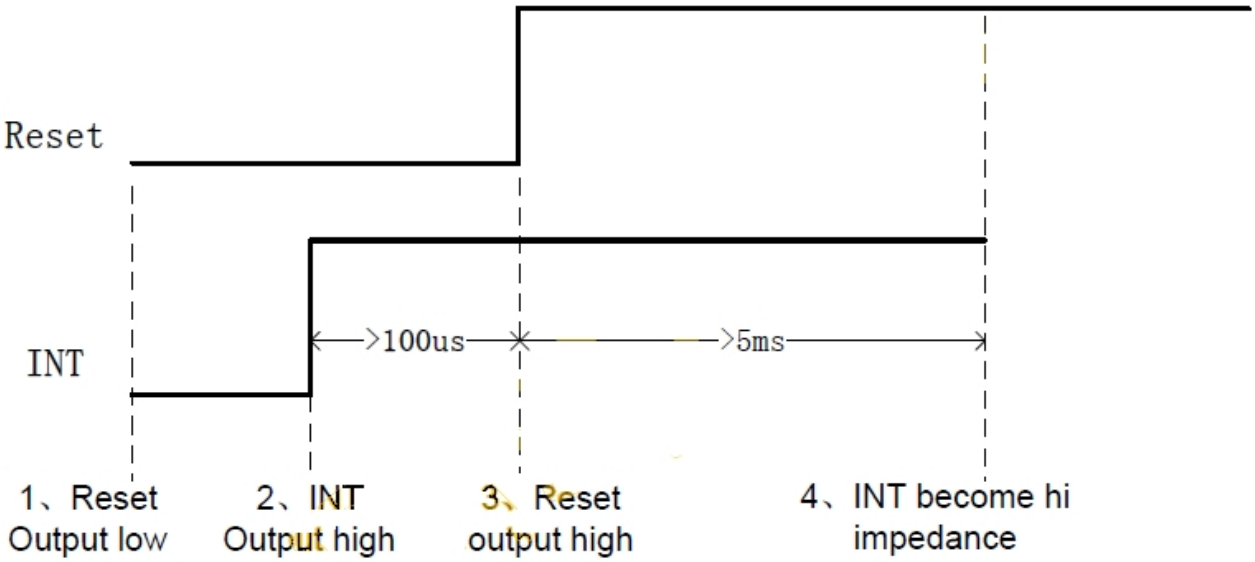
Parameter	Symbol	Min.	Max.	Unit
SCL low period	Tlo	0.9	-	us
SCL high period	Thi	0.8	-	us
SCL setup time for START condition	tst1	0.4	-	us
SCL setup time for STOP condition	tst3	0.4	-	us
SCL hold time for START condition	thd1	0.3	-	us
SDA setup time	tst2	0.4	-	us
SDA hold time	thd2	0.4	-	us

GT928 has 2 sets of slave address 0xBA/0xBB & 0x28/29. Master can control Reset & INT pin to configure the slave address in power on initial state like following：

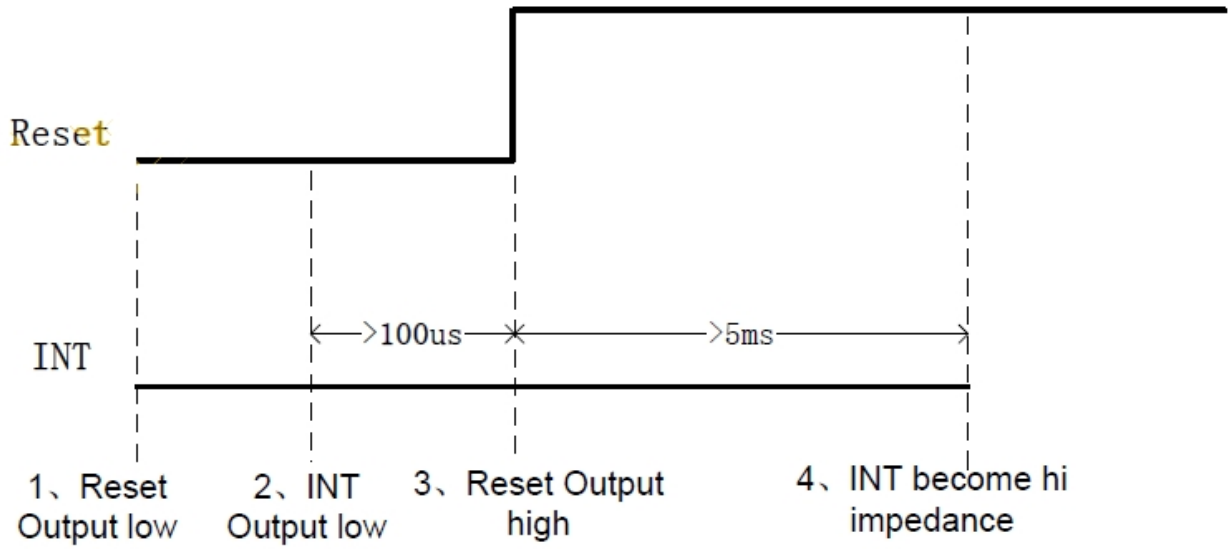
Power on diagram:



Timing of setting slave address to 0x28/0x29:



Timing of setting slave address to 0xBA/0xBB:



a) Data Transmission

(eg. slave address is 0xBA/0xBB)

Communication is always initiated by master, A high-to-low transition of SDA with SCL high is a start condition.

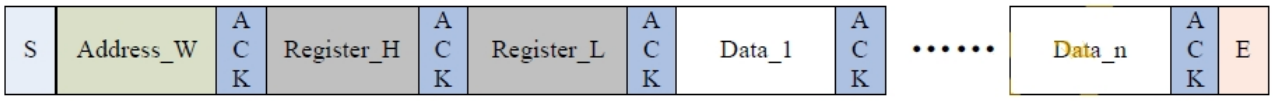
All addressing signal are serially transmitted to and from on bus in 8-bit word. GT928 sends a "0" to acknowledge when the addressing word is 0xBA/BB(or 0x28/0x29). This happens during the ninth clock cycle. If the slave address is not matched, GT928 will stay in idle state.

The data words are serially transmitted to and from in 9-bit information: 8-bit data + 1-bit ACK or NACK sent by GT928. Data changes during SCL low periods and keep valid during SCL high.

A low-to-high transition of SDA with SCL high is a stop condition.

b) Write Data to GT928

(eg. slave address is 0xBA/0xBB)



Write operations

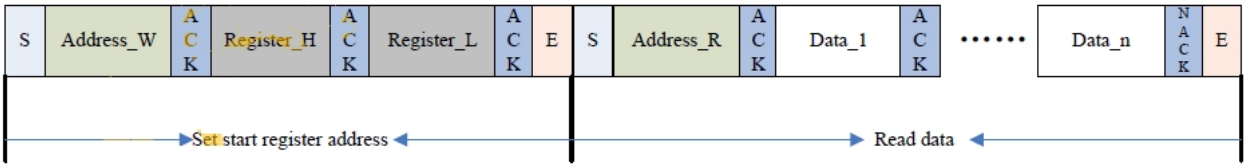
Please check the above figure, master start the communication first, and then sends device address 0XBA preparing for a write operation.

After receiving ACK from GT928, master sends out 16-bit register address, and then the data word in 8-bit, which is going to be wrote into GT928.

The address pointer of GT928 will automatically increase one after one byte writing, so master can sequentially write in one operation. When operation finished, master stop the communication.

c) Read Data from GT928

(eg. slave address is 0xBA/0xBB)



Read operation

Please check the above figure, master start the communication first, and then sends device address 0xBA for a write operation.

After receiving ACK from GT928, master sends out 16-bit register address, to set the address pointer of GT913. After receiving ACK, master produce start signal once again and send device address 0xBB, then read data word from GT928 in 8-bit.

GT928 also supports sequential read operation, and the default setting is sequential read mode. Master shall send out ACK after every byte reading successfully but NACK after the last one. Then sends stop signal to finish the communication