Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128128C3 - RGB

Product Specification ***Version : 01***

19.11.2009

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2009/11/19	SPEC.

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128xRGBx128	dots
Module dimension (L*W*H)	33.5*71.5*1.625(MAX)	mm
Active area	26.279*26.284	mm
Dot size	0.0435(W)x0.1855(H)	mm
Dot pitch	0.0685(W)x0.2055 (H)	mm

(2) Controller IC: SSD1351 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage	VI	0.3	—	4.0	V
Operating lifetime			14000(*)		Hrs

*:70cd/m^2 light on

**:Ta=25℃,50%RH

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	3.3	3.5	V
Supply Voltage For Analog	Vcc-V_{SS}	—	16	16.5	17	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	—	—	TBD	—	mA

5. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧20	85		85	deg
	(H) φ	CR≧20	85		85	deg
Contrast Ratio	CR	—		100		—
Response Time 25℃	T rise	—		40		ms
	T fall	—		40		ms

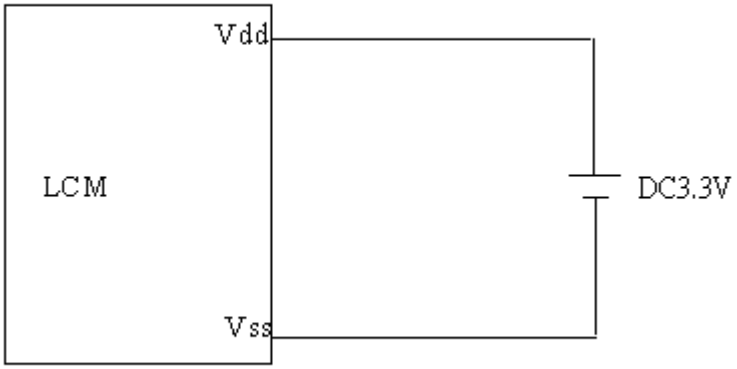
6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	RW	H/L	8080: data write enable pin 6800: Read/Write select pin
7	E	H/L	8080: data read enable pin 6800: Read/Write enable pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISPOFF/ VCC	— H/L	DISPOFF: Active L VCC: Analog power control (DC 17V)

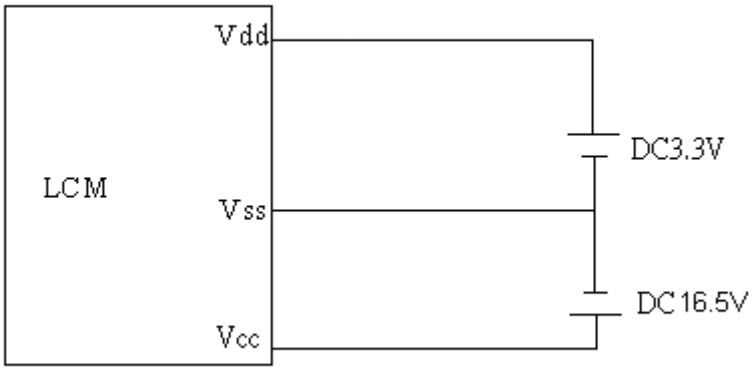
Default:8080 series interface

7. Power supply for LCD Module

＊LCM operating on "DC 3V " input with built-in positive voltage



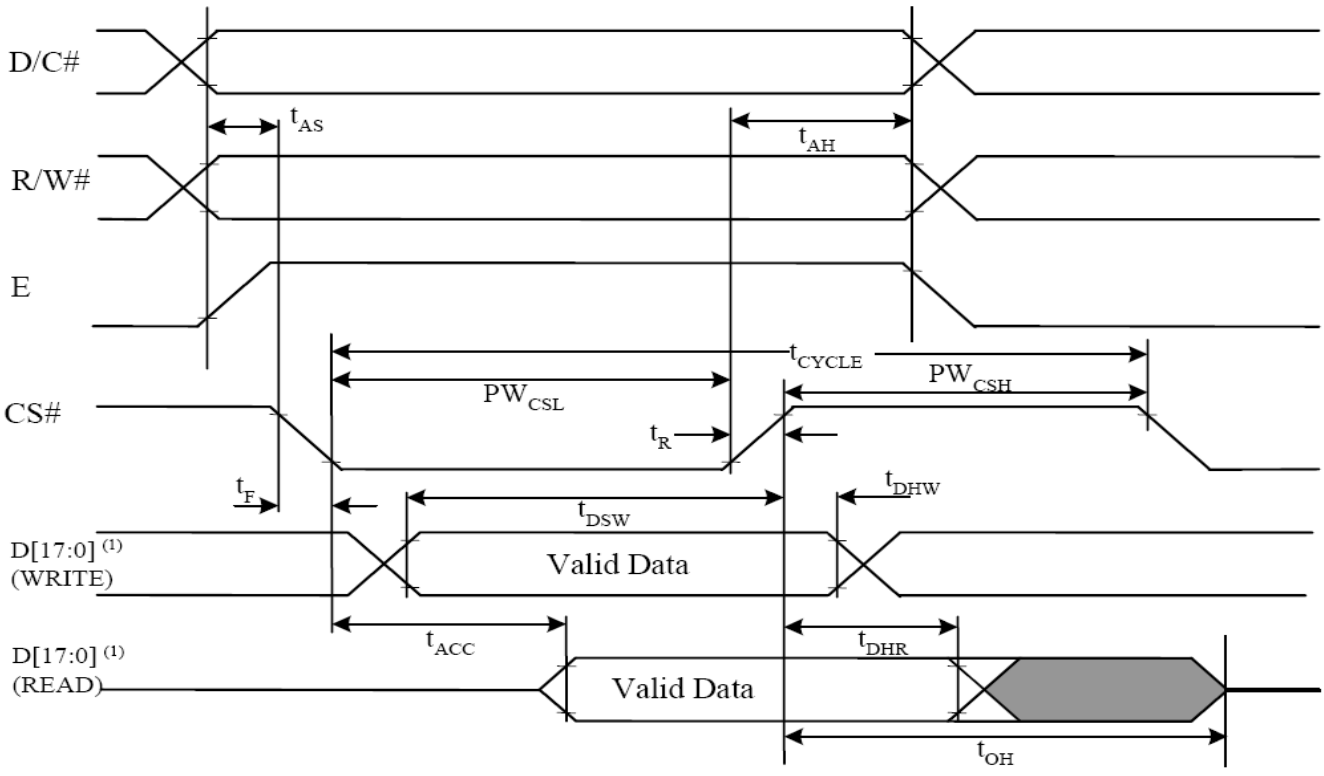
＊(Optional) LCM operating on " DC 3V " input with external positive voltage.



8. Timing Characteristics

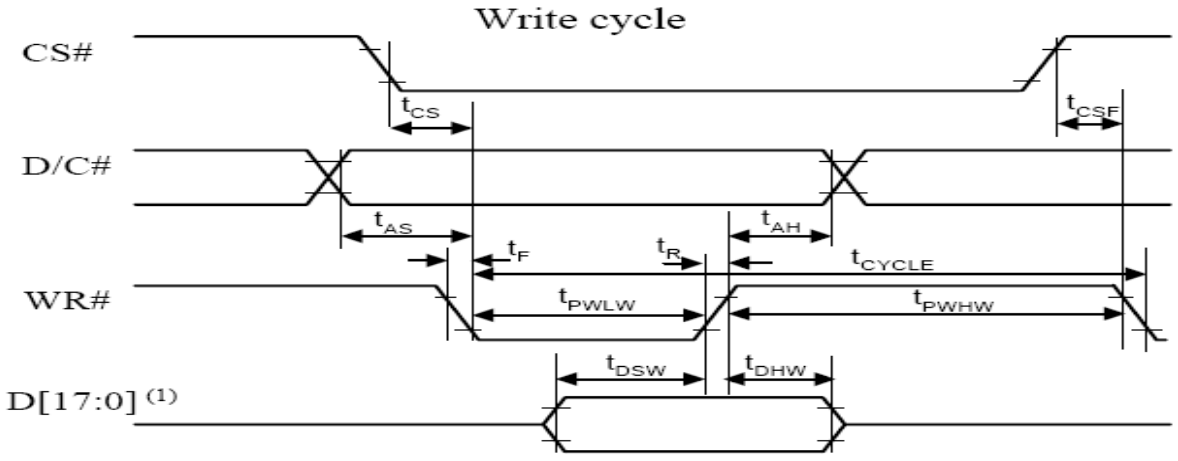
8-1.6800 MPU Interface

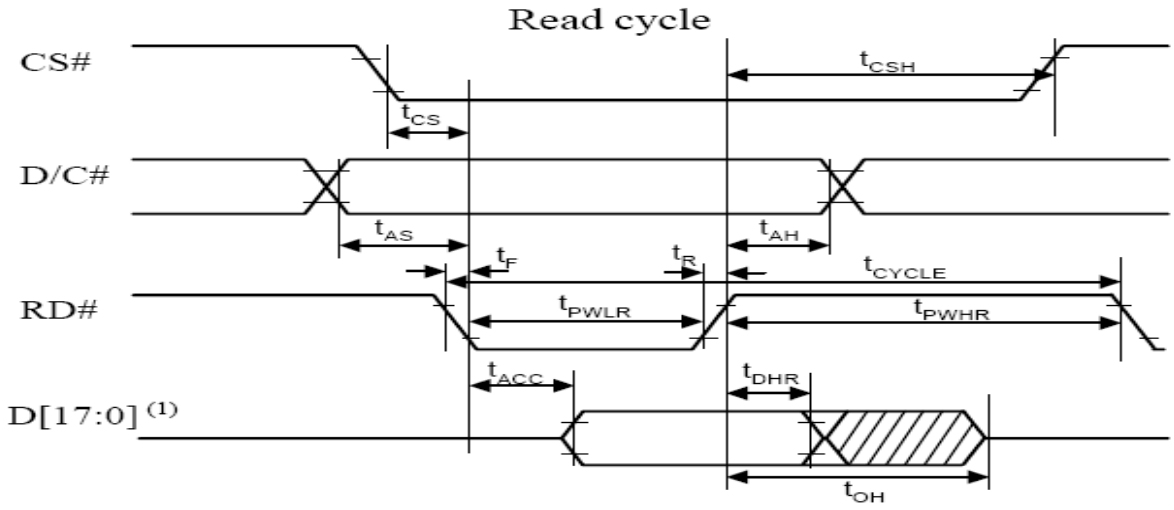
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8-2.8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns





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9. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

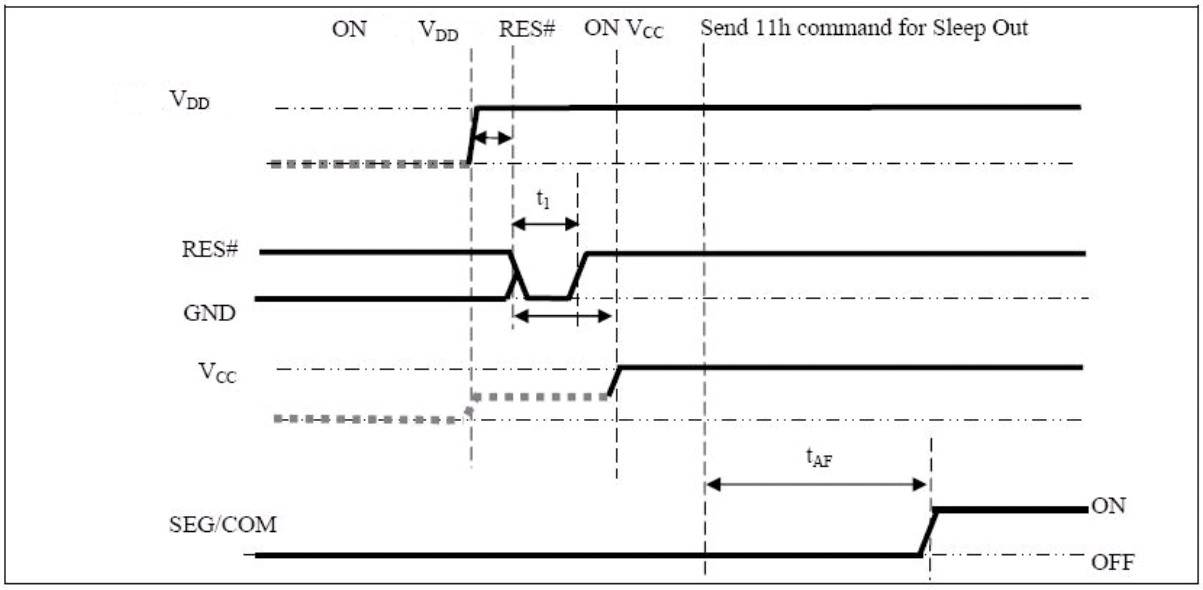
9.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

8.1.1 Power ON Sequence

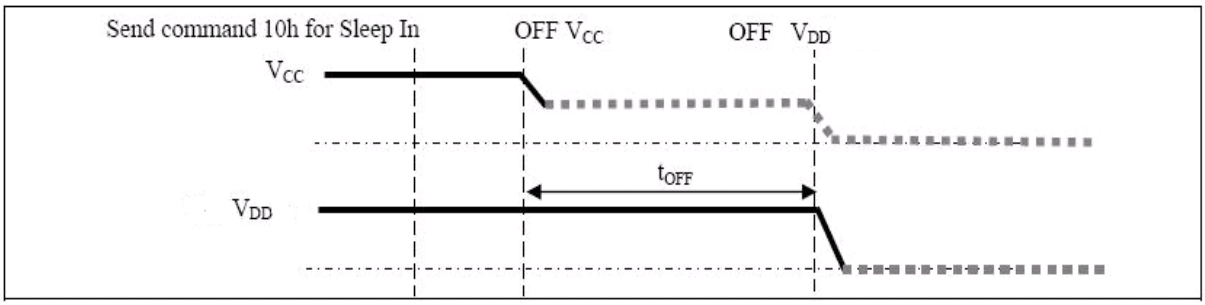
1. Power ON VCI,VDDIO,
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable.

   Then set RES# pin LOW (logic low) for at least 2us (t1)(4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t2). Then Power ON VCC. (1)
4. After VCC become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms (tAF).



8.1.2 Power OFF Sequence

1. Send command AEh for display OFF.
2. Power OFF VCC. (1), (2)
3. Wait for tOFF. Power OFF VDD (where Minimum tOFF=80ms (3),Typical tOFF=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI,VDDIO and VCC,VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
(2) VCC should be disabled when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins(VDDIO, VCC) can never be pulled to ground under any circumstance.

9.2 COMMAND TABLE

Refer to IC Spec.: SSD1351

9.3 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128x128x18bits. For mechanical flexibility , re-mapping on both Segment and Common outputs can be selected by software . Each pixel has 18-bitdata. Each sub-pixels for color A, B and C have 6bits.The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	126	127			
	Remapped	127			126			125	.....	.....	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6	COM6
7	120								.....	.....	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6	:
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

10. Appendix (Drawing)