

## AT45DB041E

2-Mbit DataFlash (with Extra 64 kBits) 1.65 V Minimum SPI Serial Flash Memory

### Features

- Single 1.65 V - 3.6 V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports RapidS™ operation
- Continuous read capability through entire array
  - Up to 85 MHz
  - Low-power read option up to 15 MHz
  - Clock-to-output time ( $t_V$ ) of 6 ns maximum
- User-configurable page size
  - 256 bytes per page
  - 264 bytes per page (default)
  - Page size can be factory pre-configured for 256 bytes
- Two fully independent SRAM data buffers (256/264 bytes)
  - Allows receiving data while reprogramming the main memory array
- Flexible programming options
  - Byte/Page Program (1 to 256/264 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase (256/264 bytes)
  - Block Erase (2 kB)
  - Sector Erase (64 kB)
  - Chip Erase (4 Mbits)
- Program and Erase Suspend/Resume
- Advanced hardware and software data protection features
  - Individual sector protection
  - Individual sector lockdown to make any sector permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low-power dissipation
  - 400 nA Ultra-Deep Power-Down current (typical)
  - 3  $\mu$ A Deep Power-Down current (typical)
  - 25  $\mu$ A Standby current (typical)
  - 7mA Active Read current (typical @ 15 MHz))
- Endurance:
  - 100,000 program/erase cycles (-40°C to +85°C)
  - 10,000 program/erase cycles (-40°C to +125°C)
- Data retention: 20 years
- Complies with full industrial temperature range
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.150" wide and 0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)
  - 8-ball Ultra-thin UBGA (6 x 6 x 0.6mm)
  - Die in Wafer Form (contact factory for availability)

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## 1. Description

The AT45DB041E is a 1.65 V minimum, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT45DB041E also supports the RapidS serial interface for applications requiring very high speed operation. Its 4,194,304 bits of memory are organized as 2,048 pages of 256 bytes or 264 bytes each. In addition to the main memory, the AT45DB041E also contains two SRAM buffers of 256/264 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Interleaving between both buffers can dramatically increase a system's ability to write a continuous data stream. Also, the SRAM buffers can be used as additional system scratch pad memory, and E<sup>2</sup>PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation.

Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash<sup>®</sup> uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, the AT45DB041E does not require high input voltages for programming. The device operates from a single 1.65 V to 3.6 V power supply for the erase and program and read operations. The AT45DB041E is enabled through the Chip Select pin ( $\overline{CS}$ ) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

## 2. Pin Configurations and Pinouts

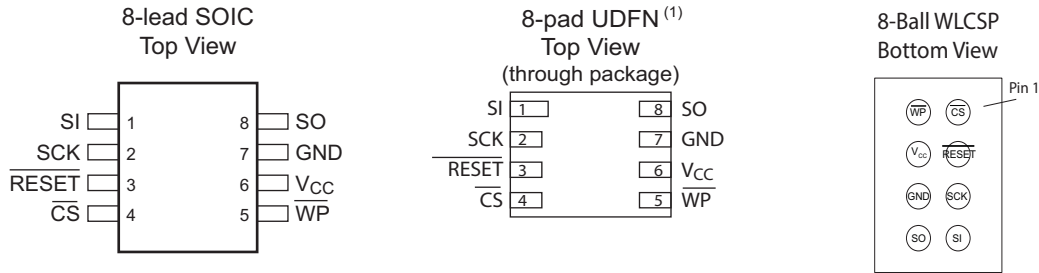


Figure 1. Pinouts

NOTES:

1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.
2. Contact Renesas Electronics for manufacturing flow and availability.

Table 1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	<p><b>Chip Select:</b> Asserting the <math>\overline{CS}</math> pin selects the device. When the <math>\overline{CS}</math> pin is deasserted, the device is deselected and normally be placed in the standby mode (not Deep Power-Down mode) and the output pin (SO) is in a high-impedance state. When the device is deselected, data is not be accepted on the input pin (SI).</p> <p>A high-to-low transition on the <math>\overline{CS}</math> pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device does not enter the standby mode until the operation is done.</p> <p>To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from <math>\overline{CS}</math> to <math>V_{CC}</math>. This ensures <math>\overline{CS}</math> ramps together with <math>V_{CC}</math> during power-up.</p>	Low	Input
SCK	<p><b>Serial Clock:</b> This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.</p>	—	Input
SI	<p><b>Serial Input:</b> The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK. Data present on the SI pin is ignored whenever the device is deselected (<math>\overline{CS}</math> is deasserted).</p>	—	Input
SO	<p><b>Serial Output:</b> The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected (<math>\overline{CS}</math> is deasserted).</p>	—	Output
$\overline{WP}$	<p><b>Write Protect:</b> When the <math>\overline{WP}</math> pin is asserted, all sectors specified for protection by the Sector Protection Register are protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The <math>\overline{WP}</math> pin functions independently of the software controlled protection method. After the <math>\overline{WP}</math> pin goes low, the contents of the Sector Protection Register cannot be modified.</p> <p>If a program or erase command is issued to the device while the <math>\overline{WP}</math> pin is asserted, the device ignores the command and performs no operation. The device returns to the idle state once the <math>\overline{CS}</math> pin has been deasserted. The Enable Sector Protection command and the Sector Lockdown command, however, are recognized by the device when the <math>\overline{WP}</math> pin is asserted.</p> <p>The <math>\overline{WP}</math> pin is internally pulled-high and can be left floating if hardware controlled protection is not used. However, it is recommended that the <math>\overline{WP}</math> pin also be externally connected to <math>V_{CC}</math> whenever possible.</p>	Low	Input

Table 1. Pin Configurations (Continued)

Symbol	Name and Function	Asserted State	Type
$\overline{\text{RESET}}$	<p><b>Reset:</b> A low state on the reset pin (<math>\overline{\text{RESET}}</math>) terminates the operation in progress and resets the internal state machine to an idle state. The device remains in the reset condition as long as a low level is present on the <math>\overline{\text{RESET}}</math> pin. Normal operation can resume once the <math>\overline{\text{RESET}}</math> pin is brought back to a high level.</p> <p>The device incorporates an internal power-on reset circuit, so there are no restrictions on the <math>\overline{\text{RESET}}</math> pin during power-on sequences. If this pin and feature is not used, then it is recommended that the <math>\overline{\text{RESET}}</math> pin be driven high externally.</p>	Low	Input
$V_{\text{CC}}$	<p><b>Device Power Supply:</b> The <math>V_{\text{CC}}</math> pin is used to supply the source voltage to the device. Operations at invalid <math>V_{\text{CC}}</math> voltages can produce spurious results; do not attempt this.</p>	—	Power
GND	<p><b>Ground:</b> The ground reference for the power supply. Connect GND to the system ground.</p>	—	Ground



### 3. Block Diagram

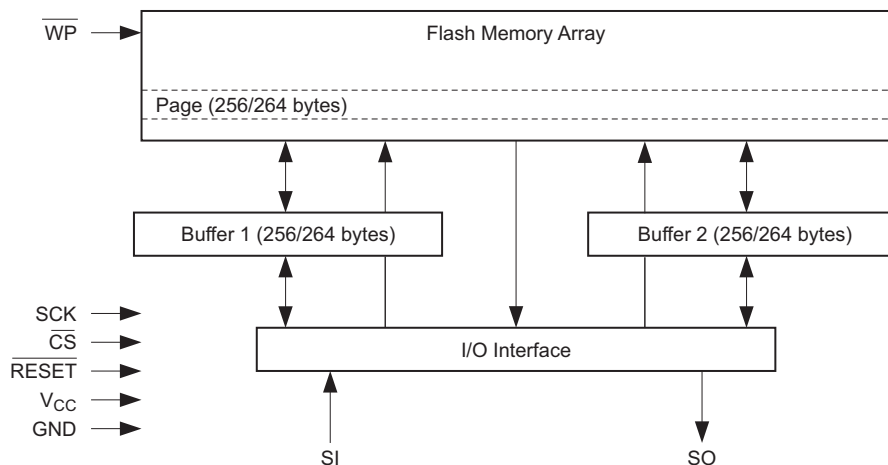


Figure 2. Block Diagram

## 4. Memory Array

To provide optimal flexibility, the AT45DB041E memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. Figure 3 illustrates the breakdown of each level and details the number of pages per sector and block. Program operations to the DataFlash can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip, sector, block, or page level.

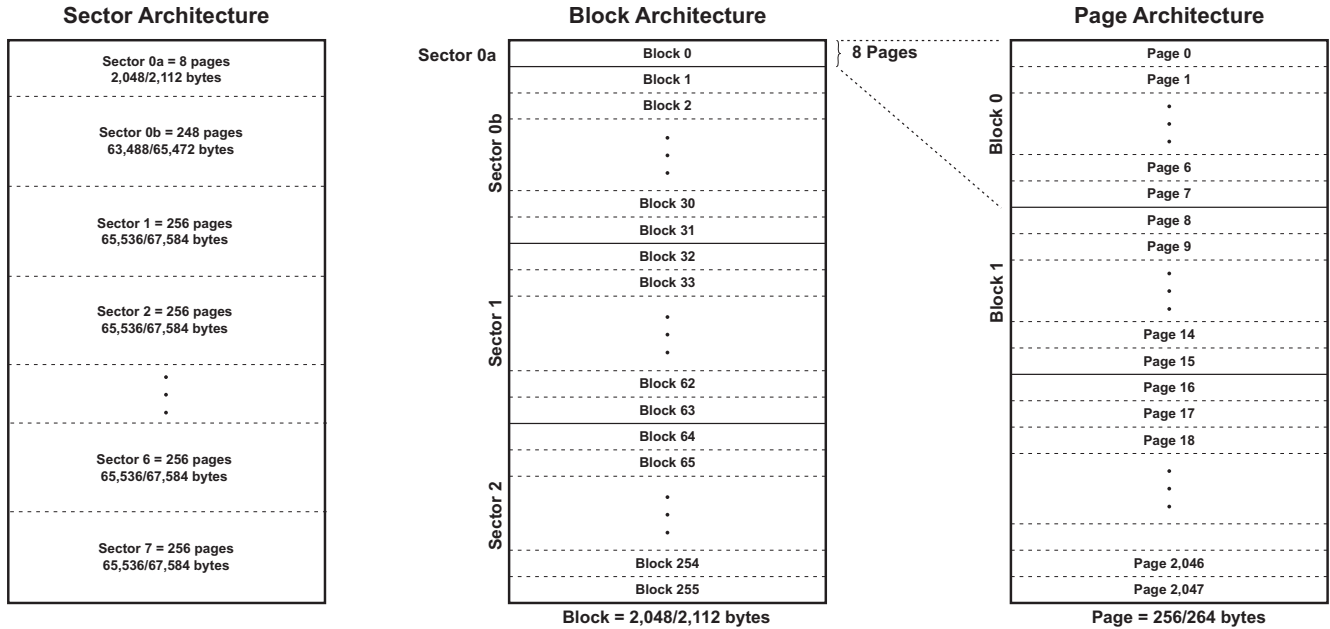


Figure 3. Memory Architecture Diagram

## 5. Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in [Table on page 46](#), through [Table on page 47](#). A valid instruction starts with the falling edge of  $\overline{CS}$  followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the  $\overline{CS}$  pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (Serial Input) pin. All instructions, addresses, and data are transferred with the Most Significant Bit (MSB) first.

Three address bytes are used to address memory locations in either the main memory array or in one of the SRAM buffers. The three address bytes are comprised of a number of dummy bits and a number of actual device address bits, with the number of dummy bits varying depending on the operation being performed and the selected device page size. Buffer addressing for the standard DataFlash page size (264 bytes) is referenced in the datasheet using the terminology BFA8 - BFA0 to denote the 9 address bits required to designate a byte address within a buffer. The main memory addressing is referenced using the terminology PA10 - PA0 and BA8 - BA0, where PA10 - PA0 denotes the 11 address bits required to designate a page address, and BA8 - BA0 denotes the 9 address bits required to designate a byte address within the page. Therefore, when using the standard DataFlash page size, a total of 20 address bits are used.

For the “power of 2” binary page size (256 bytes), the buffer addressing is referenced in the datasheet using the conventional terminology BFA7 - BFA0 to denote the eight address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A18 - A0, where A18 - A8 denotes the 11 address bits required to designate a page address, and A7 - A0 denotes the eight address bits required to designate a byte address within a page. Therefore, when using the binary page size, a total of 19 address bits are used.

## 6. Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS protocols for Mode 0 and Mode 3. See [Section 26](#), diagrams in this datasheet for details on the clock cycle sequences for each mode.

### 6.1 Continuous Array Read (Legacy Command: E8h Opcode)

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be used to sequentially read a continuous stream of data from the device by providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that automatically increments on every clock cycle, allowing one continuous read from memory to be performed without the need for additional address sequences. To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), an opcode of E8h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last nine (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), an opcode of E8h must be clocked into the device followed by three address bytes and four dummy bytes. The first 11 bits (A18 - A8) of the 19-bit address sequence specify which page of the main memory array to read and the last eight bits (A7 - A0) of the 19-bit address sequence specify the starting byte address within the page. The dummy bytes that follow the address bytes are needed to initialize the read operation. Following the dummy bytes, additional clock pulses on the SCK pin result in data being output on the SO (serial output) pin.

The  $\overline{\text{CS}}$  pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the  $\overline{\text{CS}}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the  $f_{\text{CAR1}}$  specification. The Continuous Array Read bypasses the data buffers and leaves the contents of the buffers unchanged.

**Warning:** This command is not recommended for new designs.

### 6.2 Continuous Array Read (High Frequency Mode: 1Bh Opcode)

This command can be used to read the main memory array sequentially at the highest possible operating clock frequency up to the maximum specified by  $f_{\text{CAR4}}$ . To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the  $\overline{\text{CS}}$  pin must first be asserted, and then an opcode of 1Bh must be clocked into the device followed by three address bytes and two dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 1Bh must be clocked into the device followed by three address bytes (A18 - A0) and two dummy bytes. Following the dummy bytes, additional clock pulses on the SCK pin results in data being output on the SO (Serial Output) pin.

The  $\overline{\text{CS}}$  pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of

memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the  $f_{CAR1}$  specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

### 6.3 Continuous Array Read (High Frequency Mode: 0Bh Opcode)

This command can be used to read the main memory array sequentially at higher clock frequencies up to the maximum specified by  $f_{CAR1}$ . To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the  $\overline{CS}$  pin must first be asserted, and then an opcode of 0Bh must be clocked into the device followed by three address bytes and one dummy byte. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 0Bh must be clocked into the device followed by three address bytes (A18 - A0) and one dummy byte. Following the dummy byte, additional clock pulses on the SCK pin result in data being output on the SO pin.

The  $\overline{CS}$  pin must remain low during the loading of the opcode, the address bytes, the dummy byte, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the  $f_{CAR1}$  specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

### 6.4 Continuous Array Read (Low Frequency Mode: 03h Opcode)

This command can be used to read the main memory array sequentially at lower clock frequencies up to maximum specified by  $f_{CAR2}$ . Unlike the previously described read commands, this Continuous Array Read command for the lower clock frequencies does not require the clocking in of dummy bytes after the address byte sequence. To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the  $\overline{CS}$  pin must first be asserted, and then an opcode of 03h must be clocked into the device followed by three address bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 03h must be clocked into the device followed by three address bytes (A18 - A0). Following the address bytes, additional clock pulses on the SCK pin result in data being output on the SO pin.

The  $\overline{CS}$  pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the  $f_{CAR2}$  specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

## 6.5 Continuous Array Read (Low Power Mode: 01h Opcode)

This command is ideal for applications that want to minimize power consumption and do not need to read the memory array at high frequencies. Like the 03h opcode, this Continuous Array Read command allows reading the main memory array sequentially without the need for dummy bytes to be clocked in after the address byte sequence. The memory can be read at clock frequencies up to maximum specified by  $f_{CAR3}$ . To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the  $\overline{CS}$  pin must first be asserted, and then an opcode of 01h must be clocked into the device followed by three address bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify which page of the main memory array to read and the last 9 bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 01h must be clocked into the device followed by three address bytes (A18 - A0). Following the address bytes, additional clock pulses on the SCK pin results in data being output on the SO pin.

The  $\overline{CS}$  pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the  $f_{CAR3}$  specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

## 6.6 Main Memory Page Read

A Main Memory Page Read allows the reading of data directly from a single page in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read using the standard DataFlash page size (264 bytes), an opcode of D2h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four dummy bytes. The first 11 bits (PA10 - PA0) of the 20-bit address sequence specify the page in main memory to be read and the last nine bits (BA8 - BA0) of the 20-bit address sequence specify the starting byte address within that page. To start a page read using the binary page size (256 bytes), the opcode D2h must be clocked into the device followed by three address bytes and four dummy bytes. The first 11 bits (A18 - A8) of the 19-bit address sequence specify which page of the main memory array to read, and the last eight bits (A7 - A0) of the 19-bit address sequence specify the starting byte address within that page. The dummy bytes that follow the address bytes are sent to initialize the read operation. Following the dummy bytes, the additional pulses on SCK result in data being output on the SO (serial output) pin.

The  $\overline{CS}$  pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. Unlike the Continuous Array Read command, when the end of a page in main memory is reached, the device continues reading back at the beginning of the same page rather than the beginning of the next page.

A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the  $f_{SCK}$  specification. The Main Memory Page Read bypasses both data buffers and leaves the contents of the buffers unchanged.

## 6.7 Buffer Read

The SRAM data buffers can be accessed independently from the main memory array, and using the Buffer Read command allows data to be sequentially read directly from either one of the buffers. Four opcodes, D4h or D1h for Buffer 1 and D6h or D3h for Buffer 2, can be used for the Buffer Read command. The use of each opcode depends on the maximum SCK frequency that is used to read data from the buffers. The D4h and D6h opcode can be used at any SCK frequency up to the maximum specified by  $f_{CAR1}$  while the D1h and D3h opcode can be used for lower frequency read operations up to the maximum specified by  $f_{CAR2}$ .

To perform a Buffer Read using the standard DataFlash buffer size (264 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 15 dummy bits and 9 buffer address bits (BFA8 - BFA0). To perform a Buffer Read using the binary buffer size (256 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 16 dummy bits and eight buffer address bits (BFA7 - BFA0). Following the address bytes, one dummy byte must be clocked into the device to initialize the read operation if using opcodes D4h or D6h. The  $\overline{CS}$  pin must remain low during the loading of the opcode, the address bytes, the dummy byte (if using opcodes D4h or D6h), and the reading of data. When the end of a buffer is reached, the device continues reading back at the beginning of the buffer. A low-to-high transition on the  $\overline{CS}$  pin terminates the read operation and tri-states the output pin (SO).

## 7. Program and Erase Commands

### 7.1 Buffer Write

Using the Buffer Write command allows data clocked in from the SI pin to be written directly into either one of the SRAM data buffers.

To load data into a buffer using the standard DataFlash buffer size (264 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2 must be clocked into the device followed by three address bytes comprised of 15 dummy bits and nine buffer address bits (BFA8 - BFA0). The nine buffer address bits specify the first byte in the buffer to be written.

To load data into a buffer using the binary buffer size (256 bytes), an opcode of 84h for Buffer 1 or 87h for Buffer 2, must be clocked into the device followed by 16 dummy bits and eight buffer address bits (BFA7 - BFA0). The eight buffer address bits specify the first byte in the buffer to be written.

After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device wraps around back to the beginning of the buffer. Data continues to be loaded into the buffer until a low-to-high transition is detected on the  $\overline{CS}$  pin.

### 7.2 Buffer to Main Memory Page Program with Built-In Erase

The Buffer to Main Memory Page Program with Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into an erased or programmed page in the main memory array. It is not necessary to pre-erase the page in main memory to be written because this command automatically erases the selected page prior to the program cycle.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the standard DataFlash page size (264 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the binary page size (256 bytes), an opcode of 83h for Buffer 1 or 86h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the  $\overline{CS}$  pin, the device first erases the selected page in main memory (the erased state is a logic 1) and then program the data stored in the appropriate buffer into that same page in main memory. Both erasing and programming, the page are internally self-timed and take a maximum time of  $t_{EP}$ .

During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase and program algorithm that can detect when a byte location fails to erase or program properly. If an erase or programming error arises, it is indicated by the EPE bit in the Status Register.

### 7.3 Buffer to Main Memory Page Program without Built-In Erase

The Buffer to Main Memory Page Program without Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors.

To perform a Buffer to Main Memory Page Program without Built-In Erase using the standard DataFlash page size (264 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program using the binary page size (256 bytes), an opcode of 88h for Buffer 1 or 89h for Buffer 2 must be clocked into the device followed by three address bytes comprised of three



dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the  $\overline{CS}$  pin, the device programs the data stored in the appropriate buffer into the specified page in the main memory. The page in main memory that is being programmed must have been previously erased using one of the erase commands (Page Erase, Block Erase, Sector Erase, or Chip Erase). Programming the page is internally self-timed and takes a maximum time of  $t_p$ . During this time, the RDY/BUSY bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

## 7.4 Main Memory Page Program through Buffer with Built-In Erase

The Main Memory Page Program through Buffer with Built-In Erase command combines the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations into a single operation to help simplify application firmware development. With the Main Memory Page Program through Buffer with Built-In Erase command, data is first clocked into either Buffer 1 or Buffer 2, the addressed page in memory is then automatically erased, and then the contents of the appropriate buffer are programmed into the just-erased main memory page.

To perform a Main Memory Page Program through Buffer using the standard DataFlash page size (264 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written.

To perform a Main Memory Page Program through Buffer using the binary page size (256 bytes), an opcode of 82h for Buffer 1 or 85h for Buffer 2 must first be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight buffer address bits (BFA7 - BFA0) that select the first byte in the buffer to be written.

After all address bytes have been clocked in, the device takes data from the input pin (SI) and store it in the specified data buffer. If the end of the buffer is reached, the device wraps around back to the beginning of the buffer. When there is a low-to-high transition on the  $\overline{CS}$  pin, the device first erases the selected page in main memory (the erased state is a logic 1) and then program the data stored in the buffer into that main memory page. Both erasing and programming the page are internally self-timed and take a maximum time of  $t_{EP}$ . During this time, the RDY/BUSY bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it is indicated by the EPE bit in the Status Register.

## 7.5 Main Memory Byte/Page Program through Buffer 1 without Built-In Erase

The Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command combines both the Buffer Write and Buffer to Main Memory Program without Built-In Erase operations to allow any number of bytes (1 to 256/264 bytes) to be programmed directly into previously erased locations in the main memory array. With the Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command, data is first clocked into Buffer 1, and then only the bytes clocked into the buffer are programmed into the pre-erased byte locations in main memory. Multiple bytes up to the page size can be entered with one command sequence.

To perform a Main Memory Byte/Page Program through Buffer 1 using the standard DataFlash page size (264 bytes), an opcode of 02h must first be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the device takes data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 264) can be entered. If the end of the buffer is reached, then the device wraps around back to the beginning of the buffer.

To perform a Main Memory Byte/Page Program through Buffer 1 using the binary page size (256 bytes), an opcode of 02h for Buffer 1 using must first be clocked into the device followed by three address bytes comprised of three dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight buffer address bits (BFA7 - BFA0) that selects the first byte in the buffer to be written. After all address bytes are clocked in, the device takes data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 256) can be entered. If the end of the buffer is reached, then the device wraps around back to the beginning of the buffer. When using the binary page size, the page and buffer address bits correspond to a 19-bit logical address (A18-A0) in the main memory.

After all data bytes have been clocked into the device, a low-to-high transition on the  $\overline{CS}$  pin starts the program operation in which the device programs the data stored in Buffer 1 into the main memory array. Only the data bytes that were clocked into the device are programmed into the main memory.

If only two data bytes were clocked into the device, then only two bytes are programmed into main memory and the remaining bytes in the memory page remain in their previous state.

The  $\overline{CS}$  pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data is programmed. Programming the data bytes is internally self-timed and takes a maximum time of  $t_p$  (the program time is a multiple of the  $t_{BP}$  time depending on the number of bytes being programmed). During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

## 7.6 Read-Modify-Write

A completely self-contained read-modify-write operation can be performed to reprogram any number of sequential bytes in a page in the main memory array without affecting the rest of the bytes in the same page. This command allows the device to easily emulate an EEPROM by providing a method to modify a single byte or more in the main memory in a single operation, without the need for pre-erasing the memory or the need for any external RAM buffers. The Read-Modify-Write command is essentially a combination of the Main Memory Page to Buffer Transfer, Buffer Write, and Buffer to Main Memory Page Program with Built-in Erase commands.

To perform a Read-Modify-Write using the standard DataFlash page size (264 bytes), an opcode of 58h for Buffer 1 or 59h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be written, and nine byte address bits (BA8 - BA0) that designate the starting byte address within the page to reprogram.

To perform a Read-Modify-Write using the binary page size (256 bytes), an opcode of 58h for Buffer 1 or 59h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be written, and eight byte address bits (A7 - A0) designate the starting byte address within the page to reprogram.

After the address bytes have been clocked in, any number of sequential data bytes from one to 256/264 bytes can be clocked into the device. If the end of the buffer is reached when clocking in the data, then the device wraps around back to the beginning of the buffer. After all data bytes have been clocked into the device, a low-to-high transition on the CS pin starts the self-contained, internal read-modify-write operation. Only the data bytes that were clocked into the device is reprogrammed in the main memory.

**Example:** If only one data byte was clocked into the device, then only one byte in main memory is reprogrammed and the remaining bytes in the main memory page remain in their previous state.

The  $\overline{CS}$  pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data is programmed. The reprogramming of the data bytes is internally self-timed and takes a maximum time of  $t_p$ . During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it is indicated by the EPE bit in the Status Register.

**Note:** The Read-Modify-Write command uses the same opcodes as the Auto Page Rewrite command. If no data bytes are clocked into the device, then the device performs an Auto Page Rewrite operation. See the Auto Page Rewrite command description on [page 33](#) for more details.

## 7.7 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command or the Main Memory Byte/Page Program through Buffer 1 command to be used at a later time.

To perform a Page Erase with the standard DataFlash page size (264 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) that specify the page in the main memory to be erased, and nine dummy bits.

To perform a Page Erase with the binary page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory to be erased, and eight dummy bits.

When a low-to-high transition occurs on the  $\overline{CS}$  pin, the device erases the selected page (the erased state is a logic 1). The erase operation is internally self-timed and takes a maximum time of  $t_{PE}$ . During this time, the  $\overline{RDY}/\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

## 7.8 Block Erase

The Block Erase command can be used to erase a block of eight pages at one time. This command is useful when needing to pre-erase larger amounts of memory and is more efficient than issuing eight separate Page Erase commands.

To perform a Block Erase with the standard DataFlash page size (264 bytes), an opcode of 50h must be clocked into the device, followed by three address bytes comprised of four dummy bits, eight page address bits (PA10 - PA3), and 12 dummy bits. The eight page address bits are used to specify which block of eight pages is to be erased.

Table 2. Erase Block Command

PA10/ A18	PA9/A 17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Block
0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	0	X	X	X	252
1	1	1	1	1	1	0	1	X	X	X	253
1	1	1	1	1	1	1	0	X	X	X	254
1	1	1	1	1	1	1	1	X	X	X	255

To perform a Block Erase with the binary page size (256 bytes), an opcode of 50h must be clocked into the device, followed by three address bytes comprised of five dummy bits, eight page address bits (A18 - A11), and 11 dummy bits. The eight page address bits specify which block of eight pages is to be erased.

When a low-to-high transition occurs on the  $\overline{CS}$  pin, the device erases the selected block of eight pages. The erase operation is internally self-timed and takes a maximum time of  $t_{BE}$ . During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

## 7.9 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory.

The main memory array is comprised of nine sectors, and only one sector can be erased at a time. To perform an erase of Sector 0a or Sector 0b with the standard DataFlash page size (264 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of four dummy bits, eight page address bits (PA10 - PA3), and 12 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of four dummy bits, three page address bits (PA10 - PA8), and 17 dummy bits.

To perform a Sector 0a or Sector 0b erase with the binary page size (256 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of five dummy bits, eight page address bits (A18 - A11), and 11 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by three dummy bits, three page address bits (A18 - A16), and 16 dummy bits.

The page address bits are used to specify any valid address location within the sector to be erased. When a low-to-high transition occurs on the  $\overline{CS}$  pin, the device erases the selected sector. The erase operation is internally self-timed and takes a maximum time of  $t_{SE}$ . During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

Table 3. Sector Erase

PA10/ A18	PA9/A 17	PA8/A 16	PA7/A 15	PA6/A 14	PA5/A 13	PA4/A 12	PA3/A 11	PA2/A 10	PA1/A 9	PA0/A 8	Sector
0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	1	X	X	X	0b
0	0	1	X	X	X	X	X	X	X	X	1
0	1	0	X	X	X	X	X	X	X	X	2
0	1	1	X	X	X	X	X	X	X	X	3
1	0	0	X	X	X	X	X	X	X	X	4
1	0	1	X	X	X	X	X	X	X	X	5
1	1	0	X	X	X	X	X	X	X	X	6
1	1	1	X	X	X	X	X	X	X	X	7

## 7.10 Chip Erase

The Chip Erase command allows the entire main memory array to be erased can be erased at one time.

To execute the Chip Erase command, a four-byte command sequence of C7h, 94h, 80h, and 9Ah must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. After the last bit of the opcode sequence has been clocked in, the  $\overline{CS}$  pin must be deasserted to start the erase process. The erase operation is internally self-timed and takes a time of  $t_{CE}$ . During this time, the RDY/BUSY bit in the Status Register indicates that the device is busy.

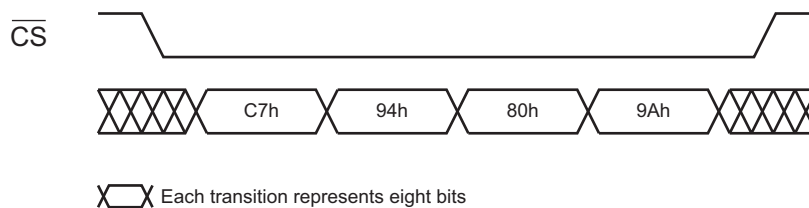
The Chip Erase command does not affect sectors that are protected or locked down; the contents of those sectors remain unchanged. Only those sectors that are not protected or locked down are erased.

The  $\overline{WP}$  pin can be asserted while the device is erasing, but protection is not activated until the internal erase cycle completes.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

**Table 4. Chip Erase Command**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7h	94h	80h	9Ah



**Figure 4. Chip Erase**

## 7.11 Program/Erase Suspend

In some code and data storage applications, it might not be possible for the system to wait the milliseconds required for the Flash memory to complete a program or erase cycle. The Program/Erase Suspend command allows a program or erase operation in progress to a particular 64 kB sector of the main memory array to be suspended so that other device operations can be performed.

**Example:** By suspending an erase operation to a particular sector, the system can perform functions such as a program or read operation within a different 64 kB sector. Other device operations, such as Read Status Register, can also be performed while a program or erase operation is suspended.

To perform a Program/Erase Suspend, an opcode of B0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently in progress is suspended within a time of  $t_{SUSP}$ . One of the Program Suspend bits ( $\overline{PS1}$  or  $\overline{PS2}$ ) or the Erase Suspend bit (ES) in the Status Register is then set to the logic 1 state. Also, the RDY/BUSY bit in the Status Register indicates that the device is ready for another operation.

Read operations are not allowed to a 64 kB sector that has had its program or erase operation suspended. If a read is attempted to a suspended sector, then the device outputs undefined data. Therefore, when performing a Continuous Array Read operation and the device's internal address counter increments and crosses the sector boundary to a suspended sector, the device then starts outputting undefined data continuously until the address counter increments and crosses a sector boundary to an unsuspended sector.

A program operation is not allowed to a sector that has been erase suspended. If a program operation is attempted to an erase suspended sector, then the program operation aborts.

During an Erase Suspend, a program operation to a different 64 kB sector can be started and subsequently suspended. This results in a simultaneous Erase Suspend/Program Suspend condition and is indicated by the states of both the ES and PS1 or PS2 bits in the Status Register being set to a logic 1.

If a Reset command is performed, or if the  $\overline{\text{RESET}}$  pin is asserted while a sector is erase suspended, then the suspend operation is aborted and the contents of the sector is left in an undefined state. However, if a reset is performed while a page is program or erase suspended, the suspend operation aborts but only the contents of the page that was being programmed or erased is undefined; the remaining pages in the 64 kB sector retain their previous contents.

**Table 5. Program/Erase Suspend Commands**

Command	Operation During Program Suspend in Buffer 1 (PS1)	Operation During Program Suspend in Buffer 2 (PS2)	Operation During Erase Suspend (ES)
Read Commands			
Read Array (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 1 (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 2 (All Opcodes)	Allowed	Allowed	Allowed
Program and Erase Commands			
Buffer 1 Write	Not Allowed	Allowed	Allowed
Buffer 2 Write	Allowed	Not Allowed	Allowed
Buffer 1 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 2 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 1 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Buffer 2 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Memory Program through Buffer 1 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 2 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 1 w/o Erase	Not Allowed	Not Allowed	Allowed
Auto Page Rewrite through Buffer 1	Not Allowed	Not Allowed	Not Allowed
Auto Page Rewrite through Buffer 2	Not Allowed	Not Allowed	Not Allowed
Read-Modify-Write through Buffer 1	Not Allowed	Not Allowed	Not Allowed
Read-Modify-Write through Buffer 2	Not Allowed	Not Allowed	Not Allowed
Page Erase	Not Allowed	Not Allowed	Not Allowed
Block Erase	Not Allowed	Not Allowed	Not Allowed
Sector Erase	Not Allowed	Not Allowed	Not Allowed
Chip Erase	Not Allowed	Not Allowed	Not Allowed
Protection and Security Commands			
Enable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Disable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Erase Sector Protection Register	Not Allowed	Not Allowed	Not Allowed
Program Sector Protection Register	Not Allowed	Not Allowed	Not Allowed

Table 5. Program/Erase Suspend Commands (Continued)

Command	Operation During Program Suspend in Buffer 1 (PS1)	Operation During Program Suspend in Buffer 2 (PS2)	Operation During Erase Suspend (ES)
Read Sector Protection Register	Allowed	Allowed	Allowed
Sector Lockdown	Not Allowed	Not Allowed	Not Allowed
Read Sector Lockdown	Allowed	Allowed	Allowed
Freeze Sector Lockdown State	Not Allowed	Not Allowed	Not Allowed
Program Security Register	Not Allowed	Not Allowed	Not Allowed
Read Security Register	Allowed	Allowed	Allowed
Additional Commands			
Main Memory to Buffer 1 Transfer	Not Allowed	Allowed	Allowed
Main Memory to Buffer 2 Transfer	Allowed	Not Allowed	Allowed
Main Memory to Buffer 1 Compare	Not Allowed	Allowed	Allowed
Main Memory to Buffer 2 Compare	Allowed	Not Allowed	Allowed
Enter Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Resume from Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Enter Ultra-Deep Power-Down mode	Not Allowed	Not Allowed	Not Allowed
Read Configuration Register	Allowed	Allowed	Allowed
Read Status Register	Allowed	Allowed	Allowed
Read Manufacturer and Device ID	Allowed	Allowed	Allowed
Reset (via Hardware or Software)	Allowed	Allowed	Allowed

## 7.12 Program/Erase Resume

The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue where it left off.

To perform a Program/Erase Resume, an opcode of D0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently suspended is resumed within a time of  $t_{RES}$ . The PS1 bit, PS2 bit, or ES bit in the Status Register are then reset back to a logic 0 state to indicate that the program or erase operation is no longer suspended. Also, the  $\overline{RDY}/\overline{BUSY}$  bit in the Status Register indicates that the device is busy performing a program or erase operation.

During a simultaneous Erase Suspend/Program Suspend condition, issuing the Program/Erase Resume command results in the program operation resuming first. After the program operation has been completed, the Program/Erase Resume command must be issued again in order for the erase operation to be resumed.

While the device is busy resuming a program or erase operation, any attempts at issuing the Program/Erase Suspend command is ignored. Therefore, if a resumed program or erase operation needs to be subsequently suspended again, the system must either wait the entire  $t_{RES}$  time before issuing the Program/Erase Suspend command, or it must check the status of the  $\overline{RDY}/\overline{BUSY}$  bit or the appropriate PS1, PS2, or ES bit in the Status Register to determine if the previously suspended program or erase operation has resumed.



## 8. Sector Protection

Two protection methods, hardware- and software-controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software-controlled method uses software commands to enable and disable sector protection; the hardware-controlled method uses the Write Protect ( $\overline{WP}$ ) pin. The selection of which sectors to be protected or unprotected is specified in the Nonvolatile Sector Protection Register. Check the Status Register to see whether or not sector protection has been enabled by either method.

### 8.1 Software Sector Protection

Software controlled protection is useful in applications in which the  $\overline{WP}$  pin is not or cannot be controlled by a host processor. In such instances, the  $\overline{WP}$  pin can be left floating (the  $\overline{WP}$  pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

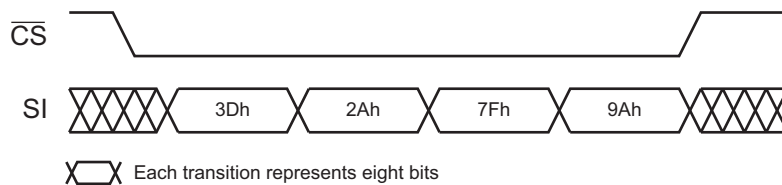
If the device is power cycled, the software controlled protection is disabled. Once the device is powered up, reissue the Enable Sector Protection command if sector protection is needed and if the  $\overline{WP}$  pin is not used.

#### 8.1.1 Enable Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and A9h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the  $\overline{CS}$  pin must be deasserted to enable the Sector Protection.

**Table 6. Enable Sector Protection Command**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3Dh	2Ah	7Fh	A9h



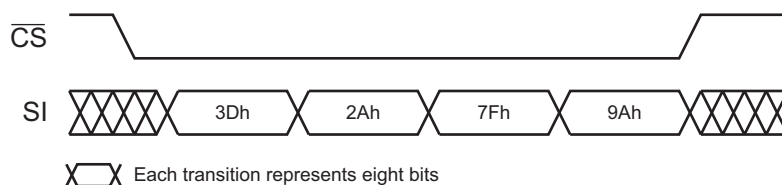
**Figure 5. Enable Sector Protection**

#### 8.1.2 Disable Sector Protection

To disable the sector protection, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and 9Ah must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the  $\overline{CS}$  pin must be deasserted to disable the sector protection.

**Table 7. Disable Sector Protection Command**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3Dh	2Ah	7Fh	9Ah



**Figure 6. Disable Sector Protection**



## 8.2 Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the  $\overline{WP}$  pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or programmed as long as the  $\overline{WP}$  pin is asserted. In order to modify the Sector Protection Register, the  $\overline{WP}$  pin must be deasserted. If the  $\overline{WP}$  pin is permanently connected to GND, then the contents of the Sector Protection Register cannot be changed. If the  $\overline{WP}$  pin is deasserted or permanently connected to  $V_{CC}$ , then the contents of the Sector Protection Register can be modified.

The  $\overline{WP}$  pin overrides the software controlled protection method but only for protecting the sectors.

**Example:** If the sectors are not previously protected by the Enable Sector Protection command, then asserting the  $\overline{WP}$  pin enables the sector protection within the maximum specified  $t_{WPE}$  time. When the  $\overline{WP}$  pin is deasserted, however, the sector protection is no longer enabled (after the maximum specified  $t_{WPD}$  time) as long as the Enable Sector Protection command was not issued while the  $\overline{WP}$  pin was asserted. If the Enable Sector Protection command was issued before or while the  $\overline{WP}$  pin was asserted, then deasserting the  $\overline{WP}$  pin does not disable the sector protection. In this case, the Disable Sector Protection command must be issued while the  $\overline{WP}$  pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the  $\overline{WP}$  pin is asserted.

A noise filter is incorporated to help protect against spurious noise that might inadvertently assert or deassert the  $\overline{WP}$  pin.

Table 8 and Figure 7 detail the sector protection status for various scenarios of the  $\overline{WP}$  pin, the Enable Sector Protection command, and the Disable Sector Protection command.

Table 8.  $\overline{WP}$  Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously	X	Disabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write
2	Low	X	X	Enabled	Read
3	High	Command Issued During Period 1 or 2	Not Issued Yet	Enabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write



Figure 7.  $\overline{WP}$  Pin and Protection Status

## 8.3 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains eight bytes of data, of which byte locations zero through seven contain values that specify whether Sectors 0 through 7 are protected or unprotected. The Sector Protection Register is user modifiable and must be erased before it can be reprogrammed. Table 9 details the format of the Sector Protection Register.

**Table 9. Sector Protection Register**

Sector Number	0 (0a, 0b)	1 to 7
Protected	See Table 10	FFh
Unprotected		00h

The default values for bytes 0 through 7 are 00h when shipped from Renesas Electronics.

**Table 10. Sector 0 (0a, 0b) Sector Protection Register Byte Value**

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-15)	N/A	N/A	
Sectors 0a and 0b Unprotected	00	00	XX	XX	0xh
Protect Sector 0a	11	00	XX	XX	Cxh
Protect Sector 0b	00	11	XX	XX	3xh
Protect Sectors 0a and 0b	11	11	XX	XX	Fxh

x = Don't care.

### 8.3.1 Erase Sector Protection Register

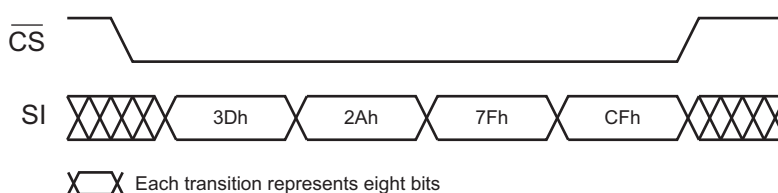
To modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

To erase the Sector Protection Register, clock a four-byte command sequence of 3Dh, 2Ah, 7Fh, and CFh into the device. After the opcode sequence has been clocked in, deassert the  $\overline{CS}$  pin to initiate the internally self-timed erase cycle. Erasing the Sector Protection Register takes a maximum time of  $t_{PE}$ . During this time, the RDY/BUSY bit in the Status Register indicates that the device is busy. If the device is powered-down before the erase cycle is done, the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with sector protection enabled or disabled. Since the erased state (FFh) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, the erroneous program or erase command is not processed because all sectors are protected.

**Table 11. Erase Sector Protection Register Command**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3Dh	2Ah	7Fh	CFh



**Figure 8. Erase Sector Protection Register**

### 8.3.2 Program Sector Protection Register

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and FCh must be clocked into the device followed by eight bytes of data corresponding to Sectors 0 through 7. After the last bit of the opcode sequence and data have been clocked in, the  $\overline{CS}$  pin must be deasserted to initiate the internally self-timed program cycle. Programming the Sector Protection Register takes a maximum time of  $t_p$ . During this time, the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy. If the device is powered-down before the erase cycle is done, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the  $\overline{CS}$  pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in cannot be guaranteed.

**Example:** If only the first two bytes are clocked in instead of the complete eight bytes, then the protection status of the last 14 sectors cannot be guaranteed. Furthermore, if more than eight bytes of data is clocked into the device, then the data wraps back around to the beginning of the register. For instance, if nine bytes of data are clocked in, then the ninth byte is stored at byte location 0 of the Sector Protection Register.

The data bytes clocked into the Sector Protection Register need to be valid values (0xh, 3xh, Cxh, and Fxh for Sector 0a or Sector 0b, and 00h or FFh for other sectors) in order for the protection to function correctly. If a non-valid value is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed.

**Example:** If a value of 17h is clocked into byte location 2 of the Sector Protection Register, then the protection status of Sector 2 cannot be guaranteed.

The Sector Protection Register can be reprogrammed while the sector protection is enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command uses Buffer 1 for processing. Therefore, the contents of Buffer 1 is altered from its previous state when this command is issued.

Table 12. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3Dh	2Ah	7Fh	FCh

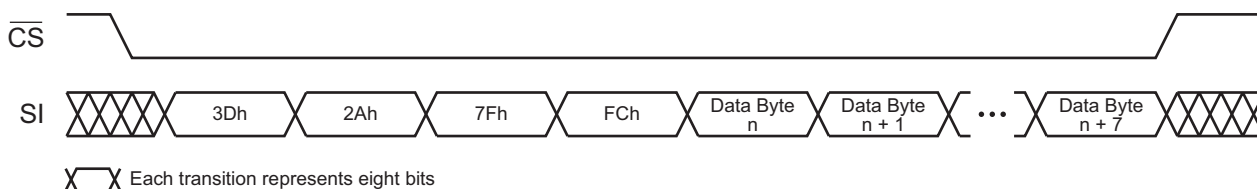


Figure 9. Program Sector Protection Register

### 8.3.3 Read Sector Protection Register

To read the Sector Protection Register, an opcode of 32h and three dummy bytes must be clocked into the device. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pin results in the Sector Protection Register contents being output on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 7) corresponds to Sector 7. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses result in undefined data being output on the SO pin. The  $\overline{CS}$  pin must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Table 13. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32h	XXh	XXh	XXh

XX = Dummy byte.

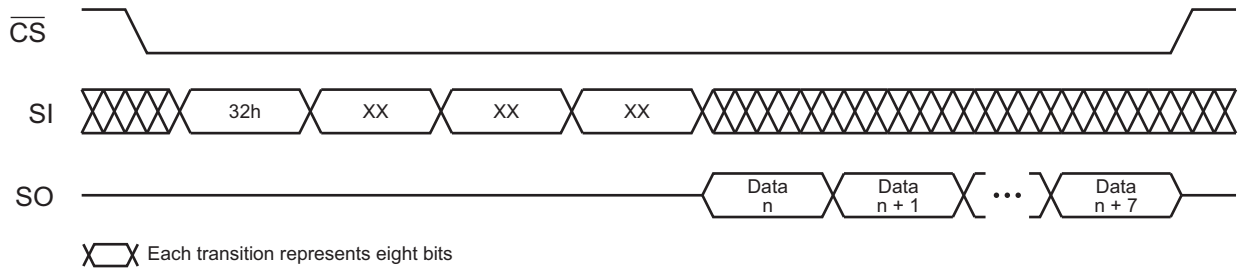


Figure 10. Read Sector Protection Register

### 8.3.4 About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register is modified during the course of the application's life cycle. If the application requires that the Security Protection Register be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application needs to limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely need to be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

## 9. Security Features

### 9.1 Sector Lockdown

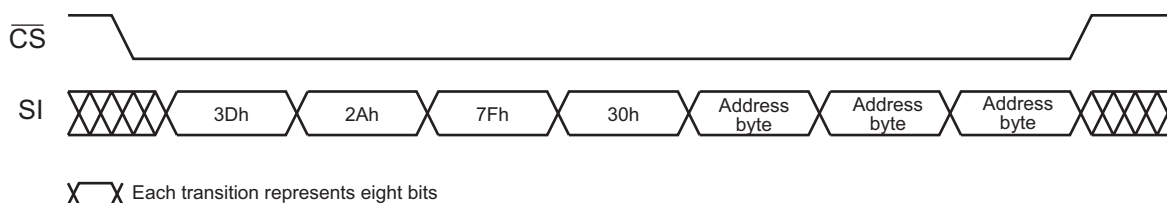
The device incorporates a sector lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read-only (ROM). This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information.

Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.

To issue the sector lockdown command, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and 30h must be clocked into the device followed by three address bytes specifying any address within the sector to be locked down. After the last address bit has been clocked in, the  $\overline{\text{CS}}$  pin must be deasserted to initiate the internally self-timed lockdown sequence. The lockdown sequence takes a maximum time of  $t_p$ . During this time, the RDY/BUSY bit in the Status Register indicates that the device is busy. If the device is powered-down before the lockdown sequence is done, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or bytes and re-issue the Sector Lockdown command if necessary.

**Table 14. Sector Lockdown Command**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector Lockdown	3Dh	2Ah	7Fh	30h



**Figure 11. Sector Lockdown**

#### 9.1.1 Read Sector Lockdown Register

The nonvolatile Sector Lockdown Register specifies which sectors in the main memory are currently unlocked or have been permanently locked down. The Sector Lockdown Register is a read-only register and contains eight bytes of data which correspond to Sectors 0 through 7. To read the Sector Lockdown Register, an opcode of 35h must be clocked into the device followed by three dummy bytes. After the last bit of the opcode and dummy bytes have been clocked in, the data for the contents of the Sector Lockdown Register is clocked out on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 7) corresponds to Sector 7. After the last byte of the Sector Lockdown Register has been read, additional pulses on the SCK pin results in undefined data being output on the SO pin.

Deasserting the  $\overline{\text{CS}}$  pin terminates the Read Sector Lockdown Register operation and put the SO pin into a high-impedance state. [Table](#) details the format the Sector Lockdown Register.

**Table 15. Sector Lockdown Register**

Sector Number	0 (0a, 0b)	1 to 7
Locked	See <a href="#">Table</a>	FFh
Unlocked		00h

Table 16. Sector 0 (0a and 0b) Sector Lockdown Register Byte Value

Sector Lock/Unlock	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-15)	N/A	N/A	
Sectors 0a and 0b Unlocked	00	00	00	00	00h
Sector 0a Locked	11	00	00	00	C0h
Sector 0b Locked	00	11	00	00	30h
Sectors 0a and 0b Locked	11	11	00	00	F0h

Table 17. Read Sector Lockdown Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Lockdown Register	35h	XXh	XXh	XXh

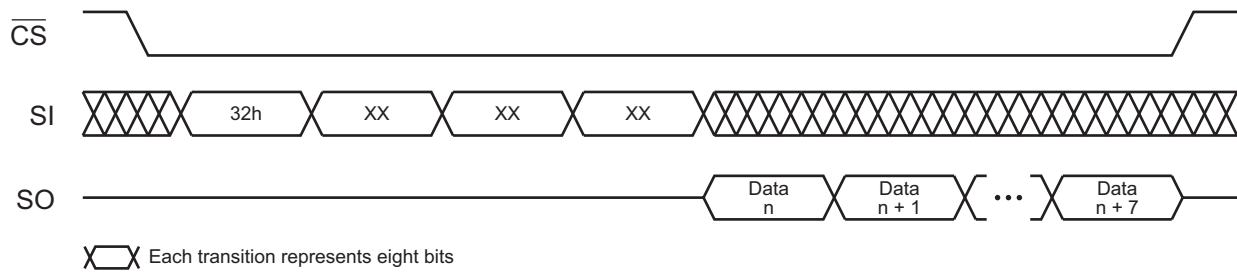


Figure 12. Read Sector Lockdown Register

### 9.1.2 Freeze Sector Lockdown

The Sector Lockdown command can be permanently disabled, and the current sector lockdown state can be permanently frozen so that no additional sectors can be locked down, aside from those already locked down. Any attempts to issue the Sector Lockdown command after the Sector Lockdown State has been frozen is ignored.

To issue the Freeze Sector Lockdown command, assert the  $\overline{CS}$  pin and clock the opcode sequence 34h, 55h, AAh, and 40h into the device. Any other data clocked into the device is ignored. When the  $\overline{CS}$  pin is deasserted, the current sector lockdown state is permanently frozen within a time of  $t_{LOCK}$ . Also, the SLE bit in the Status Register is permanently reset to a logic 0 to indicate that the Sector Lockdown command is permanently disabled.

Table 18. Freeze Sector Lockdown

Command	Byte 1	Byte 2	Byte 3	Byte 4
Freeze Sector Lockdown	34h	55h	AAh	40h

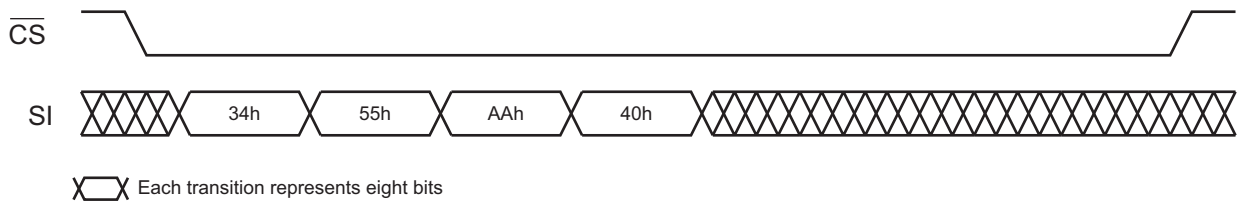


Figure 13. Freeze Sector Lockdown

## 9.2 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as a One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Adesto and contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 19. Security Register

	Security Register Byte Number							
	0	1	...	63	64	65	...	127
Data Type	One-Time User Programmable				Factory Programmed by Adesto			

### 9.2.1 Programming the Security Register

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, a four-byte opcode sequence of 9Bh, 00h, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the  $\overline{CS}$  pin must be deasserted to initiate the internally self-timed program cycle. Programming the Security Register takes a time of  $t_p$ , during which time the  $\overline{RDY}/\overline{BUSY}$  bit in the Status Register indicates that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

If the full 64 bytes of data are not clocked in before the  $\overline{CS}$  pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

**Example:** If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data wraps back around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte is stored at byte location 0 of the Security Register.

**Warning:** The user programmable portion of the Security Register can only be programmed one time.

Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command uses Buffer 1 for processing. Therefore, the contents of Buffer 1 is altered from its previous state when this command is issued.

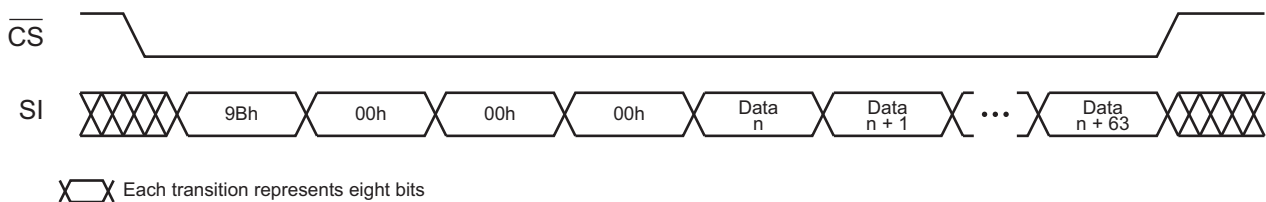


Figure 14. Program Security Register

### 9.2.2 Reading the Security Register

To read the Security Register, an opcode of 77h and three dummy bytes must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin results in undefined data being output on the SO pin.

Deasserting the  $\overline{CS}$  pin terminates the Read Security Register operation and put the SO pin into a high-impedance state.

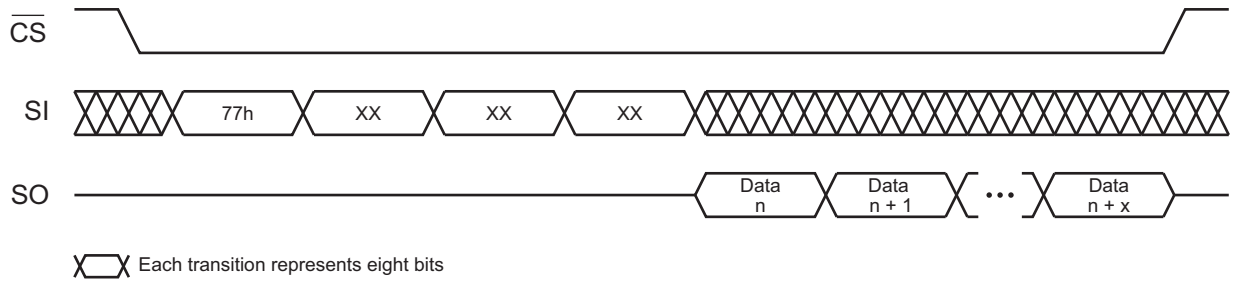


Figure 15. Read Security Register



## 10. Additional Commands

### 10.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to either Buffer 1 or Buffer 2. To transfer a page of data using the standard DataFlash page size (264 bytes), an opcode of 53h for Buffer 1 or 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) which specify the page in main memory to be transferred, and nine dummy bits. To transfer a page of data using the binary page size (256 bytes), an opcode of 53h for Buffer 1 and 55h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) which specify the page in the main memory to be transferred, and eight dummy bits.

The  $\overline{\text{CS}}$  pin must be low while toggling the SCK pin to load the opcode and the three address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer begins when the  $\overline{\text{CS}}$  pin transitions from a low to a high state. During the page transfer time ( $t_{\text{XFR}}$ ), the RDY/BUSY bit in the Status Register can be read to determine whether or not the transfer has been completed.

### 10.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in Buffer 1 or Buffer 2 as a method to ensure that data was successfully programmed after a Buffer to Main Memory Page Program command. To compare a page of data with the standard DataFlash page size (264 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10 - PA0) which specify the page in the main memory to be compared to the buffer, and nine dummy bits. To compare a page of data with the binary page size (256 bytes), an opcode of 60h for Buffer 1 or 61h for Buffer 2 must be clocked into the device followed by three address bytes comprised of five dummy bits, 11 page address bits (A18 - A8) which specify the page in the main memory to be compared to the buffer, and eight dummy bits.

The  $\overline{\text{CS}}$  pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the  $\overline{\text{CS}}$  pin, the data bytes in the selected Main Memory Page are compared with the data bytes in Buffer 1 or Buffer 2. During the compare time ( $t_{\text{COMP}}$ ), the RDY/BUSY bit in the Status Register indicates that the part is busy. After the compare operation, bit 6 of the Status Register is updated with the result of the compare.

### 10.3 Auto Page Rewrite

This command is used only if the possibility exists that static (non-changing) data can be stored in a page or pages of a sector, and the other pages of the same sector are erased and programmed a large number of times. Applications that modify data in a random fashion within a sector can fall into this category. To preserve data integrity of a sector, each page within a sector must be updated/rewritten at least once within every 50,000 cumulative page erase/program operations within that sector. The Auto Page Rewrite command provides a simple and efficient method to “refresh” a page in the main memory array in a single operation.

The Auto Page Rewrite command is a combination of the Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase commands. With the Auto Page Rewrite command, a page of data is first transferred from the main memory to Buffer 1 or Buffer 2 and then the same data (from Buffer 1 or Buffer 2) is programmed back into the same page of main memory, essentially “refreshing” the contents of that page. To start the Auto Page Rewrite operation with the standard DataFlash page size (264 bytes), a 1-byte opcode, 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes comprised of four dummy bits, 11 page address bits (PA10-PA0) that specify the page in main memory to be rewritten, and nine dummy bits.

To initiate an Auto Page Rewrite with the a binary page size (256 bytes), the opcode 58H for Buffer 1 or 59H for Buffer 2, must be clocked into the device followed by three address bytes consisting of five dummy bits, 11 page address bits (A18 - A8) that specify the page in the main memory that is to be rewritten, and eight dummy bits. When a low-to-high transition occurs on the  $\overline{\text{CS}}$  pin, the part first transfers data from the page in main memory to

a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and takes a maximum time of  $t_{EP}$ . During this time, the RDY/ $\overline{\text{BUSY}}$  Status Register indicates that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page and the possibility does not exist that there is a page or pages of static data, then the programming algorithm shown in [Figure 50 on page 68](#), is recommended. Otherwise, if there is a chance that a page or pages of a sector that contain static data, then the programming algorithm shown in [Figure 51](#), is recommended. Contact Adesto for availability of devices that are specified to exceed the 50,000 cycle cumulative limit.

**Note:** The Auto Page Rewrite command uses the same opcodes as the Read-Modify-Write command. If data bytes are clocked into the device, then the device performs a Read-Modify-Write operation. See the Read-Modify-Write command description on [page 18](#) for more details.

## 10.4 Status Register Read

The two-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, Freeze Sector Lockdown status, erase/program error status, Program/Erase Suspend status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the  $\overline{\text{CS}}$  pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence repeats itself, starting again with the first byte of the Status Register, as long as the CS pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence can output new data. The RDY/ $\overline{\text{BUSY}}$  status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the  $\overline{\text{CS}}$  pin terminates the Status Register Read operation and put the SO pin into a high-impedance state. The CS pin can be deasserted at any time and does not require that a full byte of data be read.

**Table 20. Status Register Format – Byte 1**

Bit	Name	Name	Type <sup>1)</sup>	Description	
7	RDY/ $\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	COMP	Compare Result	R	0	Main memory page data matches buffer data.
				1	Main memory page data does not match buffer data.
5:2	DENSITY	Density Code	R	0111	Four Mbit.
1	PROTECT	Sector Protection Status	R	0	Sector protection is disabled.
				1	Sector protection is enabled.
0	PAGE SIZE	Page Size Configuration	R	0	Device is configured for standard DataFlash page size (264 bytes).
				1	Device is configured for "power of 2" binary page size (256 bytes).

1. R = Readable only.

Table 21. Status Register Format – Byte 2

Bit	Name		Type <sup>(1)</sup>	Description	
7	RDY/ $\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	RES	Reserved for Future Use	R	0	Reserved for future use.
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	RES	Reserved for Future Use	R	0	Reserved for future use.
3	SLE	Sector Lockdown Enabled	R	0	Sector Lockdown command is disabled.
				1	Sector Lockdown command is enabled.
2	PS2	Program Suspend Status (Buffer 2)	R	0	No program operation has been suspended while using Buffer 2.
				1	A sector is program suspended while using Buffer 2.
1	PS1	Program Suspend Status (Buffer 1)	R	0	No program operation has been suspended while using Buffer 1.
				1	A sector is program suspended while using Buffer 1.
0	ES	Erase Suspend	R	0	No sectors are erase suspended.
				1	A sector is erase suspended.

1. R = Readable only.

#### 10.4.1 RDY/ $\overline{\text{BUSY}}$ Bit

The RDY/ $\overline{\text{BUSY}}$  bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/ $\overline{\text{BUSY}}$  bit to detect if an internally timed operation is done, new Status Register data must be continually clocked out of the device until the state of the RDY/ $\overline{\text{BUSY}}$  bit changes from a logic 0 to a logic 1.

#### 10.4.2 COMP Bit

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using the COMP bit. If the COMP bit is a logic 1, then at least one bit of the data in the Main Memory Page does not match the data in the buffer.

#### 10.4.3 DENSITY Bits

The device density is indicated using the DENSITY bits. For the AT45DB041E, the four bit binary value is 0111. The decimal value of these four binary bits does not actually equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The DENSITY bits are not the same as the density code indicated in the JEDEC Device ID information. The DENSITY bits are provided only for backward compatibility to older generation DataFlash devices.

#### 10.4.4 PROTECT Bit

The PROTECT bit provides information to the user on whether or not the sector protection has been enabled or disabled, either by the software-controlled method or the hardware-controlled method.

#### 10.4.5 PAGE SIZE Bit

The PAGE SIZE bit indicates whether the buffer size and the page size of the main memory array is configured for the “power of 2” binary page size (256 bytes) or the standard DataFlash page size (264 bytes).

#### 10.4.6 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit is set to the logic 1 state. The EPE bit is not set if an erase or program operation aborts for any reason, such as an attempt to erase

or program a protected region or a locked down sector or an attempt to erase or program a suspended sector. The EPE bit is updated after every erase and program operation.

#### **10.4.7 SLE Bit**

The SLE bit indicates whether or not the Sector Lockdown command is enabled or disabled. If the SLE bit is a logic 1, then the Sector Lockdown command is still enabled and sectors can be locked down. If the SLE bit is a logic 0, then the Sector Lockdown command has been disabled and no further sectors can be locked down.

#### **10.4.8 PS2 Bit**

The PS2 bit indicates if a program operation has been suspended while using Buffer 2. If the PS2 bit is a logic 1, then a program operation has been suspended while Buffer 2 was being used, and any command attempts that can modify the contents of Buffer 2 are ignored.

#### **10.4.9 PS1 Bit**

The PS1 bit indicates if a program operation has been suspended while using Buffer 1. If the PS1 bit is a logic 1, then a program operation has been suspended while Buffer 1 was being used, and any command attempts that can modify the contents of Buffer 1 are ignored.

#### **10.4.10 The ES bit**

The ES bit indicates whether or not an erase has been suspended. If the ES bit is a logic 1, then an erase operation (page, block, sector, or chip) has been suspended.

## 11. Deep Power-Down

During normal operation, the device is placed in the standby mode to consume less power as long as the  $\overline{CS}$  pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, all commands including the Status Register Read command are ignored with the exception of the Resume from Deep Power-Down command. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is done by asserting the  $\overline{CS}$  pin, clocking in the opcode B9h, and then deasserting the  $\overline{CS}$  pin. Any additional data clocked into the device after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the device enters the Deep Power-Down mode within the maximum time of  $t_{EDPD}$ .

The complete opcode must be clocked in before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and return to the standby mode once the  $\overline{CS}$  pin is deasserted. Also, the device defaults to the standby mode after a power cycle.

The Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

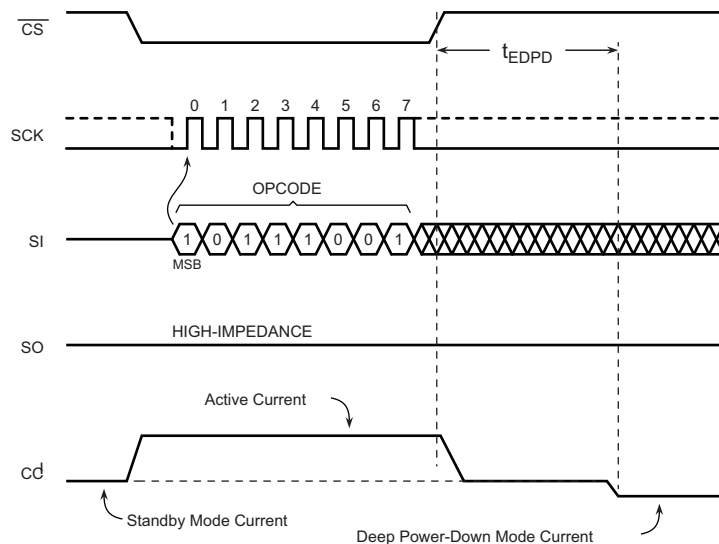


Figure 16. Deep Power-Down Timing

### 11.1 Resume from Deep Power-Down

In order to exit the Deep Power-Down mode and resume normal device operation, the Resume from Deep Power-Down command must be issued. The Resume from Deep Power-Down command is the only command that the device recognizes while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the  $\overline{CS}$  pin must first be asserted and then the opcode ABh must be clocked into the device. Any additional data clocked into the device after the opcode is ignored. When the  $\overline{CS}$  pin is deasserted, the device exits the Deep Power-Down mode and return to the standby mode within the maximum time of  $t_{RDPD}$ . After the device has returned to the standby mode, normal command operations such as Continuous Array Read can be resumed.

If the complete opcode is not clocked in before the  $\overline{CS}$  pin is deasserted, or if the  $\overline{CS}$  pin is not deasserted on an even byte boundary (multiples of eight bits), then the device aborts the operation and return to the Deep Power-Down mode.

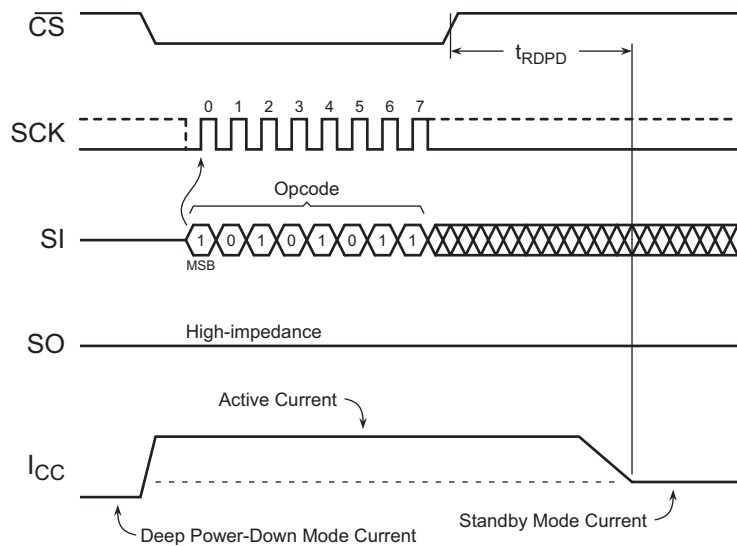


Figure 17. Resume from Deep Power-Down Timing

## 11.2 Ultra-Deep Power-Down

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry. Since almost all active circuitry is shutdown in this mode to conserve power, the contents of the SRAM buffers cannot be maintained. Therefore, any data stored in the SRAM buffers is lost once the device enters the Ultra-Deep Power-Down mode.

When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands are ignored. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is done by asserting the  $\overline{CS}$  pin, clocking in the opcode 79h, and then deasserting the  $\overline{CS}$  pin. Any additional data clocked into the device after the opcode is ignored. When the  $\overline{CS}$  pin is deasserted, the device enters the Ultra-Deep Power-Down mode within the maximum time of  $t_{EUDPD}$ .

The complete opcode must be clocked in before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and return to the standby mode once the  $\overline{CS}$  pin is deasserted. Also, the device defaults to the standby mode after a power cycle.

The Ultra-Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

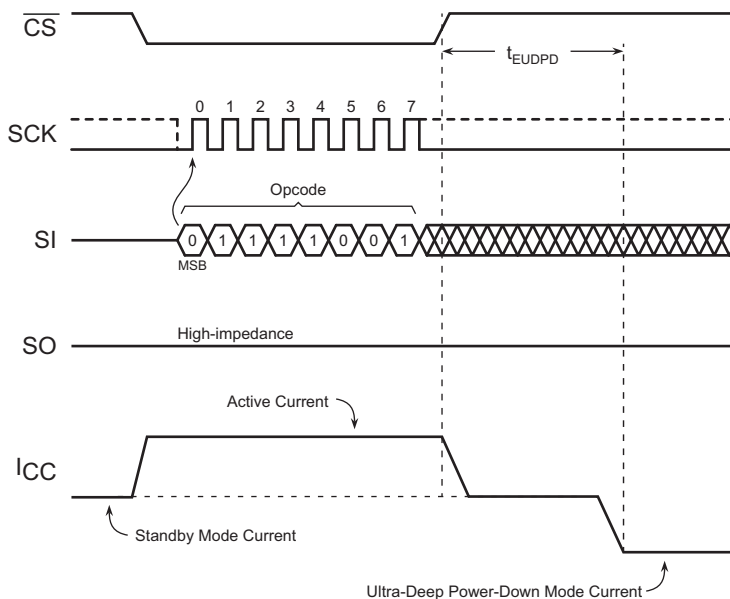


Figure 18. Ultra-Deep Power-Down Timing

### 11.3 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the  $\overline{CS}$  pin must be pulsed by asserting the  $\overline{CS}$  pin, waiting the minimum necessary  $t_{CSLU}$  time, and then deasserting the  $\overline{CS}$  pin again. To facilitate simple software development, a dummy byte opcode can also be entered while the  $\overline{CS}$  pin is being pulsed just as in a normal operation like the Program Suspend operation; the dummy byte opcode is ignored by the device in this case. After the  $\overline{CS}$  pin has been deasserted, the device exits from the Ultra-Deep Power-Down mode and return to the standby mode within a maximum time of  $t_{XUDDP}$ . If the  $\overline{CS}$  pin is reasserted before the  $t_{XUDDP}$  time has elapsed in an attempt to start a new operation, then that operation is ignored and nothing is performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

Since the contents of the SRAM buffers cannot be maintained while in the Ultra-Deep Power-Down mode, the SRAM buffers are going to contain undefined data when the device returns to the standby mode.

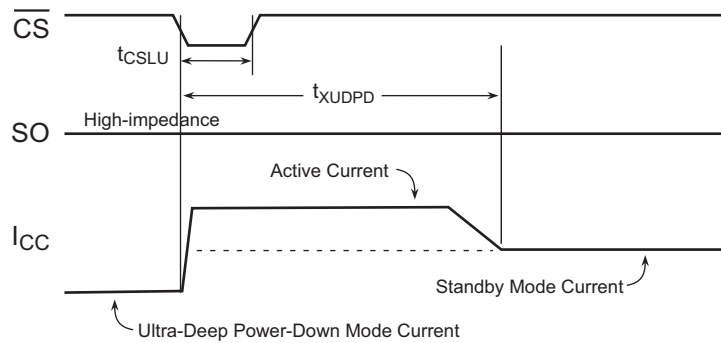


Figure 19. Exit Ultra-Deep Power-Down



## 12. Buffer and Page Size Configuration

The memory array of DataFlash devices is actually larger than other Serial Flash devices in that extra user-accessible bytes are provided in each page of the memory array. For the AT45DB041E, there are an extra eight bytes of memory in each page for a total of an extra 16 kB (128 kbits) of user-accessible memory.

Some applications, however, might not want to take advantage of this extra memory and instead architect their software to operate on a “power of 2” binary, logical addressing scheme. To allow this, the DataFlash can be configured so that the buffer and page sizes are 256 bytes instead of the standard 264 bytes. Also, the configuration of the buffer and page sizes is reversible and can be changed from 264 bytes to 256 bytes or from 256 bytes to 264 bytes. The configured setting is stored in an internal nonvolatile register so that the buffer and page size configuration is not affected by power cycles. The nonvolatile register has a limit of 10,000 erase/program cycles; therefore, take care to not switch between the size options more than 10,000 times.

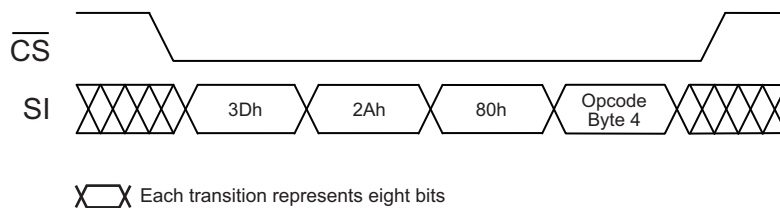
Devices are initially shipped from Adesto with the buffer and page sizes set to 264 bytes. Devices can be ordered from Adesto pre-configured for the “power of 2” binary size of 256 bytes. For details, see [Section 28, Ordering Information on page 70](#).

To configure the device for “power of 2” binary page size (256 bytes), a four-byte opcode sequence of 3Dh, 2Ah, 80h, and A6h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the  $\overline{CS}$  pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. Programming nonvolatile register takes a time of  $t_{EP}$ , during which time the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the configuration process and register program cycle in order for the buffer and page size to be configured to 256 bytes.

To configure the device for standard DataFlash page size (264 bytes), a four-byte opcode sequence of 3Dh, 2Ah, 80h, and A7h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the  $\overline{CS}$  pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. Programming nonvolatile register takes a time of  $t_{EP}$ , during which time the RDY/ $\overline{BUSY}$  bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the configuration process and register program cycle in order for the buffer and page size to be configured to 264 bytes.

**Table 22. Buffer and Page Size Configuration Commands**

“Power of 2” binary page size (256 bytes)	3Dh	2Ah	80h	A6h
DataFlash page size (264 bytes)	3Dh	2Ah	80h	A7h



**Figure 20. Buffer and Page Size Configuration**

### 13. Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC Standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information.

The Read Manufacturer and Device ID command is limited to a maximum clock frequency of  $f_{CLK}$ . Since not all Flash devices are capable of operating at very high clock frequencies, design applications to read the identification information from the devices at a reasonably low clock frequency to ensure that all devices to be used in the application can be identified properly. Once the identification process is complete, the application can then increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the  $\overline{CS}$  pin must first be asserted and then the opcode 9Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output is the Manufacturer ID, followed by two bytes of the Device ID information. The fourth byte output is the Extended Device Information (EDI) String Length, which is 01h indicating that one byte of EDI data follows. After the one byte of EDI data is output, the SO pin goes into a high-impedance state; therefore, additional clock cycles are going to have no affect on the SO pin and no data is output. As indicated in the JEDEC Standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the  $\overline{CS}$  pin terminates the Manufacturer and Device ID Read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

**Table 23. Manufacturer and Device ID Information**

Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Byte 1)	24h
3	Device ID (Byte 2)	00h
4	Extended Device Information (EDI) String Length	01h
5	[Optional to Read] EDI Byte 1	00h

**Table 24. Manufacturer and Device ID Details**

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC code: 0001 1111 (1Fh for Adesto)
	0	0	0	1	1	1	1	1		
Device ID (Byte 1)	Family Code			Density Code					24h	Family code: 001 (AT45Dxxx Family) Density code: 00100 (Four Mbit)
	0	0	1	0	0	1	0	0		
Device ID (Byte 2)	Sub Code			Product Variant					00h	Sub code: 000 (Standard Series) Product variant:00000
	0	0	0	0	0	0	0	0		

Table 25. EDI Data

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
5	RFU			Device Revision					00h	RFU: Reserved for Future Use Device revision: 00000 (Initial Version)
	0	0	0	0	0	0	0	0		

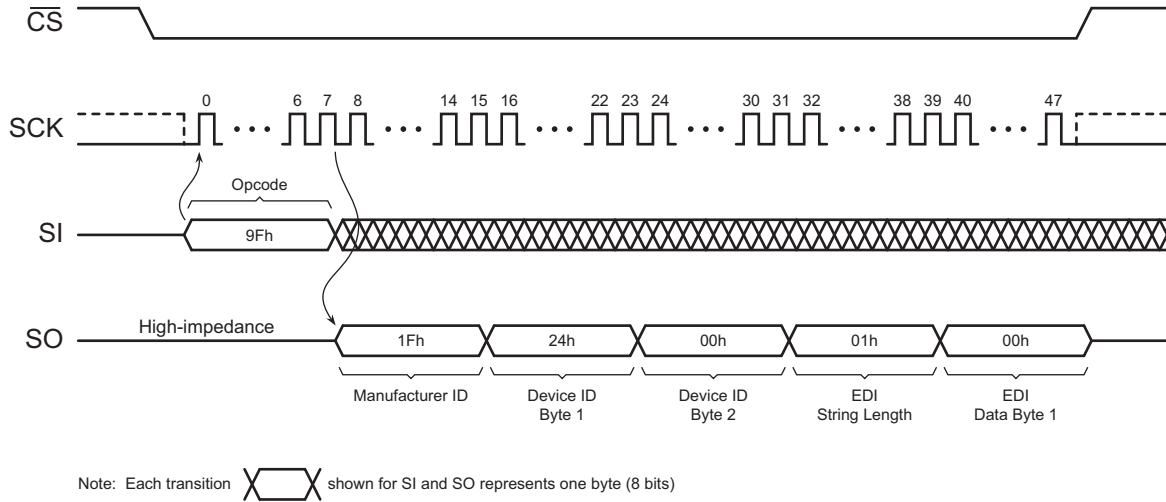


Figure 21. Read Manufacturer and Device ID Timing

## 14. Software Reset

In some applications, it can be necessary to prematurely terminate a program or erase cycle early rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Software Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state.

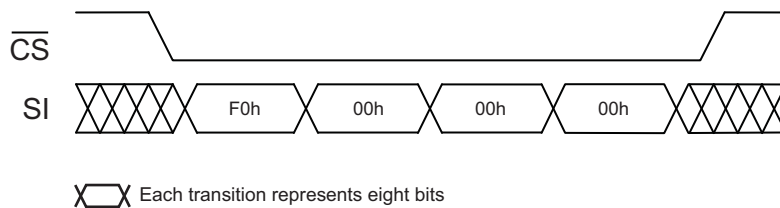
To perform a Software Reset, the  $\overline{CS}$  pin must be asserted and a four-byte command sequence of F0h, 00h, 00h, and 00h must be clocked into the device. Any additional data clocked into the device after the last byte is ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently in progress is terminated within a time  $t_{SWRST}$ . Since the program or erase operation might not complete before the device is reset, the contents of the page being programmed or erased cannot be guaranteed to be valid.

The Software Reset command has no effect on the states of the Sector Protection Register, the Sector Lockdown Register, or the buffer and page size configuration. The PS2, PS1, and ES bits of the Status Register, however, are reset back to their default states. If a Software Reset operation is performed while a sector is erase suspended, the suspend operation aborts and the contents of the page or block being erased in the suspended sector are left in an undefined state. If a Software Reset is performed while a sector is program suspended, the suspend operation aborts and the contents of the page that was being programmed and subsequently suspended are undefined. The remaining pages in the sector retain their previous contents.

The complete four-byte opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no reset operation is performed.

**Table 26. Software Reset**

Command	Byte 1	Byte 2	Byte 3	Byte 4
Software Reset	F0h	00h	00h	00h



**Figure 22. Software Reset**

## 15. Operation Mode Summary

The commands described previously can be grouped into four different categories to better describe which commands can be executed at what times.

### Group A commands consist of:

1. Main Memory Page Read
2. Continuous Array Read (SPI)
3. Read Sector Protection Register
4. Read Sector Lockdown Register
5. Read Security Register
6. Buffer 1 (or 2) Read

### Group B commands consist of:

1. Page Erase
2. Block Erase
3. Sector Erase
4. Chip Erase
5. Main Memory Page to Buffer 1 (or 2) Transfer
6. Main Memory Page to Buffer 1 (or 2) Compare
7. Buffer 1 (or 2) to Main Memory Page Program with Built-In Erase
8. Buffer 1 (or 2) to Main Memory Page Program without Built-In Erase
9. Main Memory Page Program through Buffer 1 (or 2) with Built-In Erase
10. Main Memory Byte/Page Program through Buffer 1 without Built-In Erase
11. Auto Page Rewrite
12. Read-Modify-Write

### Group C commands consist of:

1. Buffer 1 (or 2) Write
2. Status Register Read
3. Manufacturer and Device ID Read

### Group D commands consist of:

1. Erase Sector Protection Register
2. Program Sector Protection Register
3. Sector Lockdown
4. Program Security Register
5. Buffer and Page Size Configuration
6. Freeze Sector Lockdown

If a Group A command is in progress (not fully completed), do not start another command in Group A, B, C, or D. However, during the internally self-timed portion of Group B commands, any command in Group C can be executed. The Group B commands using Buffer 1 must use Group C commands using Buffer 2 and vice versa. Finally, during the internally self-timed portion of a Group D command, execute only the Status Register Read command.

Most of the commands in Group B can be suspended and resumed, except the Buffer Transfer, Buffer Compare, Auto Page Rewrite and Read-Modify-Write operations. If a Group B command is suspended, all of the Group A commands can be executed. See [Table 5](#) to determine which of the Group B, Group C, and Group D commands are allowed.

## 16. Command Tables

**Table 27. Read Commands**

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (High Frequency)	1Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Buffer 1 Read (Low Frequency)	D1h
Buffer 2 Read (Low Frequency)	D3h
Buffer 1 Read (High Frequency)	D4h
Buffer 2 Read (High Frequency)	D6h

**Table 28. Program and Erase Commands**

Command	Opcode
Buffer 1 Write	84h
Buffer 2 Write	87h
Buffer 1 to Main Memory Page Program with Built-In Erase	83h
Buffer 2 to Main Memory Page Program with Built-In Erase	86h
Buffer 1 to Main Memory Page Program without Built-In Erase	88h
Buffer 2 to Main Memory Page Program without Built-In Erase	89h
Main Memory Page Program through Buffer 1 with Built-In Erase	82h
Main Memory Page Program through Buffer 2 with Built-In Erase	85h
Main Memory Byte/Page Program through Buffer 1 without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah
Program/Erase Suspend	B0h
Program/Erase Resume	D0h
Read-Modify-Write through Buffer 1	58h
Read-Modify-Write through Buffer 2	59h

Table 29. Protection and Security Commands

Command	Opcode
Enable Sector Protection	3Dh + 2Ah + 7Fh + A9h
Disable Sector Protection	3Dh + 2Ah + 7Fh + 9Ah
Erase Sector Protection Register	3Dh + 2Ah + 7Fh + CFh
Program Sector Protection Register	3Dh + 2Ah + 7Fh + FCh
Read Sector Protection Register	32h
Sector Lockdown	3Dh + 2Ah + 7Fh + 30h
Read Sector Lockdown Register	35h
Freeze Sector Lockdown	34h + 55h + AAh + 40h
Program Security Register	9Bh + 00h + 00h + 00h
Read Security Register	77h

Table 30. Additional Commands

Command	Opcode
Main Memory Page to Buffer 1 Transfer	53h
Main Memory Page to Buffer 2 Transfer	55h
Main Memory Page to Buffer 1 Compare	60h
Main Memory Page to Buffer 2 Compare	61h
Auto Page Rewrite	58h
Auto Page Rewrite	59h
Deep Power-Down	B9h
Resume from Deep Power-Down	ABh
Ultra-Deep Power-Down	79h
Status Register Read	D7h
Manufacturer and Device ID Read	9Fh
Configure "Power of 2" (Binary) Page Size	3Dh + 2Ah + 80h + A6h
Configure Standard DataFlash Page Size	3Dh + 2Ah + 80h + A7h
Software Reset	F0h + 00h + 00h + 00h

Table 31. Legacy Commands<sup>1</sup>

Command	Opcode
Buffer 1 Read	54H
Buffer 2 Read	56H
Main Memory Page Read	52H
Continuous Array Read	68H
Status Register Read	57H

1. Legacy commands are not recommended for new designs.

Table 32. Detailed Bit-level Addressing Sequence for Binary Page Size (256 bytes)

Page Size = 256 bytes										Address Byte					Address Byte					Address Byte					Added Dummy Bytes									
Opcode	Opcode									Reserved	Reserved	Reserved	Reserved	Reserved	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9		A8	A7	A6	A5	A4	A3	A2	A1	A0
01h	0	0	0	0	0	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
02h	0	0	0	0	0	0	1	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
03h	0	0	0	0	0	0	1	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
0Bh	0	0	0	0	1	0	1	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1	
1Bh	0	0	0	1	1	0	1	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	2	
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
50h	0	1	0	1	0	0	0	0	X	X	X	X	X	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	N/A	
53h	0	1	0	1	0	0	1	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
55h	0	1	0	1	0	1	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
58h <sup>(1)</sup>	0	1	0	1	1	0	0	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
59h <sup>(1)</sup>	0	1	0	1	1	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
58h <sup>(2)</sup>	0	1	0	1	1	0	0	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
59h <sup>(2)</sup>	0	1	0	1	1	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
60h	0	1	1	0	0	0	0	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
61h	0	1	1	0	0	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
79h	0	1	1	1	1	0	0	1	N/A					N/A					N/A					N/A										
7Ch	0	1	1	1	1	1	0	0	X	X	X	X	X	A	A	A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
81h	1	0	0	0	0	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	N/A	
82h	1	0	0	0	0	0	1	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
83h	1	0	0	0	0	0	1	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
85h	1	0	0	0	0	1	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A	
86h	1	0	0	0	0	1	1	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
89h	1	0	0	0	1	0	0	1	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A	
9Fh	1	0	0	1	1	1	1	1	N/A					N/A					N/A					N/A										
B9h	1	0	1	1	1	0	0	1	N/A					N/A					N/A					N/A										
ABh	1	0	1	0	1	0	1	1	N/A					N/A					N/A					N/A										
B0h	1	0	1	1	0	0	0	0	N/A					N/A					N/A					N/A										
D0h	1	1	0	1	0	0	0	0	N/A					N/A					N/A					N/A										
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	N/A	
D2h	1	1	0	1	0	0	1	0	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4	
D3h	1	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	1
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1	N/A					N/A					N/A					N/A										

1. Shown to indicate when the Auto Page Rewrite operation is executed.
2. Shown to indicate when the Read-Modify-Write operation is executed.
3. X = Dummy bit.



Table 33. Detailed Bit-Level Addressing Sequence for Standard DataFlash Page Size (264 bytes)

Page Size = 264 bytes										Address Byte				Address Byte								Address Byte								Added Dummy Bytes			
Opcode		Opcode								Reserved	Reserved	Reserved	Reserved	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA8	BA7	BA6	BA5	BA4		BA3	BA2	BA1
01h	0	0	0	0	0	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
02h	0	0	0	0	0	0	1	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
03h	0	0	0	0	0	0	1	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
0Bh	0	0	0	0	1	0	1	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	1	
1Bh	0	0	0	1	1	0	1	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	2	
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
50h	0	1	0	1	0	0	0	0	X	X	X	X	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	N/A	
53h	0	1	0	1	0	0	1	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
55h	0	1	0	1	0	1	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
58h <sup>(1)</sup>	0	1	0	1	1	0	0	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
59h <sup>(1)</sup>	0	1	0	1	1	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
58h <sup>(2)</sup>	0	1	0	1	1	0	0	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
59h <sup>(2)</sup>	0	1	0	1	1	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
60h	0	1	1	0	0	0	0	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
61h	0	1	1	0	0	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A	
79h	0	1	1	1	1	0	0	1	N/A				N/A				N/A								N/A								
7Ch	0	1	1	1	1	1	0	0	X	X	X	X	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	N/A	
81h	1	0	0	0	0	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	N/A	
82h	1	0	0	0	0	0	1	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
83h	1	0	0	0	0	0	1	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	N/A	
85h	1	0	0	0	0	1	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	N/A	
86h	1	0	0	0	0	1	1	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	N/A	
88h	1	0	0	0	1	0	0	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
89h	1	0	0	0	1	0	0	1	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	N/A	
9Fh	1	0	0	1	1	1	1	1	N/A				N/A				N/A								N/A								
B9h	1	0	1	1	1	0	0	1	N/A				N/A				N/A								N/A								
ABh	1	0	1	0	1	0	1	1	N/A				N/A				N/A								N/A								
B0h	1	0	1	1	0	0	0	0	N/A				N/A				N/A								N/A								
D0h	1	1	0	1	0	0	0	0	N/A				N/A				N/A								N/A								
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	N/A	
D2h	1	1	0	1	0	0	1	0	X	X	X	X	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	4	
D3h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	N/A	
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	1	
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	1	
D7h	1	1	0	1	0	1	1	1	N/A				N/A				N/A								N/A								

1. Shown to indicate when the Auto Page Rewrite operation is executed.  
 2. Shown to indicate when the Read-Modify-Write operation is executed.  
 3. P = Page Address bit; B = Byte/Buffer Address bit; X = Dummy bit.

## 17. Power-On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the output pin (SO) is in a high impedance state, and a high-to-low transition on the  $\overline{CS}$  pin is required to start a valid instruction. The SPI mode (3 or 0) is automatically selected on every falling edge of  $\overline{CS}$  by sampling the inactive clock state.

### 17.1 Power-Up/Power-Down Voltage and Timing Requirements

As the device initializes, there is a transient current demand. The system needs to be capable of providing this current to ensure correct initialization. During power-up, the device must not be READ for at least the minimum  $t_{VCSL}$  time after the supply voltage reaches the minimum  $V_{POR}$  level ( $V_{POR\ min}$ ). While the device is being powered-up, the internal Power-On Reset (POR) circuitry keeps the device in a reset mode until the supply voltage rises above the minimum  $V_{CC}$ . During this time, all operations are disabled and the device does not respond to any commands.

If the first operation to the device after power-up is a program or erase operation, then the operation cannot be started until the supply voltage reaches the minimum  $V_{CC}$  level and an internal device delay has elapsed. This delay is a maximum time of  $t_{PUW}$ . After the  $t_{PUW}$  time, the device goes in to standby mode if  $\overline{CS}$  is at logic high or active mode if  $\overline{CS}$  is at logic low. For the case of Power-down then Power-up operation, or if a power interruption occurs (such that  $V_{CC}$  drops below  $V_{POR\ max}$ ), the  $V_{CC}$  of the Flash device must be maintained below  $V_{PWD}$  for at least the minimum specified  $T_{PWD}$  time. This is to ensure the Flash device resets properly after a power interruption.

Table 34. Voltage and Timing Requirements for Power-Up/Power-Down

Symbol	Parameter	Min	Max	Units
$V_{PWD}^1$	$V_{CC}$ for device initialization		1.0	V
$t_{PWD(1)}$	Minimum duration for device initialization	300		$\mu s$
$t_{VCSL}$	Minimum $V_{CC}$ to chip select low time for Read command	70		$\mu s$
$t_{VR(1)}$	$V_{CC}$ rise time	1	500000	$\mu s/V$
$V_{POR}$	Power on reset voltage	1.45	1.6	V
$t_{PUW}$	Power up delay time before Program or Erase is allowed		3	ms

1. Not 100% tested (value guaranteed by design and characterization).

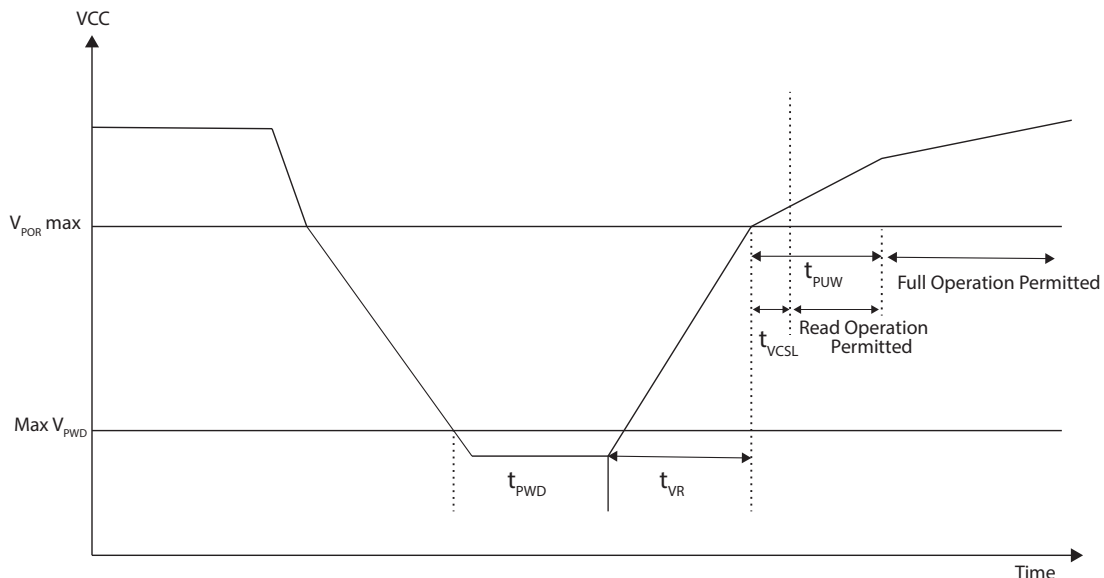


Figure 23. Power-Up Timing

## 18. System Considerations

The serial interface is controlled by the Serial Clock (SCK), Serial Input (SI), and Chip Select ( $\overline{\text{CS}}$ ) pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. PCB traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash devices occurs during the programming and erasing operations. The supply voltage regulator needs to be able to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erasing can lead to improper operation and possible data corruption.

## 19. Electrical Specifications

### 19.1 Absolute Maximum Ratings

Temperature under Bias . . . . .	-55°C to +125°C
Storage Temperature. . . . .	-65°C to +150°C
Absolute Maximum $V_{CC}$ . . . . .	3.96 V
All Output Voltages with Respect to Ground . . . . .	-0.6 V to 4.2 V (Max $V_{CC}$ of 3.6 V + 0.6 V)
All Input Voltages with Respect to Ground (excluding $V_{CC}$ pin, including NC pins) . . . . .	-0.6 V to 4.2 V (Max $V_{CC}$ of 3.6 V + 0.6 V)

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

### 19.2 DC and AC Operating Range

Table 35. Operating Ranges

	AT45DB041E
Operating Temperature (Case)	-40°C to +85°C ( $V_{CC}$ Power Supply 1.65 V to 3.6 V)
	-40°C to +125°C ( $V_{CC}$ Power Supply 2.3 V to 3.6 V)
$V_{CC}$ Power Supply	1.65 V to 3.6 V

## 19.3 DC Characteristics

Table 36. DC Characteristics (-40°C to +85°C)

Symbol	Parameter	Condition	1.65 V to 3.6 V			2.3 V to 3.6 V			Units
			Min	Typ	Max	Min	Typ	Max	
$I_{UDPD}$	Ultra-Deep Power-Down Current	$\overline{CS} = V_{CC}$ . All other inputs at 0V or $V_{CC}$		0.4	1		0.4	1	$\mu A$
$I_{DPD}$	Deep Power-Down Current	$\overline{CS} = V_{CC}$ . All other inputs at 0V or $V_{CC}$		4.5	12		5	12	$\mu A$
$I_{SB}$	Standby Current	$\overline{CS} = V_{CC}$ . All other inputs at 0 V or $V_{CC}$		25	40		25	40	$\mu A$
$I_{CC1}^1$	Active Current, Low Power Read (01h) Operation	$f = 1 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		6	9		6	9	mA
		$f = 15 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		7	10		7	10	mA
$I_{CC2}^{1,2}$	Active Current, Read Operation	$f = 50 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		10	12		10	12	mA
		$f = 85 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		12	15		12	15	mA
$I_{CC3}$	Active Current, Program Operation	$\overline{CS} = V_{CC}$		14	16		14	16	mA
$I_{CC4}$	Active Current, Erase Operation	$\overline{CS} = V_{CC}$		8	12		8	12	mA
$I_{LI}$	Input Load Current	All inputs at CMOS levels			1			1	$\mu A$
$I_{LO}$	Output Leakage Current	All inputs at CMOS levels			1			1	$\mu A$
$V_{IL}$	Input Low Voltage				$V_{CC} \times 0.3$			$V_{CC} \times 0.3$	V
$V_{IH}$	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.6$	$V_{CC} \times 0.7$		$V_{CC} + 0.6$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 100 \mu A$			0.4			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2 \text{ V}$			$V_{CC} - 0.2 \text{ V}$			V

1. Typical values measured at 1.8 V at 25°C for the 1.65 V to 3.6 V range.

2. Typical values measured at 3.0 V at 25°C for the 2.3 V to 3.6 V range.

Table 37. DC Characteristics (-40°C to +125°C)

Symbol	Parameter	Condition	1.65 V to 3.6 V			2.3 V to 3.6 V			Units
			Min	Typ	Max	Min	Typ	Max	
$I_{UDPD}$	Ultra-Deep Power-Down Current	$\overline{CS} = V_{CC}$ . All other inputs at 0V or $V_{CC}$		0.4	1		0.4	1	$\mu A$
$I_{DPD}$	Deep Power-Down Current	$\overline{CS} = V_{CC}$ . All other inputs at 0V or $V_{CC}$		4.5	20		5	20	$\mu A$
$I_{SB}$	Standby Current	$\overline{CS} = V_{CC}$ . All other inputs at 0 V or $V_{CC}$		25	45		25	45	$\mu A$
$I_{CC1}^1$	Active Current, Low Power Read (01h) Operation	$f = 1 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		6	9		6	9	mA
		$f = 15 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		7	10		7	10	mA
$I_{CC2}^{1,2}$	Active Current, Read Operation	$f = 50 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		10	12		10	12	mA
		$f = 85 \text{ MHz}; I_{OUT} = 0 \text{ mA}$		12	15		12	15	mA
$I_{CC3}$	Active Current, Program Operation	$\overline{CS} = V_{CC}$		14	20		14	20	mA
$I_{CC4}$	Active Current, Erase Operation	$\overline{CS} = V_{CC}$		8	12		8	12	mA
$I_{LI}$	Input Load Current	All inputs at CMOS levels			1			1	$\mu A$
$I_{LO}$	Output Leakage Current	All inputs at CMOS levels			1			1	$\mu A$
$V_{IL}$	Input Low Voltage				$V_{CC} \times 0.3$			$V_{CC} \times 0.3$	V
$V_{IH}$	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.6$	$V_{CC} \times 0.7$		$V_{CC} + 0.6$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 100 \mu A$			0.4			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2 \text{ V}$			$V_{CC} - 0.2 \text{ V}$			V

1. Typical values measured at 1.8 V at 25°C for the 1.65 V to 3.6 V range.

2. Typical values measured at 3.0 V at 25°C for the 2.3 V to 3.6 V range.

## 19.4 AC Characteristics

Table 38. AC Characteristics (-40°C to +85°C)

Symbol	Parameter	1.65 to 3.6 V		2.3 V to 3.6 V		Units
		Min	Max	Min	Max	
f <sub>SCK</sub>	SCK Frequency		70		85	MHz
f <sub>CAR1</sub>	SCK Frequency for Continuous Read (0x0B)		70		85	MHz
f <sub>CAR2</sub>	SCK Frequency for Continuous Read (0x03) (Low Frequency)		40		50	MHz
f <sub>CAR3</sub>	SCK Frequency for Continuous Read (Low Power Mode – 01h Opcode)		15		15	MHz
f <sub>CAR4</sub>	SCK Frequency for Continuous Read (0x1B)		85		104	
t <sub>WH</sub>	SCK High Time	4		4		ns
t <sub>WL</sub>	SCK Low Time	4		4		ns
t <sub>SCKR</sub> <sup>1</sup>	SCK Rise Time, Peak-to-peak	0.1		0.1		V/ns
t <sub>SCKF</sub> <sup>1</sup>	SCK Fall Time, Peak-to-peak	0.1		0.1		V/ns
t <sub>CS</sub>	Minimum $\overline{CS}$ High Time	20		20		ns
t <sub>CSS</sub>	$\overline{CS}$ Setup Time	6		5		ns
t <sub>CSH</sub>	$\overline{CS}$ Hold Time	5		5		ns
t <sub>SU</sub>	Data In Setup Time	2		2		ns
t <sub>H</sub>	Data In Hold Time	1		1		ns
t <sub>HO</sub>	Output Hold Time	0		0		ns
t <sub>DIS</sub> <sup>□</sup>	Output Disable Time		8		6	ns
t <sub>V</sub>	Output Valid		7		6	ns
t <sub>WPE</sub>	$\overline{WP}$ Low to Protection Enabled		1		1	μs
t <sub>WPD</sub>	$\overline{WP}$ High to Protection Disabled		1		1	μs
t <sub>LOCK</sub>	Freeze Sector Lockdown Time (from $\overline{CS}$ High)		200		200	μs
t <sub>EUDPD</sub> <sup>1</sup>	$\overline{CS}$ High to Ultra-Deep Power-Down		3		3	μs
t <sub>CSLU</sub>	Minimum $\overline{CS}$ Low Time to Exit Ultra-Deep Power-Down	20		20		ns
t <sub>XUDPD</sub>	Exit Ultra-Deep Power-Down Time		280		140	μs
t <sub>EDPD</sub> <sup>1</sup>	$\overline{CS}$ High to Deep Power-Down		2		2	μs
t <sub>RDPD</sub>	Resume from Deep Power-Down Time		35		35	μs
t <sub>XFR</sub>	Page to Buffer Transfer Time		100		100	μs
t <sub>COMP</sub>	Page to Buffer Compare Time		100		100	μs
t <sub>RST</sub>	$\overline{RESET}$ Pulse Width	10		10		μs
t <sub>REC</sub>	$\overline{RESET}$ Recovery Time		1		1	μs
t <sub>SWRST</sub>	Software Reset Time		35		35	μs

1. Values are based on device characterization, not 100% tested in production.

Table 39. AC Characteristics (-40°C to +125°C)

Symbol	Parameter	1.65 to 3.6 V		2.3 V to 3.6 V		Units
		Min	Max	Min	Max	
f <sub>SCK</sub>	SCK Frequency		70		85	MHz
f <sub>CAR1</sub>	SCK Frequency for Continuous Read (0x0B)		70		70	MHz
f <sub>CAR2</sub>	SCK Frequency for Continuous Read (0x03) (Low Frequency)		33		33	MHz
f <sub>CAR3</sub>	SCK Frequency for Continuous Read (Low Power Mode – 01h Opcode)		15		15	MHz
f <sub>CAR4</sub>	SCK Frequency for Continuous Read (0x1B)		85		104	
t <sub>WH</sub>	SCK High Time	4		4		ns
t <sub>WL</sub>	SCK Low Time	4		4		ns
t <sub>SCKR</sub> <sup>1</sup>	SCK Rise Time, Peak-to-peak	0.1		0.1		V/ns
t <sub>SCKF</sub> <sup>1</sup>	SCK Fall Time, Peak-to-peak	0.1		0.1		V/ns
t <sub>CS</sub>	Minimum $\overline{\text{CS}}$ High Time	24		24		ns
t <sub>CSS</sub>	$\overline{\text{CS}}$ Setup Time	6		5		ns
t <sub>CSH</sub>	$\overline{\text{CS}}$ Hold Time	5		5		ns
t <sub>SU</sub>	Data In Setup Time	2		2		ns
t <sub>H</sub>	Data In Hold Time	1		1		ns
t <sub>HO</sub>	Output Hold Time	0		0		ns
t <sub>DIS</sub> <sup>□</sup>	Output Disable Time		8		6	ns
t <sub>V</sub>	Output Valid		8		6	ns
t <sub>WPE</sub>	$\overline{\text{WP}}$ Low to Protection Enabled		1		1	μs
t <sub>WPD</sub>	$\overline{\text{WP}}$ High to Protection Disabled		1		1	μs
t <sub>LOCK</sub>	Freeze Sector Lockdown Time (from $\overline{\text{CS}}$ High)		200		200	μs
t <sub>EUDPD</sub> <sup>1</sup>	$\overline{\text{CS}}$ High to Ultra-Deep Power-Down		3		3	μs
t <sub>CSLU</sub>	Minimum $\overline{\text{CS}}$ Low Time to Exit Ultra-Deep Power-Down	20		20		ns
t <sub>XUDPD</sub>	Exit Ultra-Deep Power-Down Time		280		140	μs
t <sub>EDPD</sub> <sup>1</sup>	$\overline{\text{CS}}$ High to Deep Power-Down		2		2	μs
t <sub>RDPD</sub>	Resume from Deep Power-Down Time		35		35	μs
t <sub>XFR</sub>	Page to Buffer Transfer Time		100		100	μs
t <sub>COMP</sub>	Page to Buffer Compare Time		100		100	μs
t <sub>RST</sub>	$\overline{\text{RESET}}$ Pulse Width	10		10		μs
t <sub>REC</sub>	$\overline{\text{RESET}}$ Recovery Time		1		1	μs
t <sub>SWRST</sub>	Software Reset Time		35		35	μs

1. Values are based on device characterization, not 100% tested in production.



## 19.5 Program and Erase Characteristics

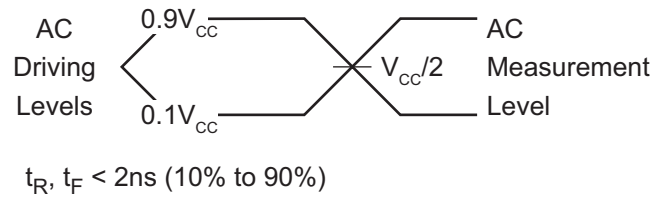
Table 40. Program and Erase Characteristics (-40°C to +85°C)

Symbol	Parameter		1.65 to 3.6 V		2.3 V to 3.6 V		Units
			Typ	Max	Typ	Max	
t <sub>EP</sub>	Page Erase and Programming Time (256/264 bytes)		10	25	15	25	ms
t <sub>P</sub>	Page Programming Time		1.5	3	1.5	3	ms
t <sub>BP</sub>	Byte Programming Time		8		8		μs
t <sub>PE</sub>	Page Erase Time		12	25	12	25	ms
t <sub>BE</sub>	Block Erase Time		30	35	30	35	ms
t <sub>SE</sub>	Sector Erase Time		.7	1.1	.7	1.1	s
t <sub>CE</sub>	Chip Erase Time		6	17	5	17	s
t <sub>SUSP</sub>	Suspend Time	Program	8	15	8	15	μs
		Erase	20	30	20	30	
t <sub>RES</sub>	Resume Time	Program	8	15	8	15	μs
		Erase	20	30	20	30	
t <sub>OTPP</sub>	OTP Security Register Program Time		200	500	200	500	μs

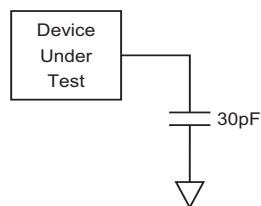
Table 41. Program and Erase Characteristics (-40°C to +125°C)

Symbol	Parameter		1.65 to 3.6 V		2.3 V to 3.6 V		Units
			Typ	Max	Typ	Max	
t <sub>EP</sub>	Page Erase and Programming Time (256/264 bytes)		10	25	15	25	ms
t <sub>P</sub>	Page Programming Time		1.5	3	1.5	3	ms
t <sub>BP</sub>	Byte Programming Time		8		8		μs
t <sub>PE</sub>	Page Erase Time		12	25	12	25	ms
t <sub>BE</sub>	Block Erase Time		30	50	30	50	ms
t <sub>SE</sub>	Sector Erase Time		.7	1.3	.7	1.3	s
t <sub>CE</sub>	Chip Erase Time		6	17	5	17	s
t <sub>SUSP</sub>	Suspend Time	Program	8	15	8	15	μs
		Erase	20	30	20	30	
t <sub>RES</sub>	Resume Time	Program	8	15	8	15	μs
		Erase	20	30	20	30	
t <sub>OTPP</sub>	OTP Security Register Program Time		200	500	200	500	μs

## 20. Input Test Waveforms and Measurement Levels



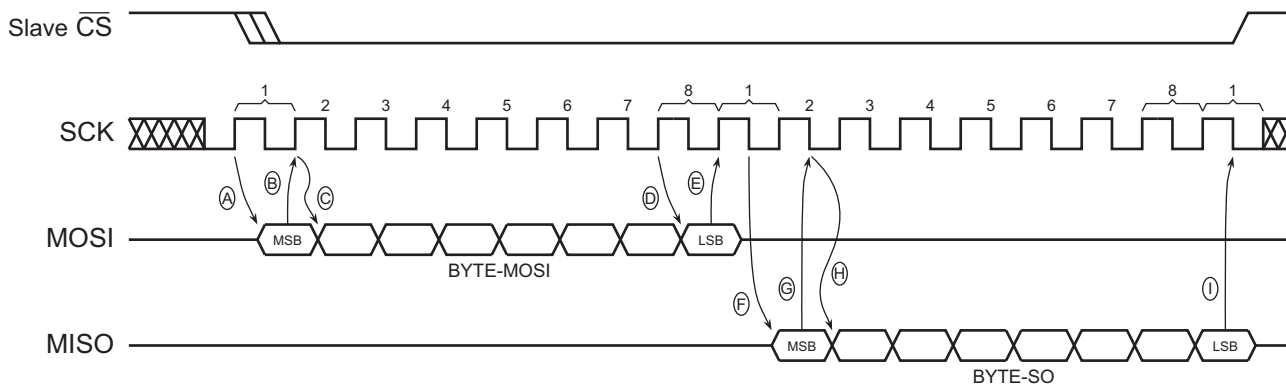
## 21. Output Test Load



## 22. Using the RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller must wait until the next falling edge of SCK to latch the data in. Similarly, the host controller must clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.



MOSI = Master Out, Slave In  
 MISO = Master In, Slave Out  
 The Master is the host controller and the Slave is the DataFlash.

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.  
 The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

- A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
- B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
- C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
- D. Last bit of BYTE-MOSI is clocked out from the Master
- E. Last bit of BYTE-MOSI is clocked into the slave
- F. Slave clocks out first bit of BYTE-SO
- G. Master clocks in first bit of BYTE-SO
- H. Slave clocks out second bit of BYTE-SO
- I. Master clocks in last bit of BYTE-SO

Figure 24. RapidS Mode Timing

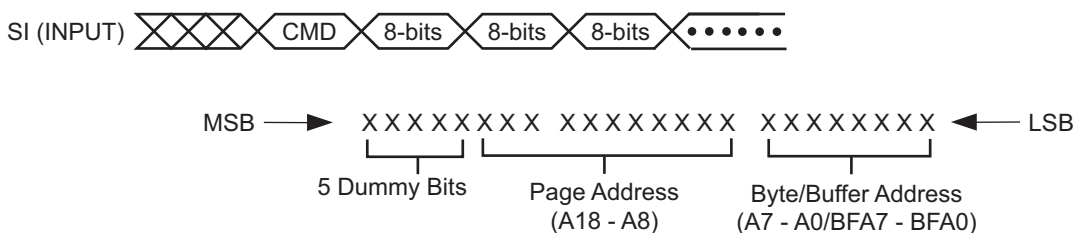


Figure 25. Command Sequence for Read/Write Operations for Page Size 256 bytes  
 (Except Status Register Read, Manufacturer and Device ID Read)

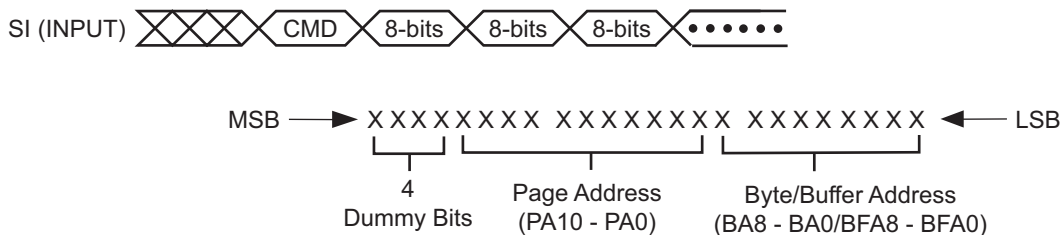
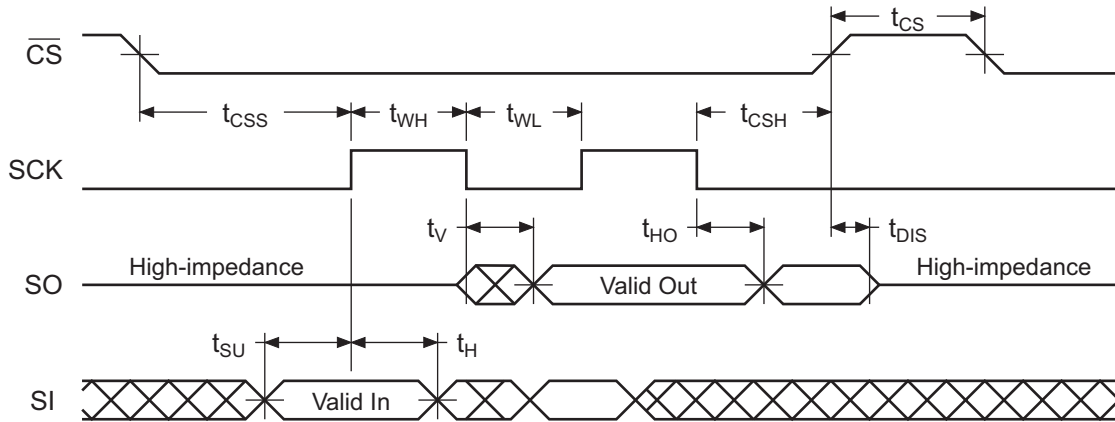


Figure 26. Command Sequence for Read/Write Operations for Page Size 264 bytes  
 (Except Status Register Read, Manufacturer and Device ID Read)

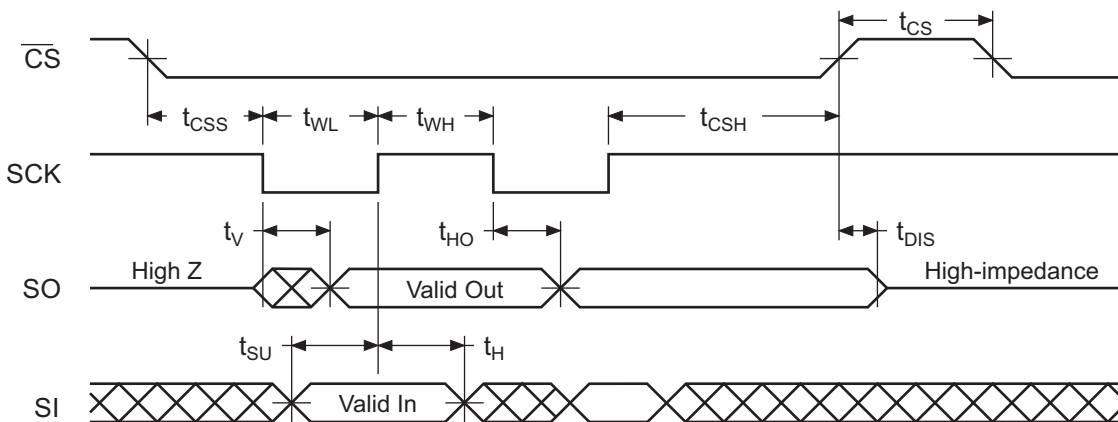
## 23. AC Waveforms

Four different timing waveforms are shown in **Figure 27** through **Figure 30**. Waveform 1 shows the SCK signal being low when  $\overline{CS}$  makes a high-to-low transition and Waveform 2 shows the SCK signal being high when  $\overline{CS}$  makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as  $t_{WL}$ ). Timing Waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 85 MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and 4 illustrate general timing diagram for RapidS serial interface. These are similar to Waveform 1 and 2, except that output SO is not restricted to become valid during the  $t_{WL}$  period. These timing waveforms are valid over the full frequency range (maximum frequency = 85 MHz) of the RapidS serial case.



**Figure 27. Waveform 1 = SPI Mode 0 Compatible**



**Figure 28. Waveform 2 = SPI Mode 3 Compatible**

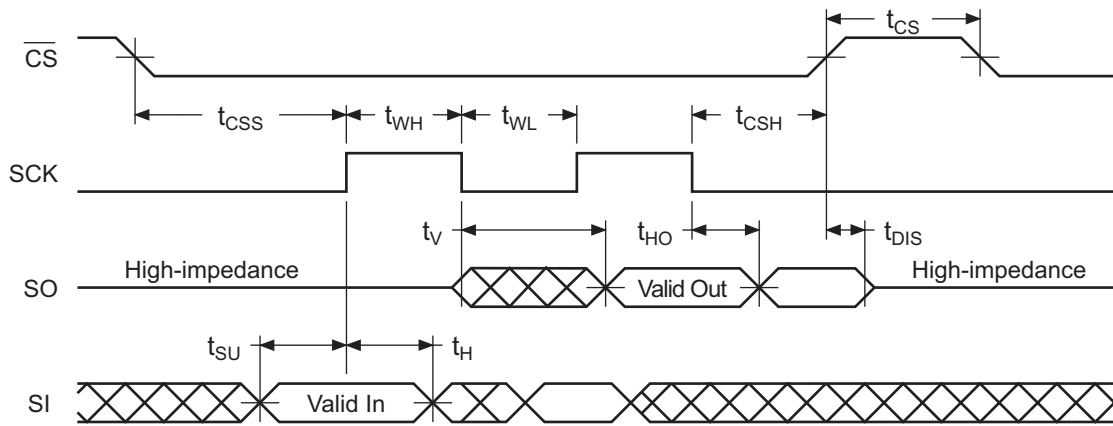


Figure 29. Waveform 3 = RapidS Mode 0

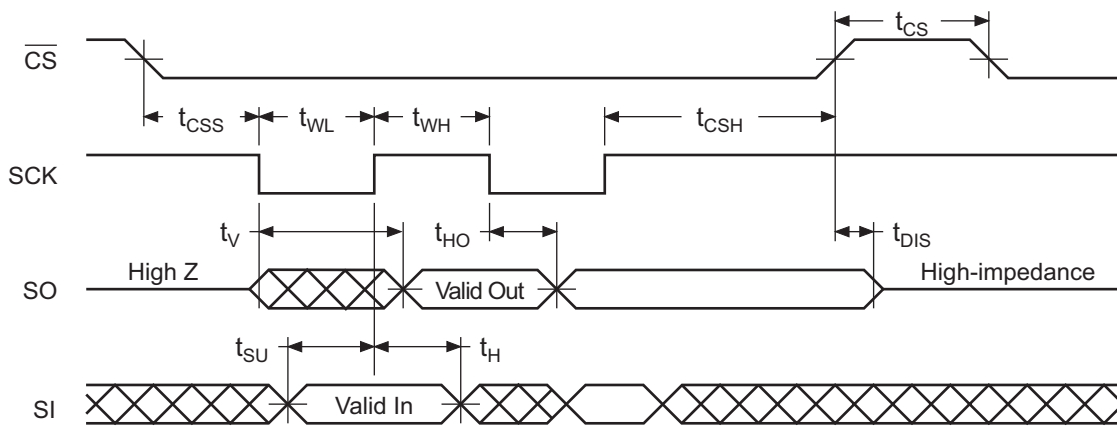


Figure 30. Waveform 4 = RapidS Mode 3

## 24. Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

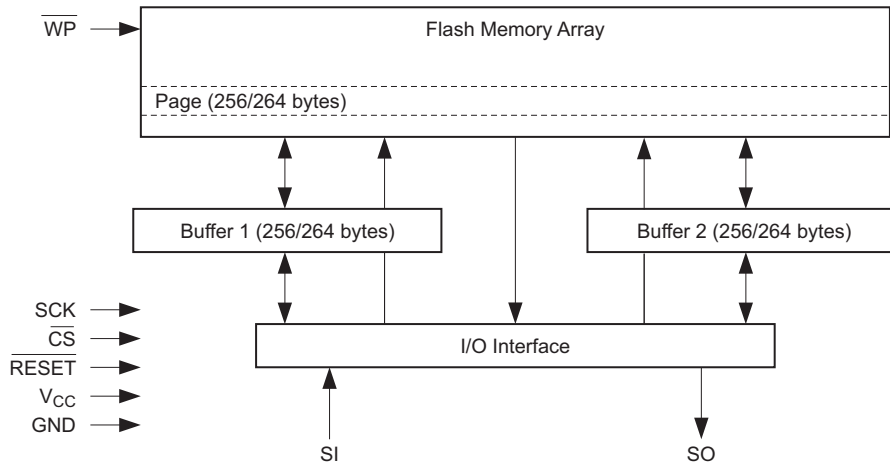


Figure 31. Block Diagram

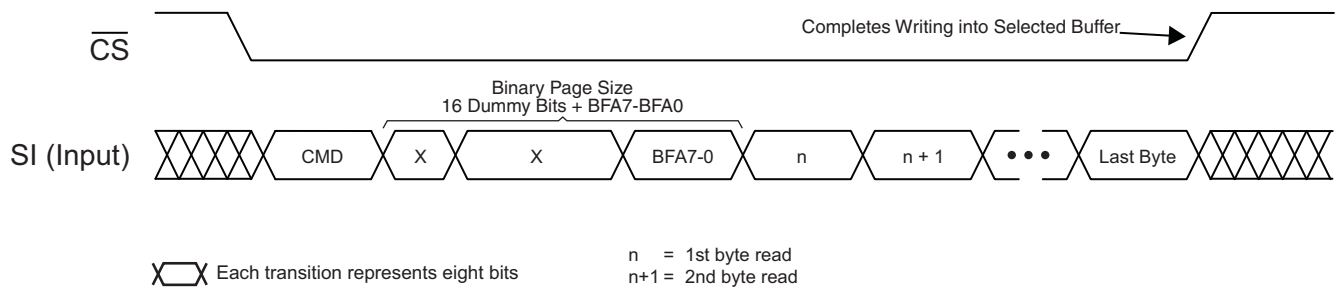


Figure 32. Buffer Write

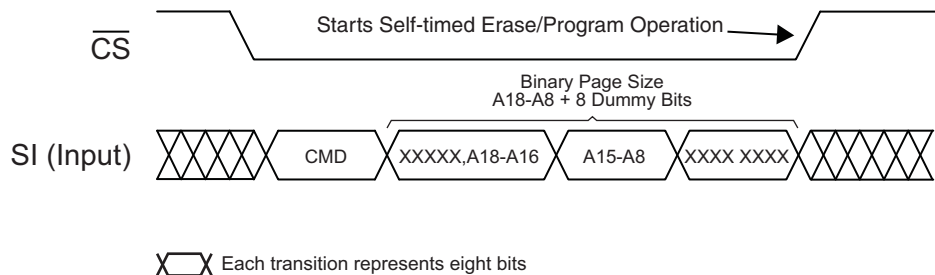


Figure 33. Buffer to Main Memory Page Program

## 25. Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

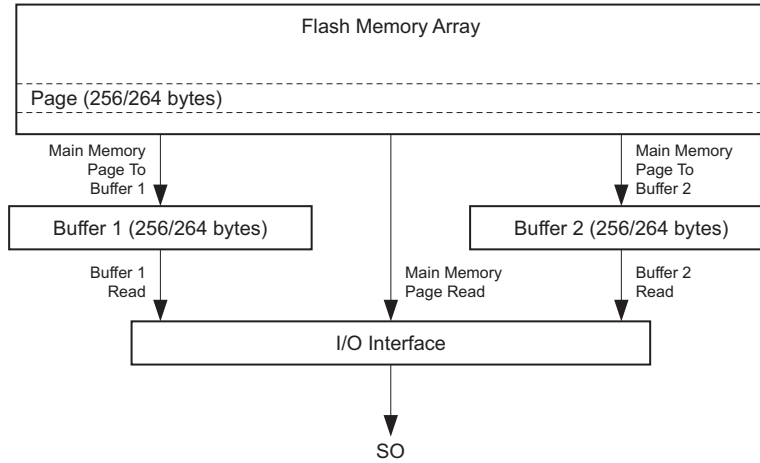


Figure 34. Block Diagram

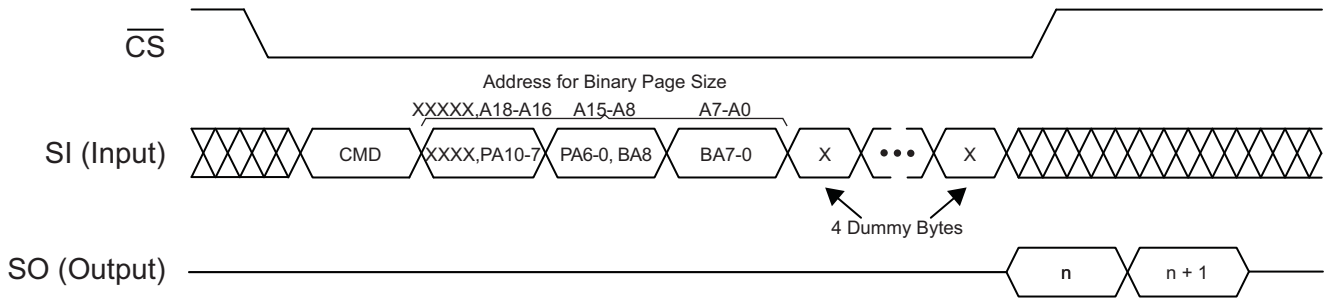


Figure 35. Main Memory Page Read

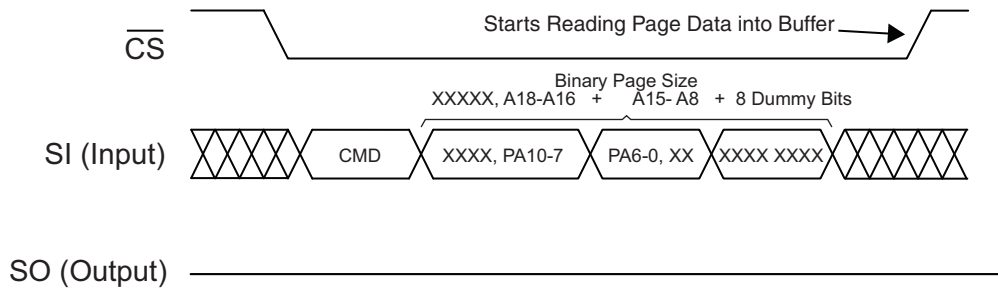


Figure 36. Main Memory Page to Buffer Transfer

Data From the selected Flash Page is read into either SRAM Buffer

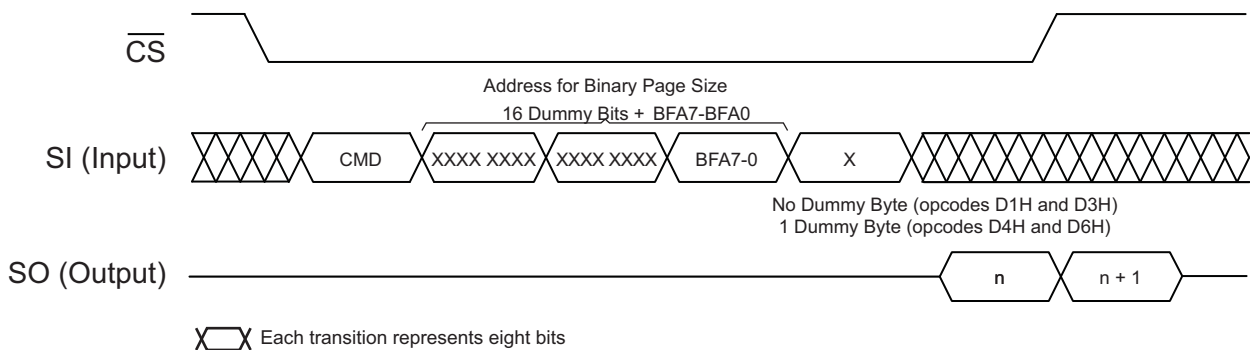


Figure 37. Buffer Read

## 26. Detailed Bit-level Read Waveforms: RapidS Mode 0/Mode 3

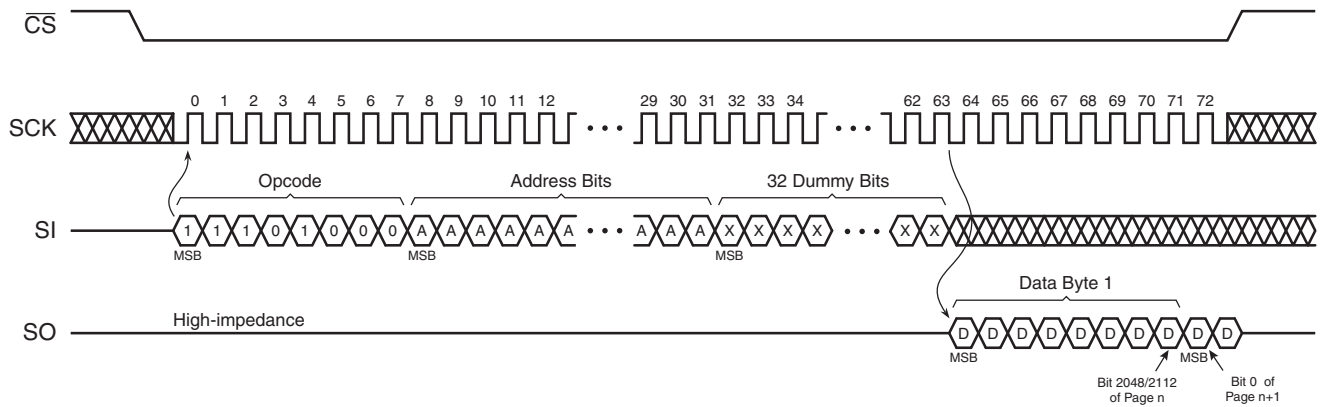


Figure 38. Continuous Array Read Timing (Legacy Opcode E8h)

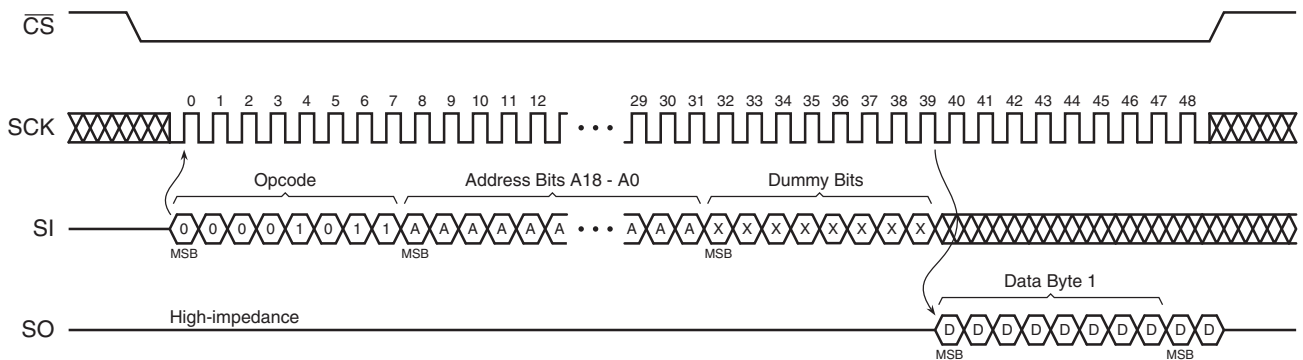


Figure 39. Continuous Array Read Timing (Opcode 0Bh)

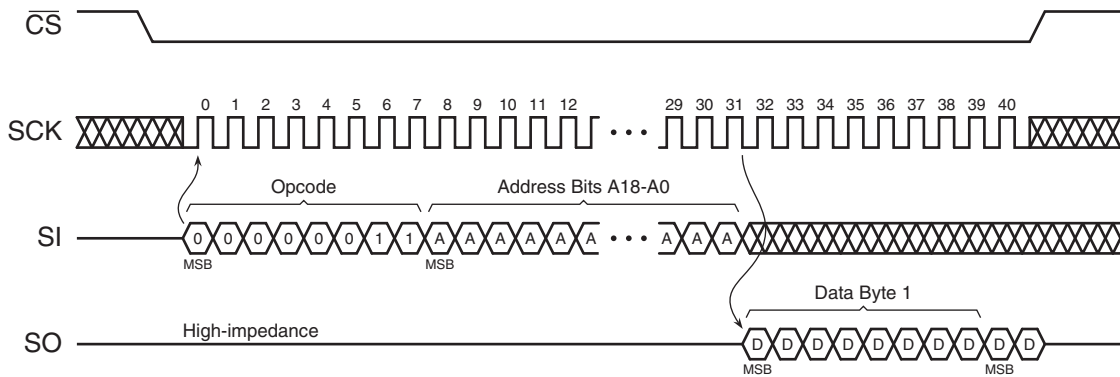


Figure 40. Continuous Array Read Timing (Opcode 01h or 03h)



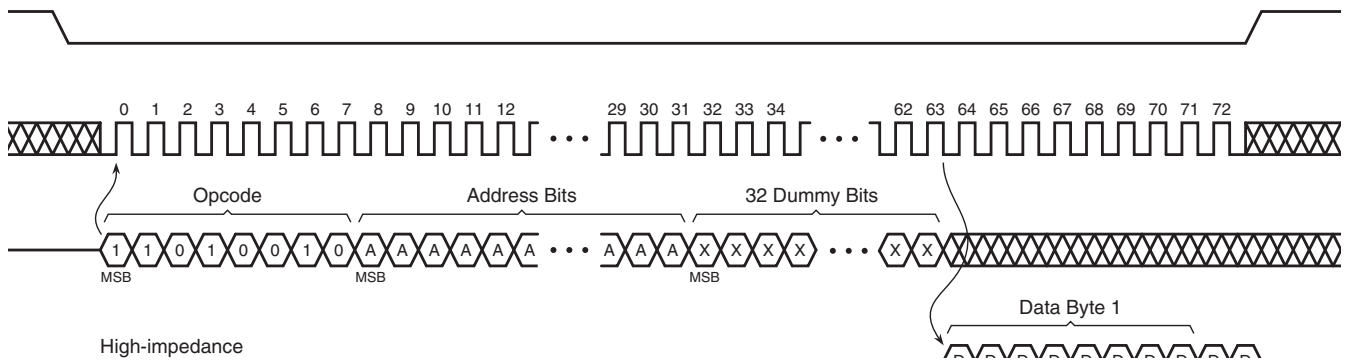


Figure 41. Main Memory Page Read Timing (Opcode D2h)

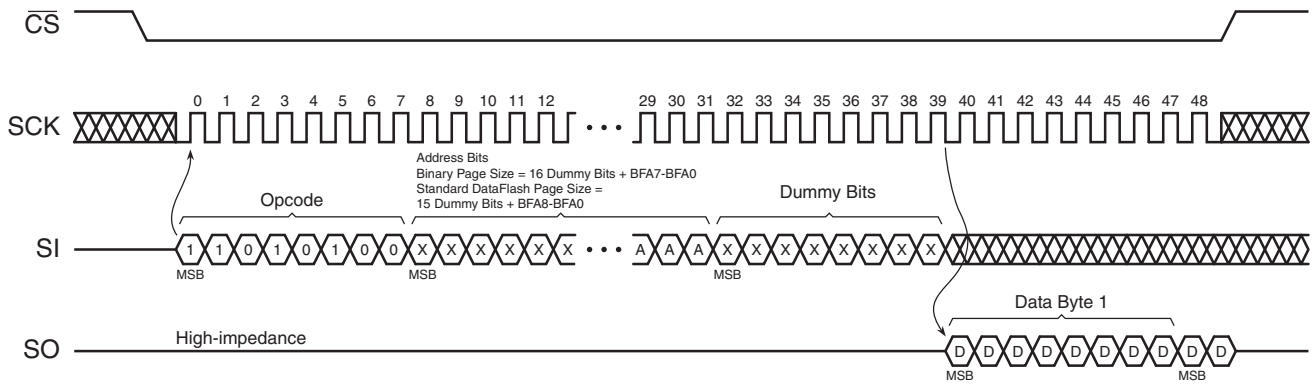


Figure 42. Buffer Read Timing (Opcode D4h or D6h)

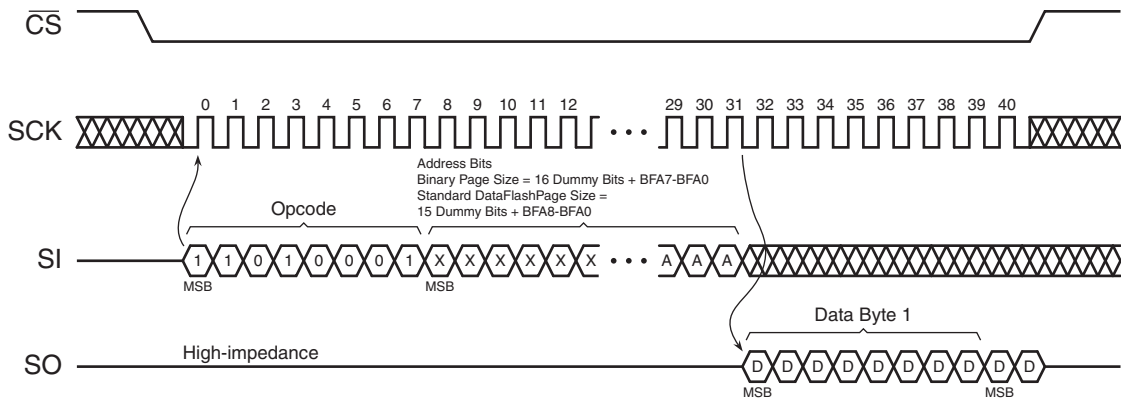


Figure 43. Buffer Read – Low Frequency Timing (Opcode D1h or D3h)

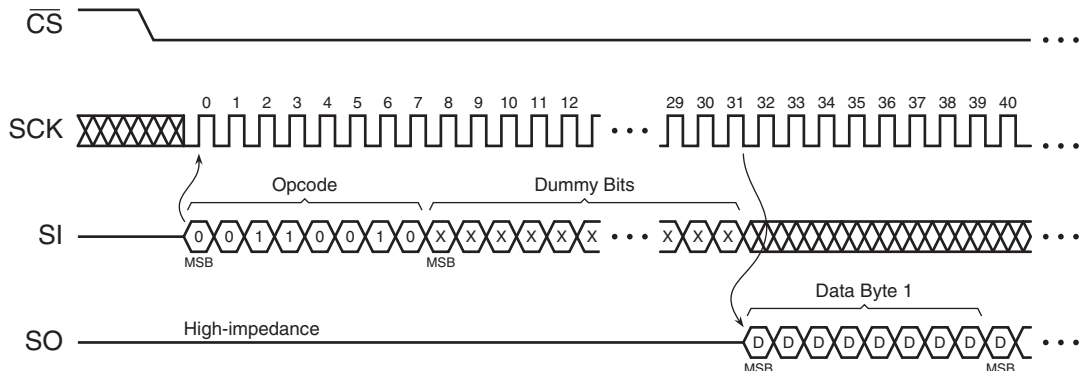


Figure 44. Read Sector Protection Register Timing (Opcode 32h)

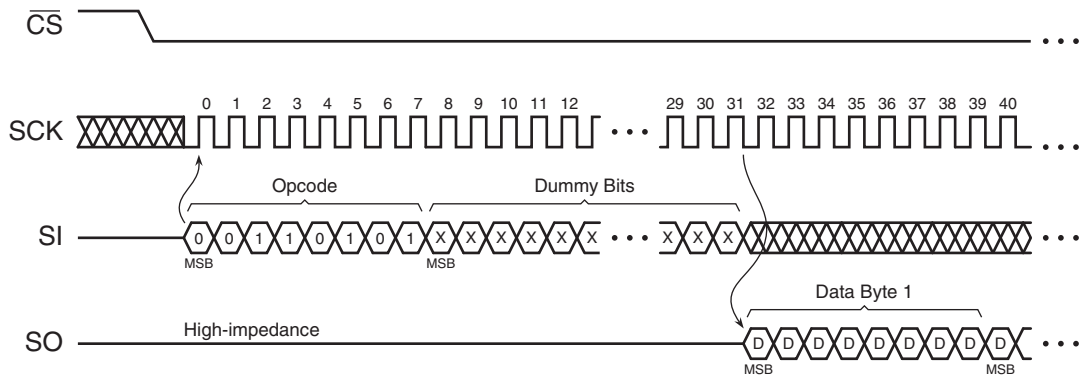


Figure 45. Read Sector Lockdown Register Timing (Opcode 35h)

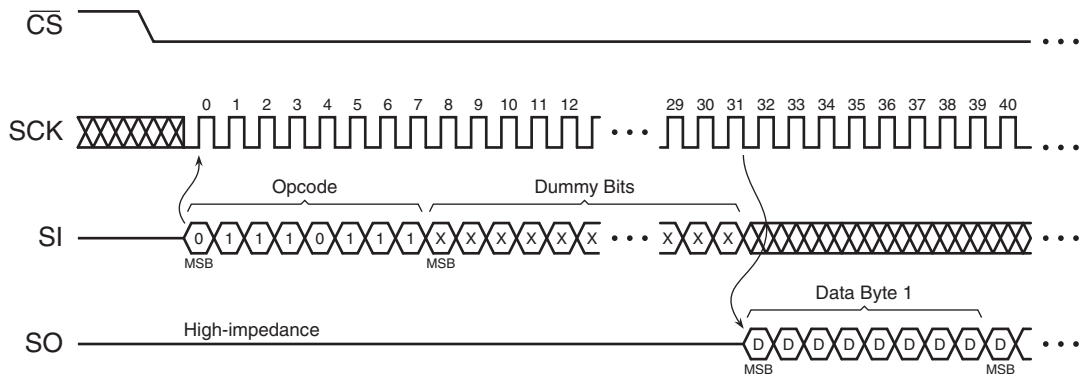


Figure 46. Read Security Register Timing (Opcode 77h)

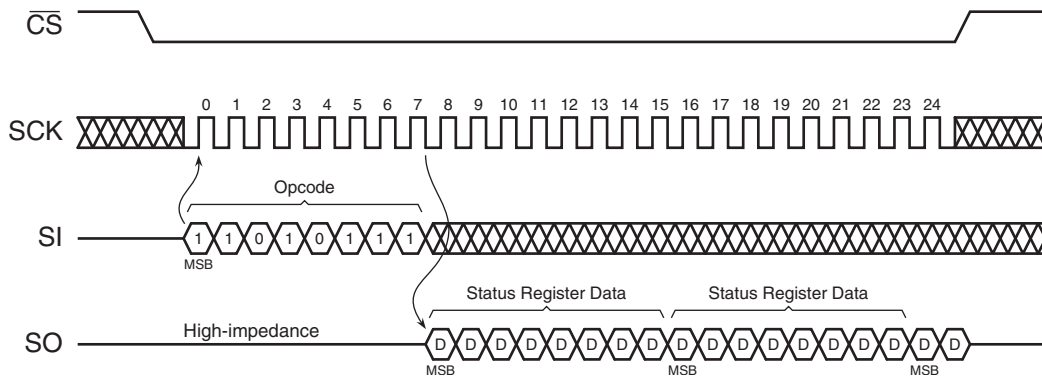
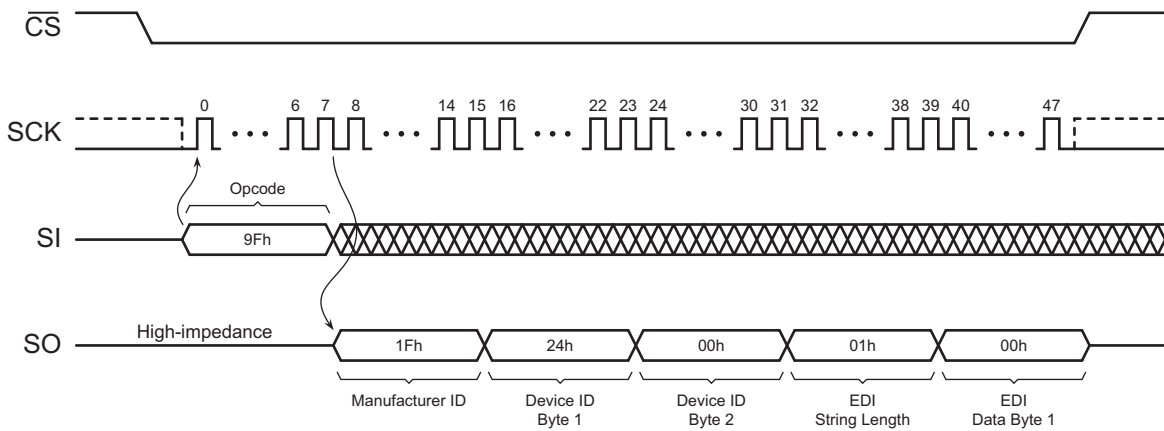


Figure 47. Status Register Read Timing (Opcode D7h)




Note: Each transition  shown for SI and SO represents one byte (8 bits)

Figure 48. Manufacturer and Device Read Timing (Opcode 9Fh)

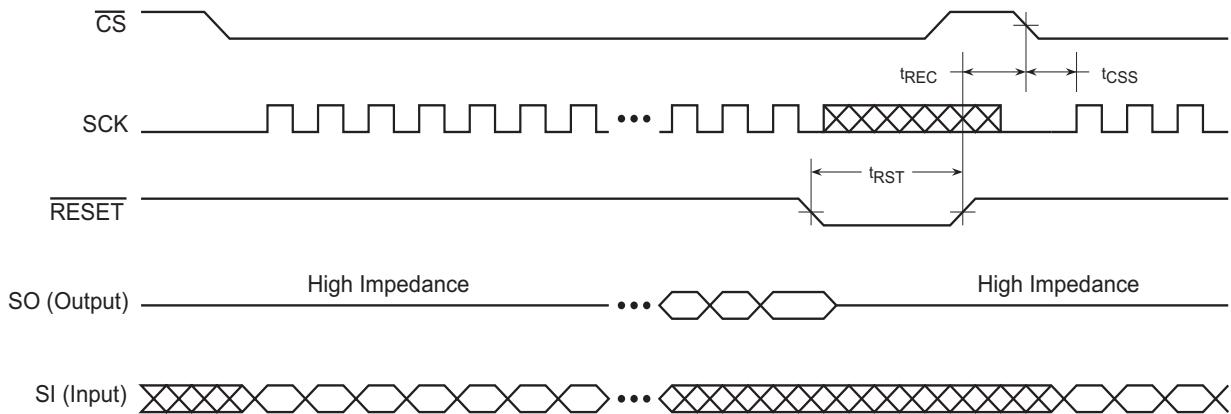
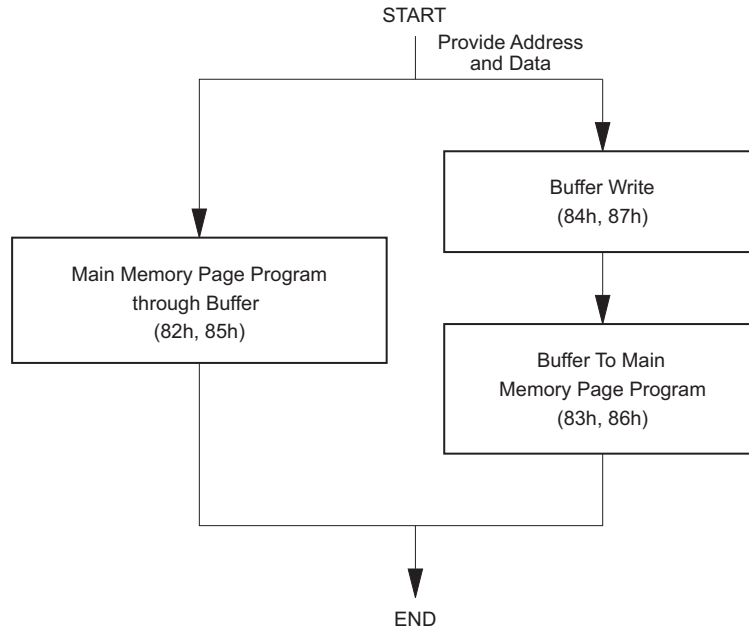


Figure 49. Reset Timing

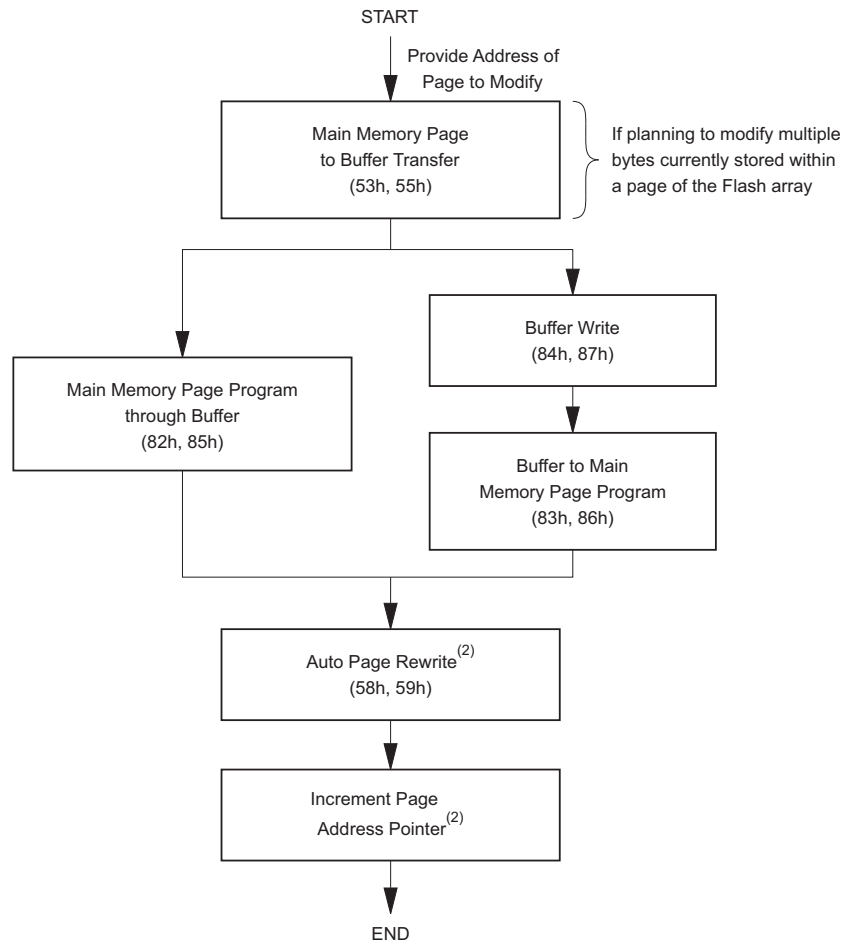
The  $\overline{CS}$  signal must be in the high state before the  $\overline{RESET}$  signal is deasserted.

## 27. Auto Page Rewrite Flowchart



**Figure 50. Algorithm for Programming or Re-programming of the Entire Array Sequentially**

1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a buffer write operation followed by a buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm is repeated sequentially for each page within the entire array.

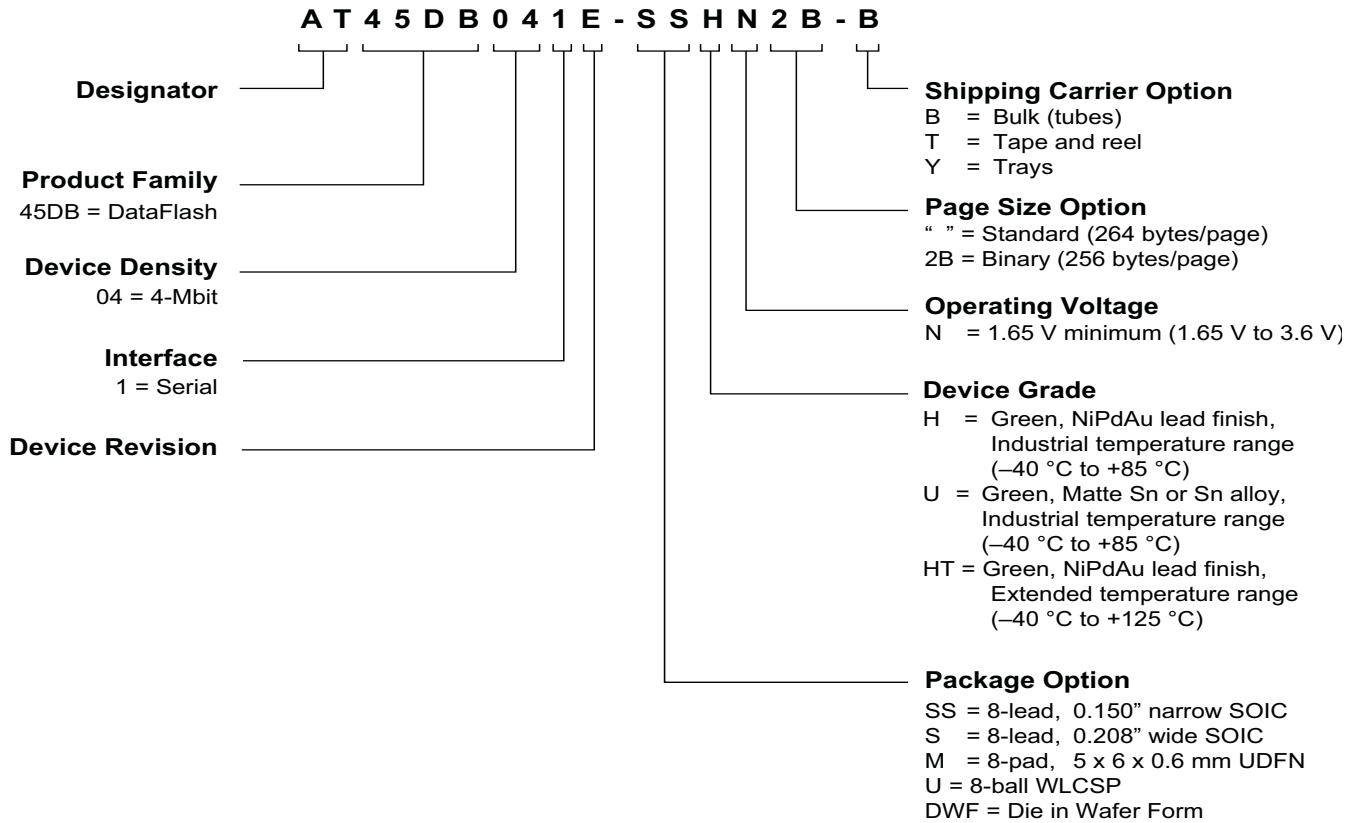


**Figure 51. Algorithm for Programming or Re-programming of the Entire Array Randomly**

1. To preserve data integrity, each page of an DataFlash sector must be updated/rewritten at least once within every 50,000 cumulative page erase and program operations.
2. A page address pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the page address pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications can choose to wait until 50,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector.

## 28. Ordering Information

### 28.1 Ordering Detail



### 28.2 Ordering Codes (Standard DataFlash Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f <sub>sck</sub>	Device Grade	
AT45DB041E-SSHNT-B <sup>1</sup>	8S1	NiPdAu	1.65 V to 3.6 V	85 MHz	Industrial (-40°C to 85°C)	
AT45DB041E-SSHNT-T <sup>1</sup>						
AT45DB041E-SHNT-B <sup>1</sup>	8S2					
AT45DB041E-SHNT-T <sup>1</sup>						
AT45DB041E-MHNT-Y <sup>1</sup>	8 MA1					
AT45DB041E-MHNT-T <sup>1</sup>						
AT45DB041E-SSHNHT-T <sup>1</sup>	8S1				Industrial (-40°C to 125°C)	
AT45DB041E-SSHNHT-B <sup>1</sup>						
AT45DB041E-SHNHT-T <sup>1</sup>	8S2					
AT45DB041E-SHNHT-B <sup>1</sup>						
AT45DB041E-UUN-T <sup>1,3</sup>	CS4-8A					
AT45DB041E-DWF <sup>2</sup>	DWF					

- The shipping carrier suffix is not marked on the device.
- Contact Renesas Electronics for mechanical drawing or Die Sales information.
- Contact Renesas Electronics for manufacturing flow and availability.

## 28.3 Ordering Codes (Binary Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f <sub>SCK</sub>	Device Grade
AT45DB041E-SSHN2B-T <sup>1,2</sup>	8S1	NiPdAu	1.65 V to 3.6 V	85 MHz	Industrial (-40°C to 85°C)
AT45DB041E-SHN2B-T <sup>1,2</sup>	8S2				
AT45DB041E-MHN2B-T <sup>1,2</sup>	8 MA1				
AT45DB041E-UUN2B-T <sup>1,2,3</sup>	CS4-8A				

- The shipping carrier suffix is not marked on the device.
- Parts ordered with suffix code '2B' are shipped in tape and reel (T&R) with the page size set to 256 bytes. This option is only available for shipping in T&R (-T).
- Contact Renesas Electronics for manufacturing flow and availability.

Package Type	
8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8 MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)
CS4-8A	8-ball Wafer Level Chip Scale Package
DWF	Die in Wafer Form

## 28.4 Ordering Codes (Reserved)

Ordering Code	Package	Lead Finish	Operating Voltage	f <sub>SCK</sub>	Device Grade
AT45DB041E-SSHNHA-T <sup>1,2</sup>	8S1	NiPdAu	1.65 V to 3.6 V	85MHz	Industrial (-40°C to 85°C)
AT45DB041E-SHNHA-T <sup>1,2</sup>	8S2				
AT45DB041E-SSHNHC-T <sup>1,3</sup>	8S1				
AT45DB041E-SHNHC-T <sup>1,3</sup>	8S2				

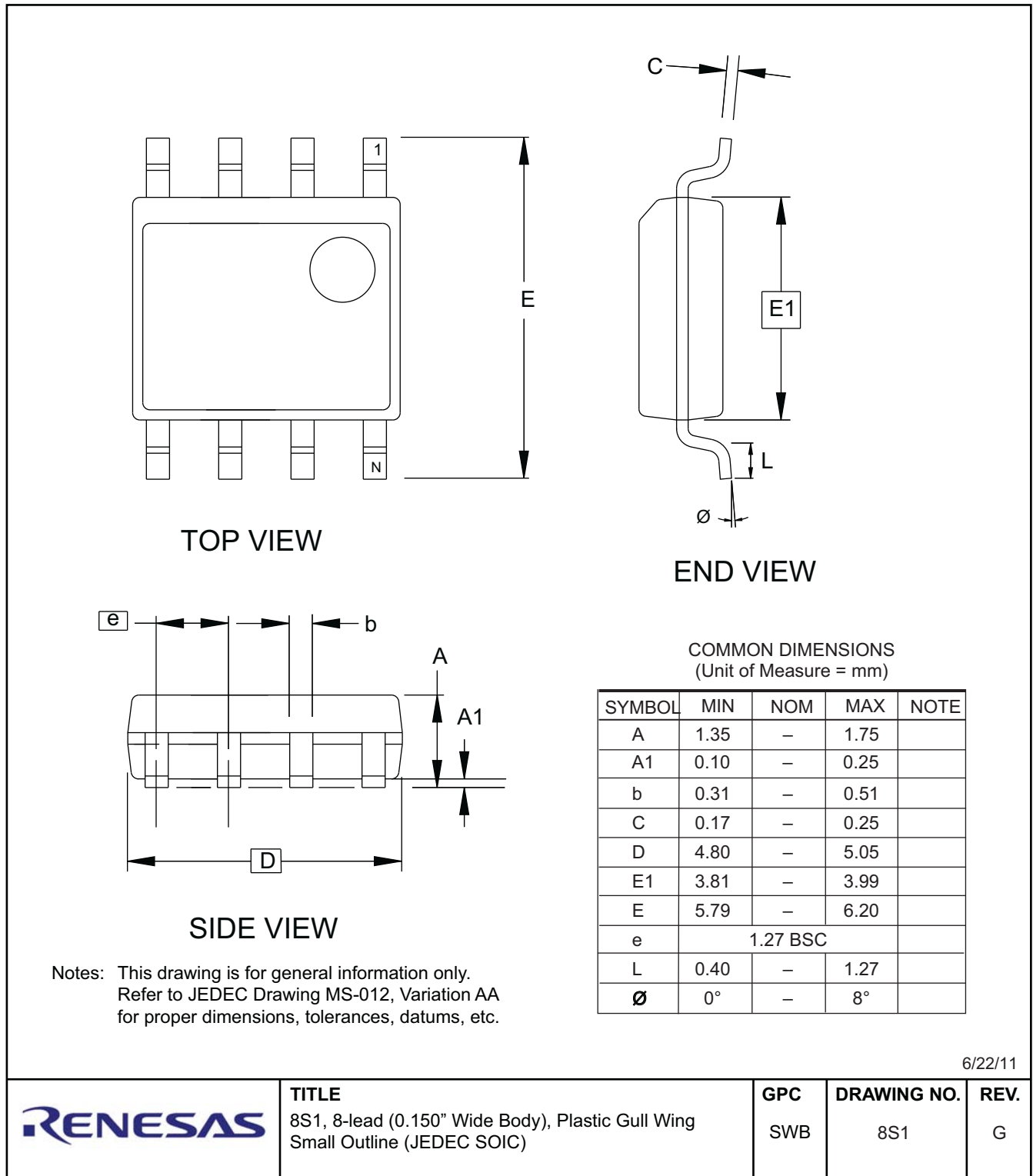
- Notes:
- The shipping carrier suffix is not marked on the device.
  - Parts ordered with suffix code 'HA' are shipped in tape and reel (T&R) only, with the page size set to 264 bytes.
  - Parts ordered with suffix code 'HC' are shipped in tape and reel (T&R) only, with the page size set to 256 bytes.

Contact Renesas Electronics for a description of these 'Reserved' codes.

8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)

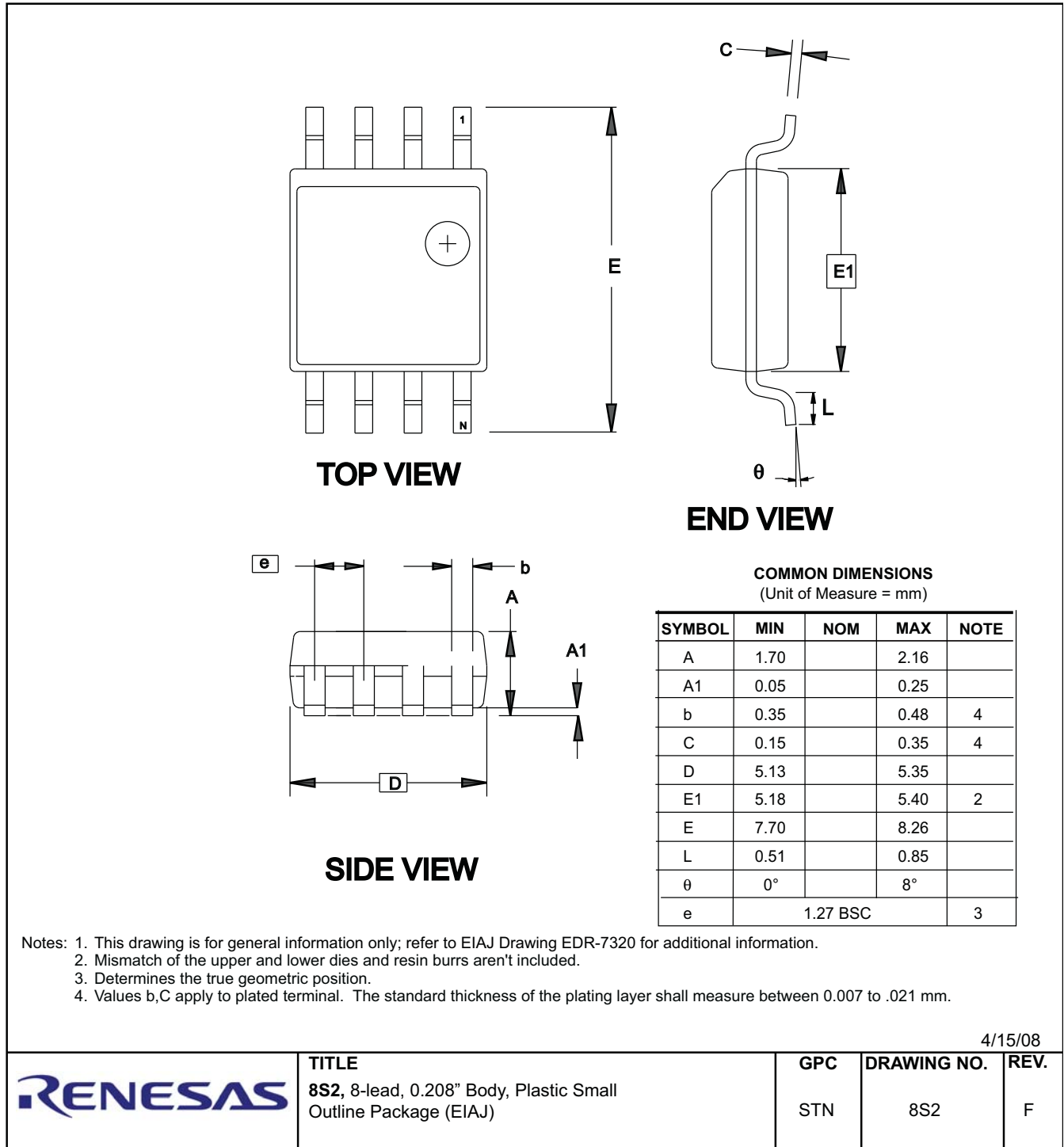
## 29. Packaging Information

### 29.1 8S1 – 8-lead JEDEC SOIC

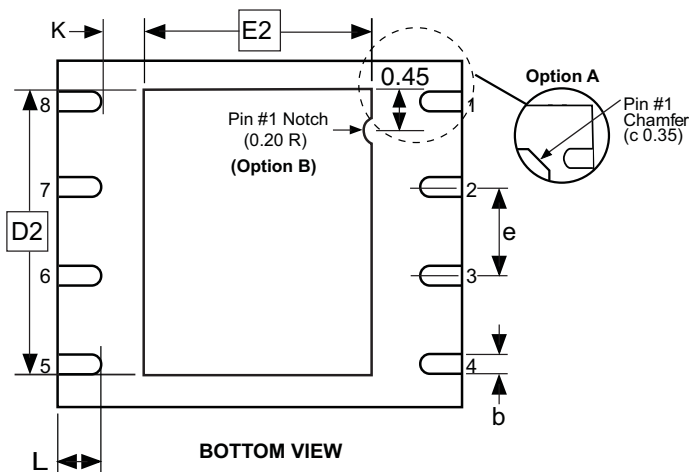
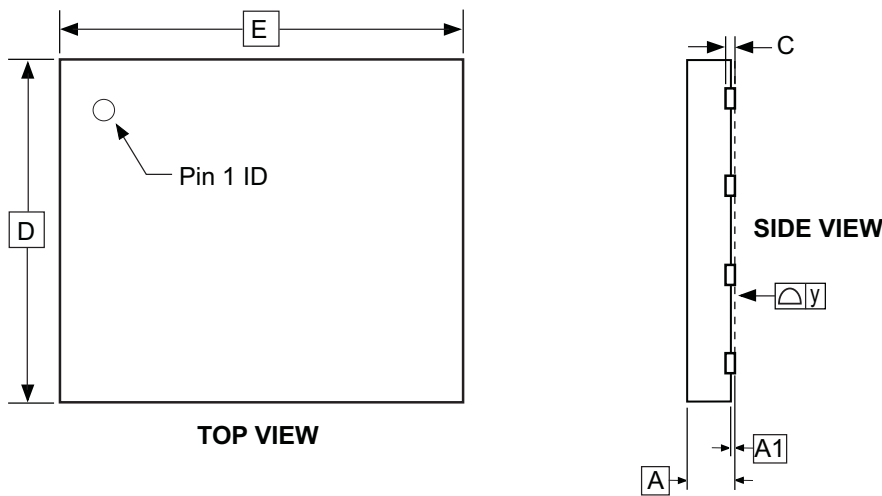




29.2 8S2 – 8-lead EIAJ SOIC



### 29.3 8 MA1 – 8-pad UDFN



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C	0.152 REF			
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e	1.27			
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.  
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	<b>TITLE</b> <b>8MA1</b> , 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	<b>GPC</b> YFG	<b>DRAWING NO.</b> 8MA1	<b>REV.</b> D



## 30. Revision History

Doc. Rev.	Date	Comments
8783A	09/2012	Initial document release.
8783B	11/2012	Added Legacy Commands table. Updated to Adesto template.
8783C	6/2013	Updated power and electrical specifications. Removed CCUN-T package (not available with this device) and other UBGA references. "Buffer 1 (or 2) Read" moved from Group C to Group A in Operation Mode Summary.
8783D	7/2013	Updated electrical specification for $f_{CAR1}$ for 1.65 V to 3.6 V to 70 MHz - (SCK Frequency for Continuous Read (0x0B)). Removed Preliminary Status.
8783E	7/2013	Updated Auto Page Rewrite cycle to 50,000 cumulative page erase/program operations. Added reserved part order codes. Updated DC conditions for $V_{OL}$ , $I_{CC3}$ and $I_{CC4}$ .
8783F	10/2013	Updated spec in Continuous Array Read (1Bh Opcode) to $f_{CAR4}$ . Corrected Low Power Read Option (up to 15 MHz). Corrected Ultra-Deep Power-Down current (400nA typical). Updated spec for Input High Voltage (Max) to $V_{CC} + 0.6$ V.
8783G	1/2014	Removed mention of 9-ball Ultra-thin UBGA (6 x 6 x 0.6 mm). Not available in this package.
8783H	7/2015	Expanded explanation of Power up/Power down (Section 16). Added Die in Wafer Form package option. Updated Table 6-4 (Main Memory to Buffer Compare). Corrected references in Section 9.3 (Auto Page Rewrite). Corrected Table 15-7. Added information on Power Up (Section 16.1). Updated Tables 12-1 and 12-3. Updated condition description for $I_{UDPD}$ , $I_{DPD}$ , and $I_{SB}$ . Updated Deep Power Down and Ultra Deep Power Down timing diagrams.
8783I	3/2016	Added WLCSP package option. Updated Condition description for $I_{DPD}$ , $I_{SB}$ , $I_{CC1}$ and $I_{CC2}$ . Added footnote to $I_{CC1}$ , $t_{DIS}$ , $t_{EUDPD}$ , $t_{EPD}$ . Updated footnote 2 on Table 18.3. Removed footnotes from Table 18.5.
8783J	1/2017	Updated $t_{XUDPD}$ . Added patent information.
8783K	2/2017	Added Errata section.
8783L	7/2017	Added clarification of Absolute Maximum Ratings. Corrected Active Read and Standby specs on Features page. Added footnote and updated WLCSP references.
8783M	7/2020	Updated format and layout. Copy edited throughout (no change to technical content). For packages ending in SHN-B and SHN-T, removed link to note in the Ordering Codes tables that states: "Not recommended for new designs. Use the 8S1 package option."
8783N	3/2021	Updated notes 2 and 3 for Table 28.2. Updated original note 4, and removed original note 2 from Table 28.3. Updated contact info under Table 28.4.
8783O	2/2022	Changed Adesto logo to Renesas.
8783P	9/2022	Applied new corporate template to document. Added the following sentence to the end of the CS description in Table 1: "To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from CS to $V_{CC}$ . This ensures CS ramps together with $V_{CC}$ during power-up." Integrated the AT45DB041E-024D-HT Addendum content.

## 31. Errata

The specification for Exit Ultra Deep Power Down has been updated. The new specification for the 1.65 V - 3.6 V range is 280  $\mu$ s. The new specification for the 2.3 V - 3.6 V range is 140  $\mu$ s.

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