

PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free

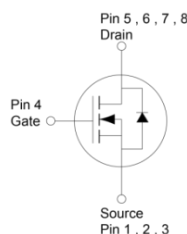
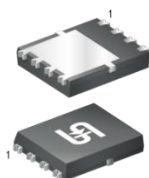
APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converters

PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
V_{DS}	40	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	1.9	mΩ
	$V_{GS} = 4.5V$	2.7	
Q_g	$V_{GS} = 4.5V$	49	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	40	V	
Gate-Source Voltage	V_{GS}	± 16	V	
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	214	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	100	A
	$T_C = 100^\circ\text{C}$		100	
	$T_A = 25^\circ\text{C}$		30	
Pulsed Drain Current (Note 2)		I_{DM}	400	A
Single Pulse Avalanche Current (Note 3)		I_{AS}	42.8	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	274.5	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	150	W
	$T_C = 125^\circ\text{C}$		50	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient (Note 4)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

NOTE:

1. Package current limit.
2. Pulse Width $\leq 100\mu\text{s}$.
3. $L = 0.3\text{mH}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
4. Device on a PCB FR4 with 1 in² (single layer, 2 oz thick) copper area for drain connection.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.4	1.8	2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 5)	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	$R_{DS(on)}$	--	1.3	1.9	m Ω
	$V_{GS} = 4.5\text{V}, I_D = 50\text{A}$		--	1.6	2.7	
Forward Transconductance (Note 5)	$V_{DS} = 10\text{V}, I_D = 12.5\text{A}$	g_{fs}	--	106	--	S
Dynamic (Note 6)						
Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DS} = 25\text{V},$ $I_D = 30\text{A}$	Q_g	--	49	74	nC
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 25\text{V},$ $I_D = 30\text{A}$	Q_g	--	104	156	
Gate-Source Charge		Q_{gs}	--	19	38	
Gate-Drain Charge		Q_{gd}	--	15	30	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	6282	9423	pF
Output Capacitance		C_{oss}	--	1204	2408	
Reverse Transfer Capacitance		C_{rss}	--	63	126	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	1.0	--	Ω
Switching (Note 7)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 25\text{V},$ $I_D = 30\text{A}, R_G = 3.3\Omega$	$t_{d(on)}$	--	16	--	ns
Rise Time		t_r	--	77	--	
Turn-Off Delay Time		$t_{d(off)}$	--	74	--	
Fall Time		t_f	--	104	--	
Source-Drain Diode						
Diode Forward Voltage (Note 5)	$V_{GS} = 0\text{V}, I_S = 50\text{A}$	V_{SD}	--	--	1.1	V
Reverse Recovery Time	$I_S = 30\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	61	--	ns
Reverse Recovery Charge		Q_{rr}	--	97	--	nC

Notes:

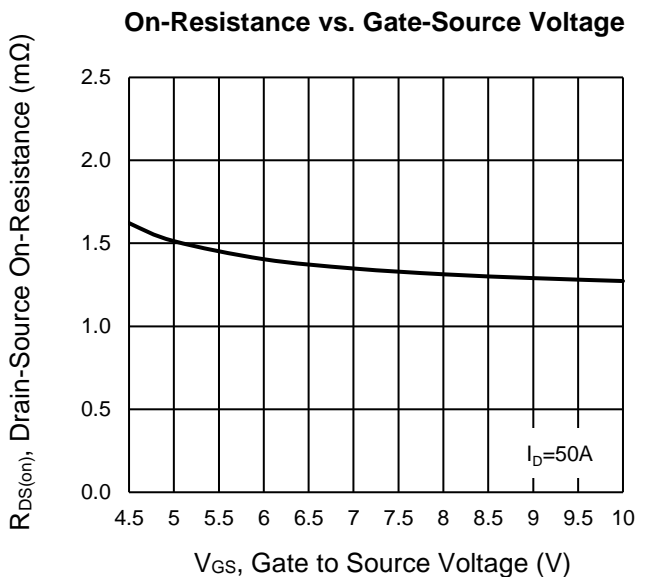
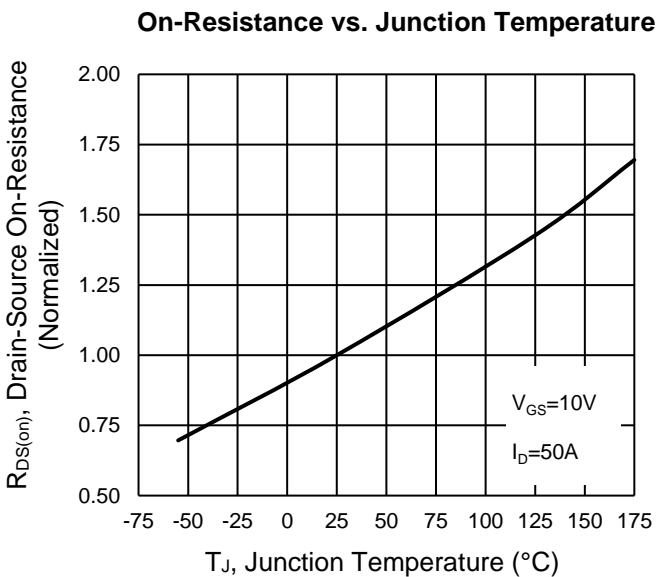
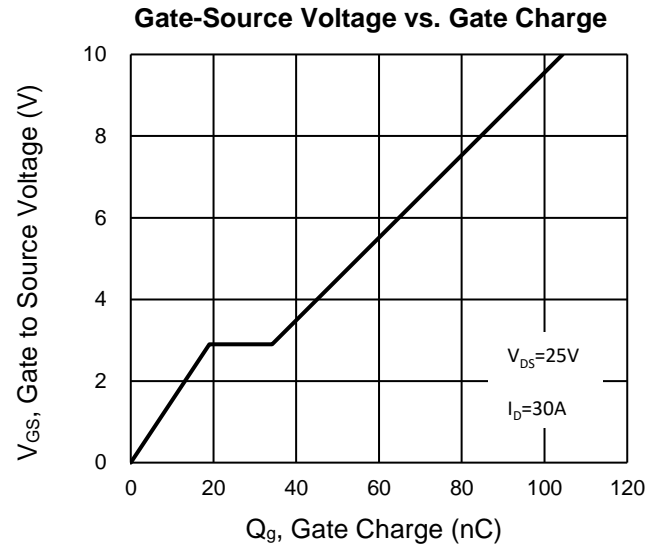
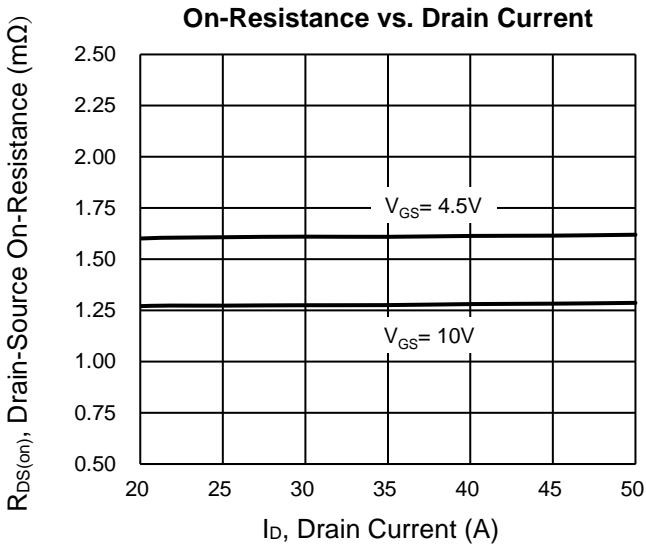
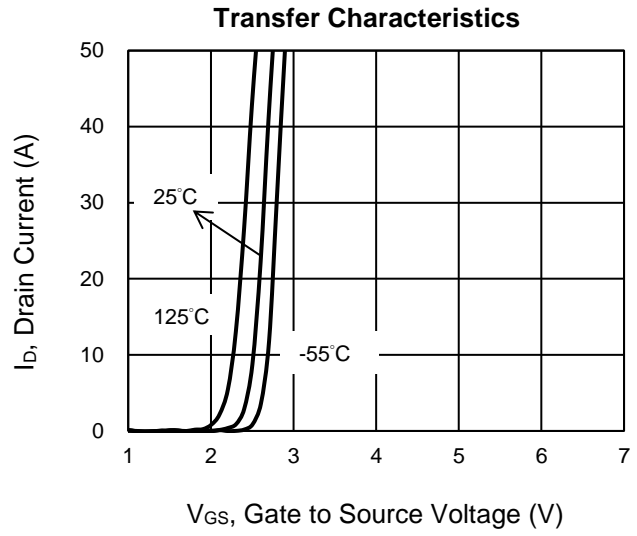
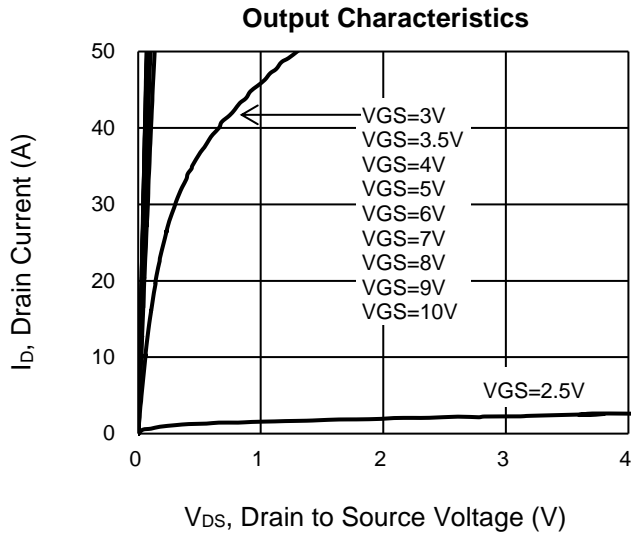
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM019NH04LCR RLG	PDFN56U	2,500pcs / 13" Reel

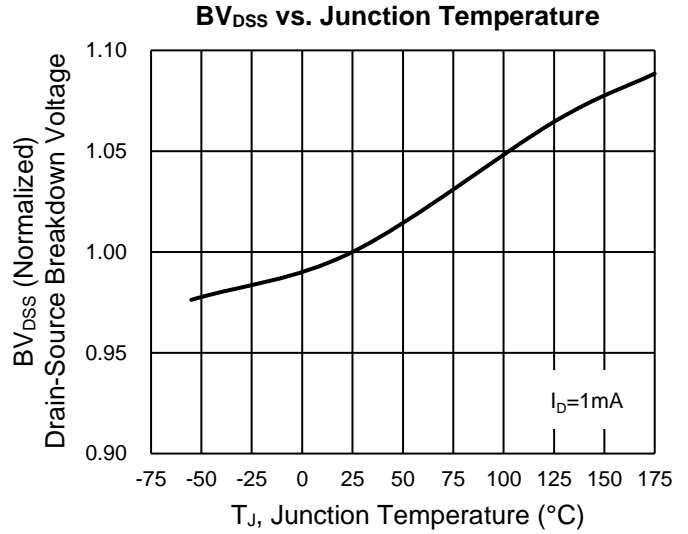
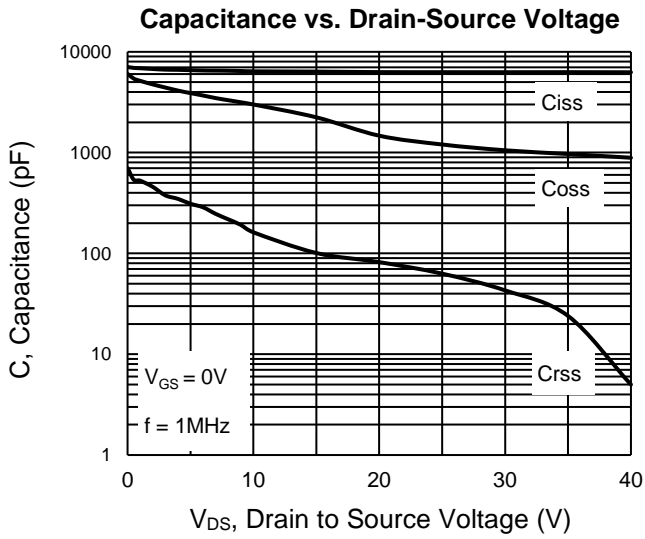
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

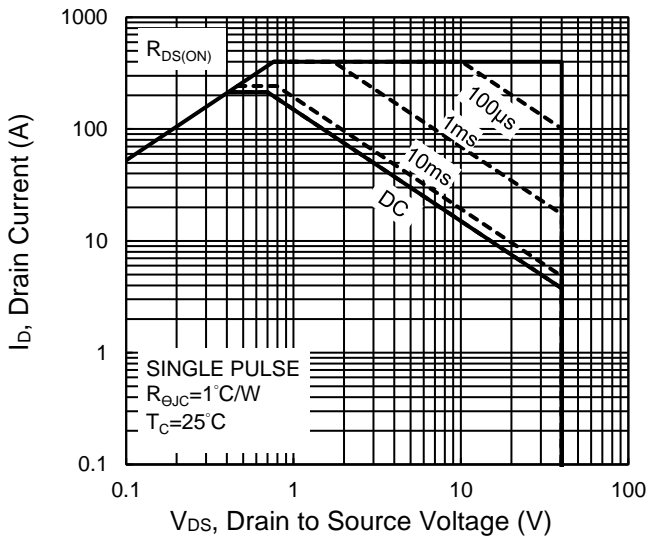


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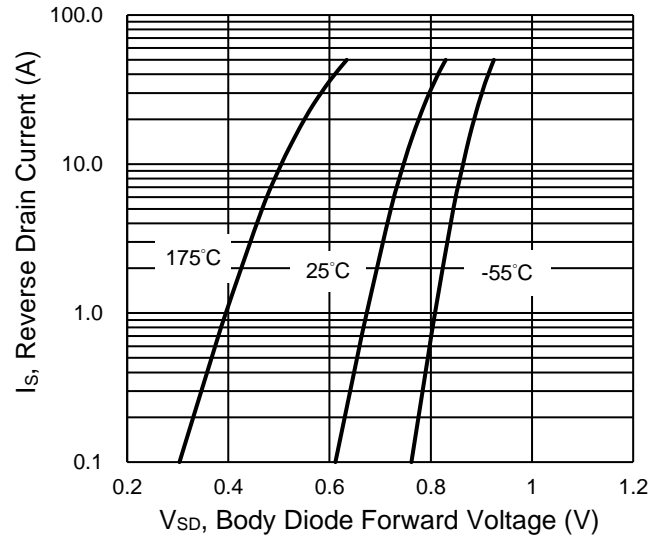
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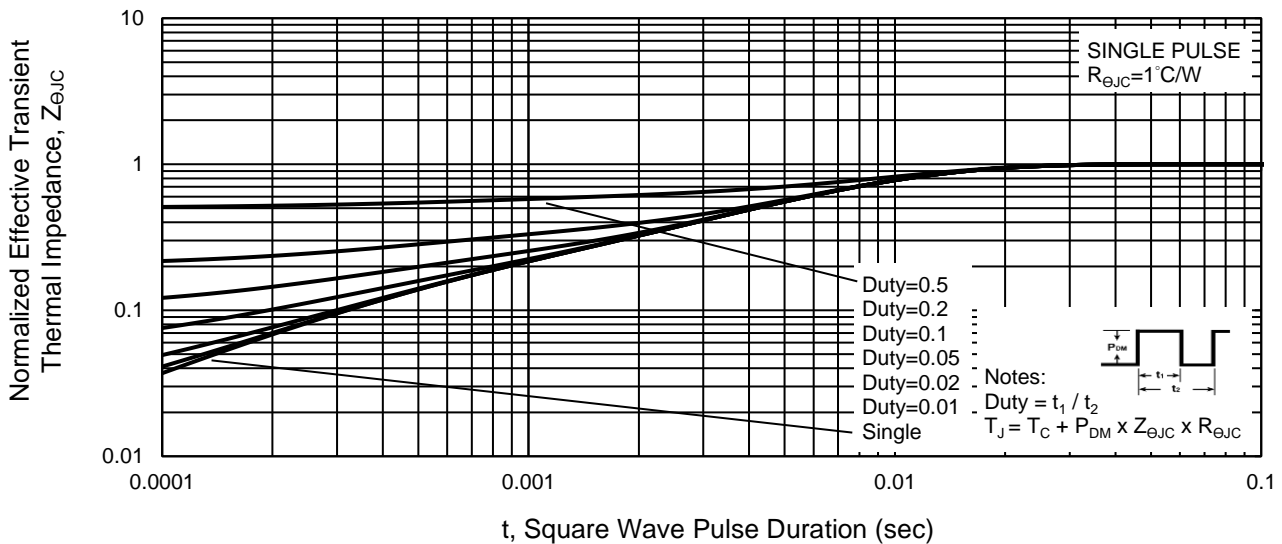
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



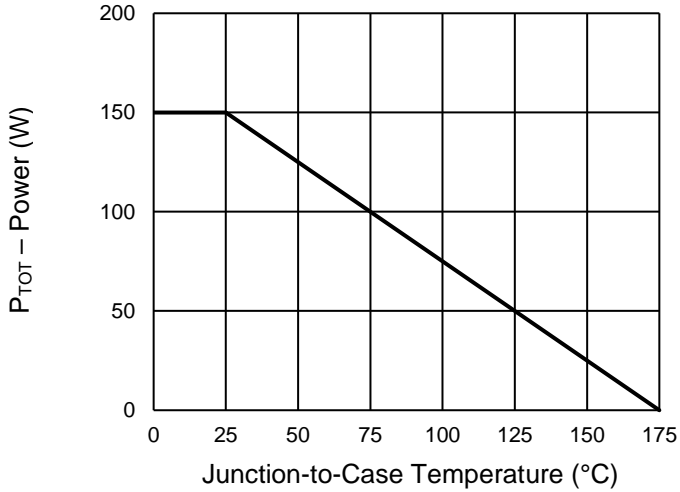
Normalized Thermal Transient Impedance, Junction-to-Case



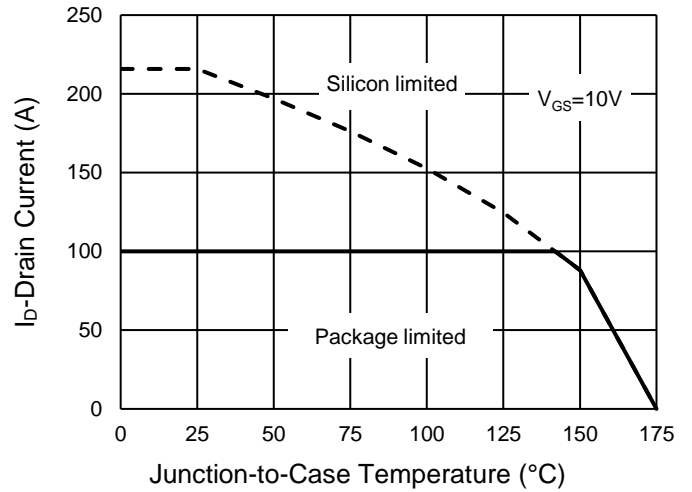
CHARACTERISTICS CURVES

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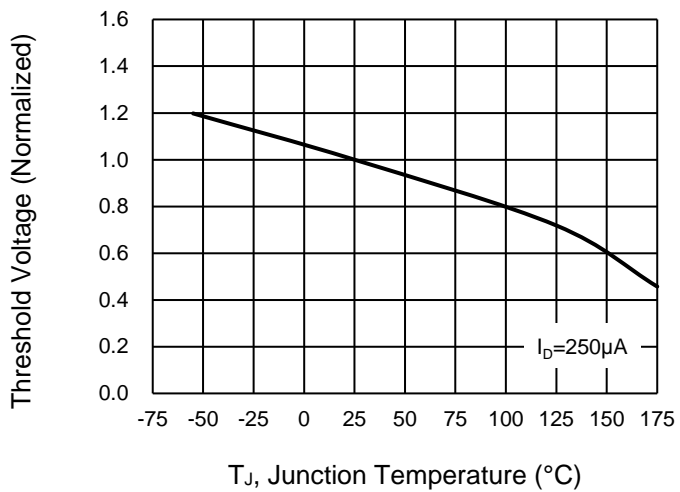
Power Dissipation



Drain Current

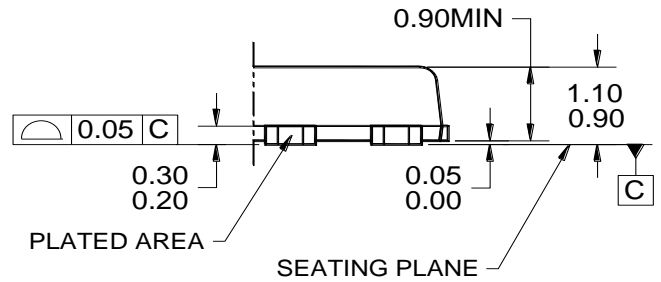
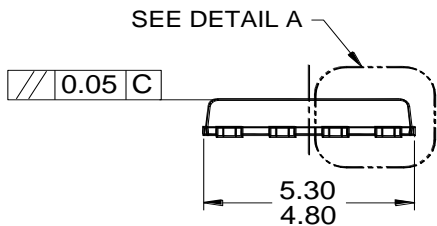
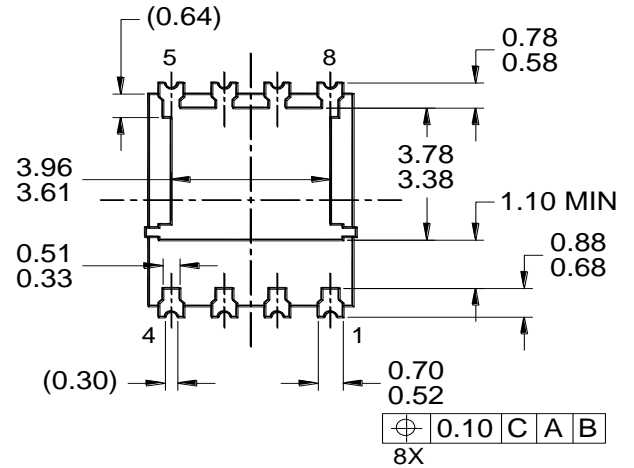
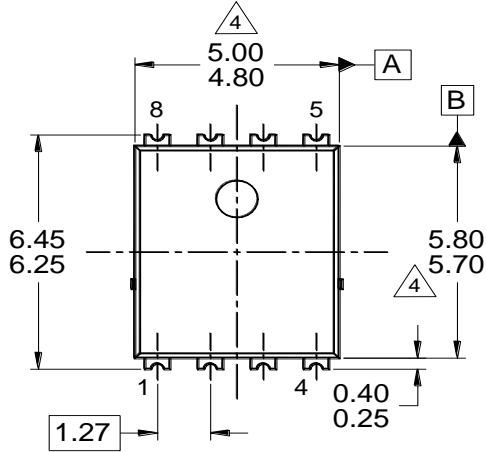


Normalized gate threshold voltage vs Temperature

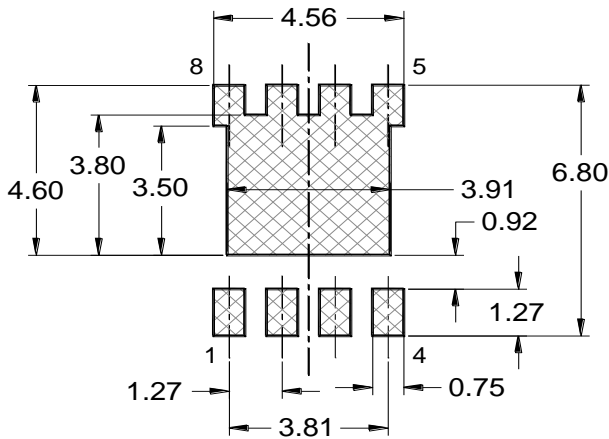


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

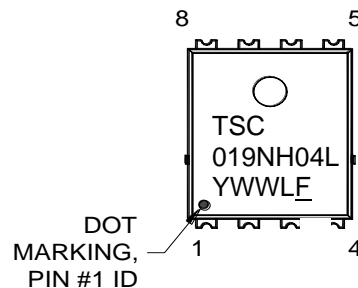
PDFN56U



DETAIL A
(SCALE 2:1)



SUGGESTED PAD LAYOUT
(REFERENCE ONLY)



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

- Y = YEAR CODE
- WW = WEEK CODE (01~52)
- L = LOT CODE (1~9, A~Z)
- F = FACTORY CODE
- = AEC-Q101 QUALIFIED

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