

Small Signal Dual P-Channel MOSFET

FEATURES

- AEC-Q101 Qualified
- Advanced trench cell design
- ESD protected G-S 2kV (HBM)
- RoHS Compliant
- Halogen-free

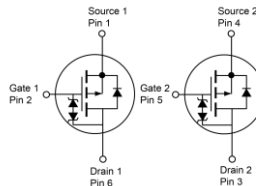
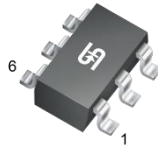
APPLICATIONS

- Switching circuits
- High-speed line driver
- High-side loadswitch
- Relay driver

PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
V_{DS}	-60	V	
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	6	Ω
	$V_{GS} = -4.5V$	7	
Q_g	$V_{GS} = -4.5V$	1	nC



SOT-363



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-170	mA
Pulsed Drain Current (Note 1)	I_{DM}	-0.68	A
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	320
		$T_A = 125^\circ\text{C}$	64
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance (Note 2)	$R_{\theta JA}$	390	$^\circ\text{C/W}$

Notes:

1. Pulse Width $\leq 100\mu\text{s}$.
2. Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-0.8	-1.5	-2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Zero Gate Voltage Drain Current	$V_{DS} = -60V, V_{GS} = 0V$	I_{DSS}	--	--	-1	μA
	$V_{DS} = -60V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$		--	--	-100	
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -170mA$	$R_{DS(on)}$	--	1.9	6	Ω
	$V_{GS} = -4.5V, I_D = -160mA$		--	2.4	7	
Forward Transconductance	$V_{DS} = -10V, I_D = -170mA$	g_{fs}	--	434	--	mS
Dynamic (Note 4)						
Total Gate Charge	$V_{DS} = -30V, I_D = -170mA,$ $V_{GS} = -10V$	Q_g	--	1.9	--	nC
Total Gate Charge	$V_{DS} = -30V, I_D = -160mA,$ $V_{GS} = -4.5V$	Q_g	--	1	--	nC
Gate-Source Charge		Q_{gs}	--	0.3	--	
Gate-Drain Charge		Q_{gd}	--	0.3	--	
Input Capacitance	$V_{DS} = -30V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	38.2	--	pF
Output Capacitance		C_{oss}	--	8	--	
Reverse Transfer Capacitance		C_{rss}	--	4.2	--	
Switching (Note 5)						
Turn-On Delay Time	$V_{DD} = -30V, R_G = 6.0\Omega,$ $I_D = -170mA, V_{GS} = -10V$	$t_{d(on)}$	--	5.5	--	ns
Turn-On Rise Time		t_r	--	2.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	39.2	--	
Turn-Off Fall Time		t_f	--	19.6	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$I_S = -170mA, V_{GS} = 0V$	V_{SD}	--	-0.9	-1.3	V

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

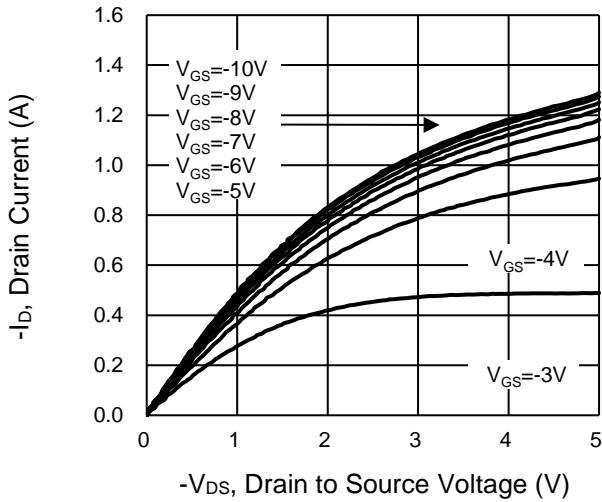
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM84KDCU6 RFG	SOT-363	3,000pcs / 7" Reel

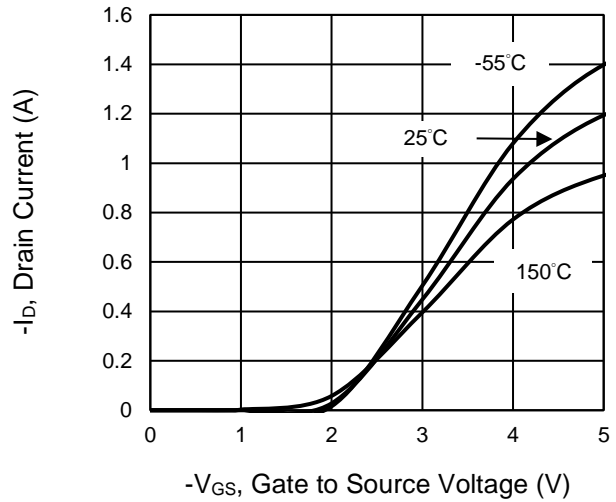
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

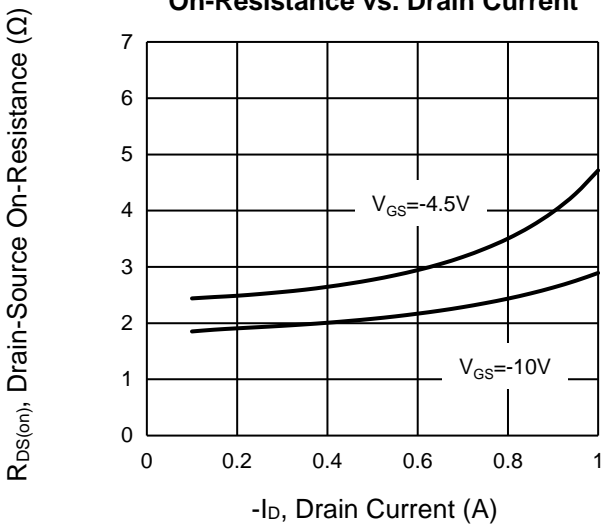
Output Characteristic



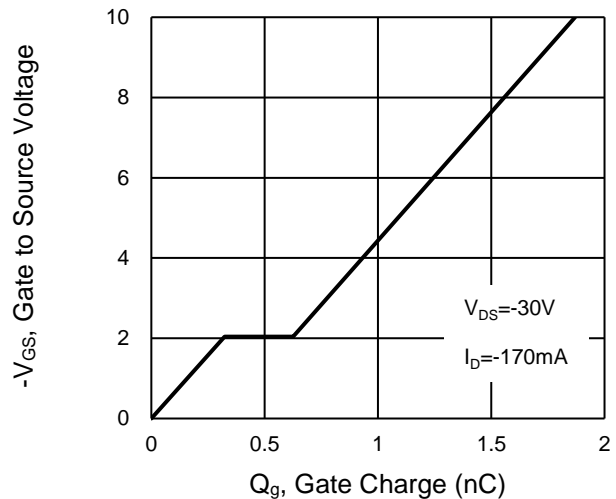
Transfer Characteristics



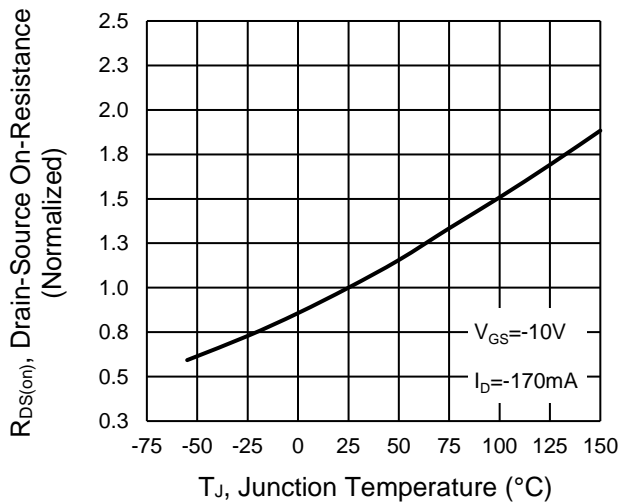
On-Resistance vs. Drain Current



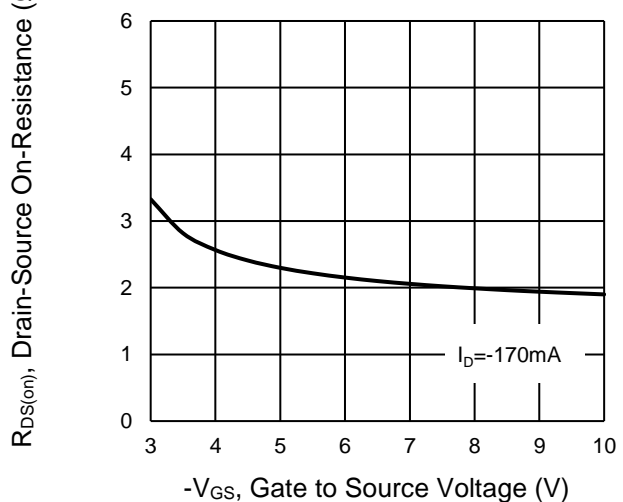
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



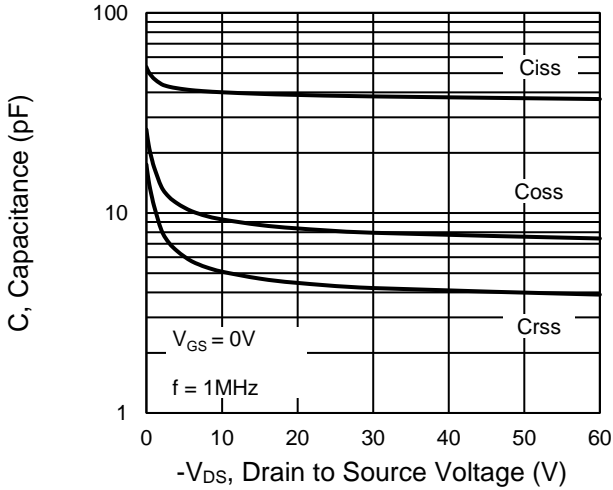
On-Resistance vs. Gate-Source Voltage



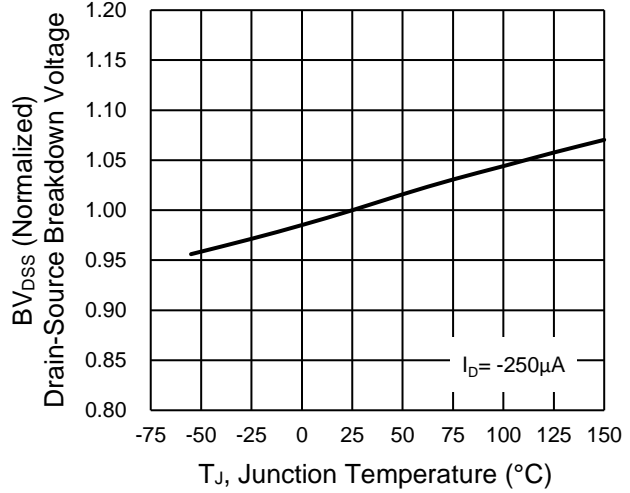
CHARACTERISTICS CURVES

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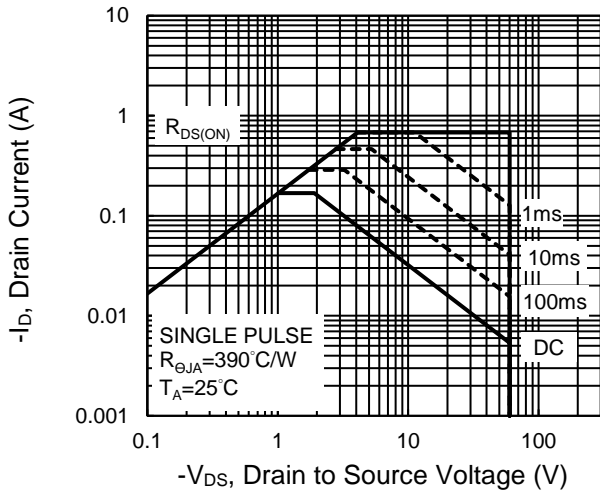
Capacitance vs. Drain-Source Voltage



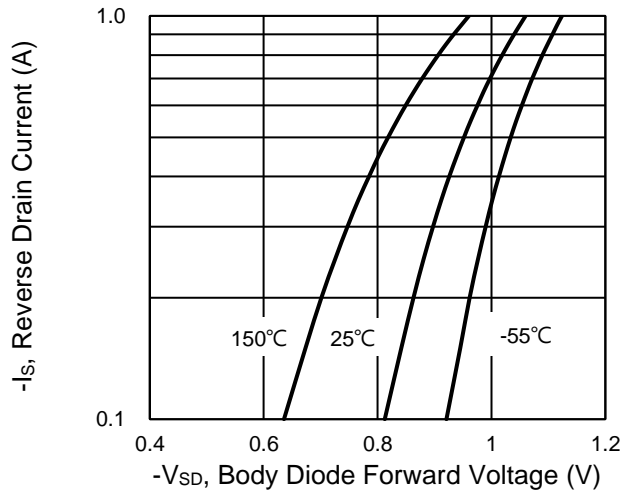
BV_{DSS} vs. Junction Temperature



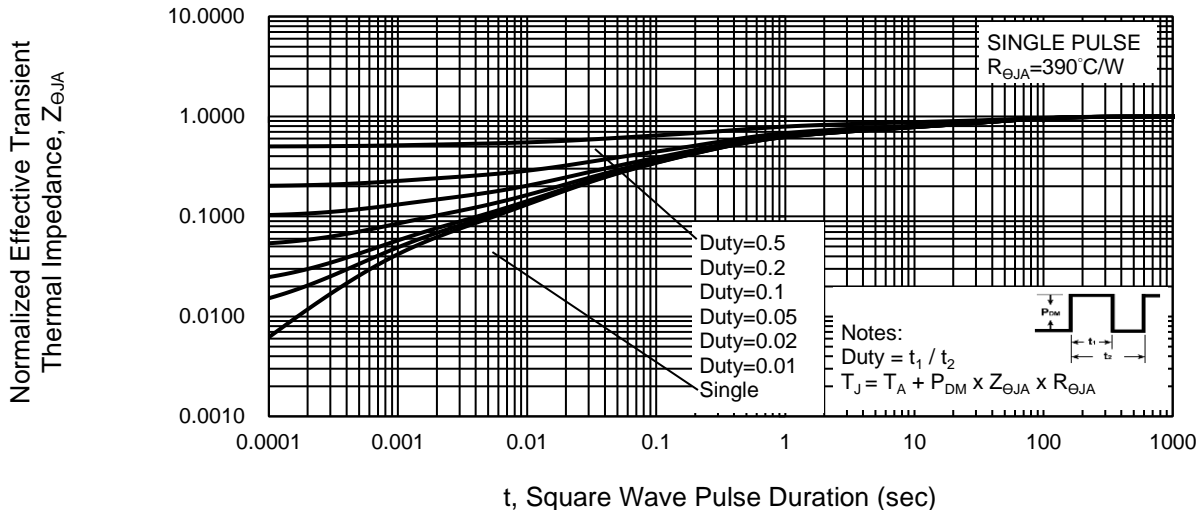
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage



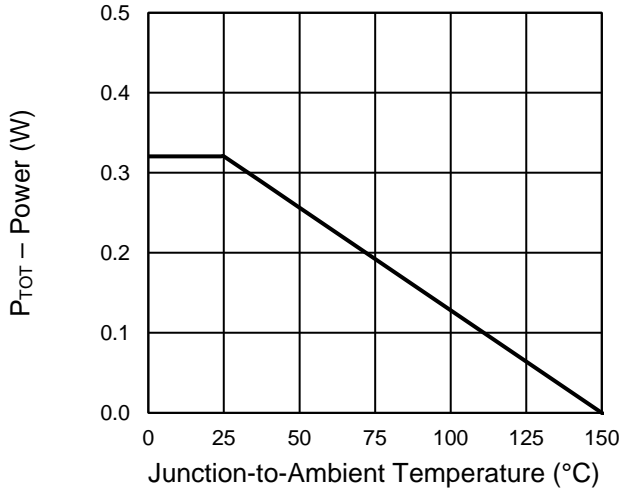
Normalized Thermal Transient Impedance, Junction-to-Ambient



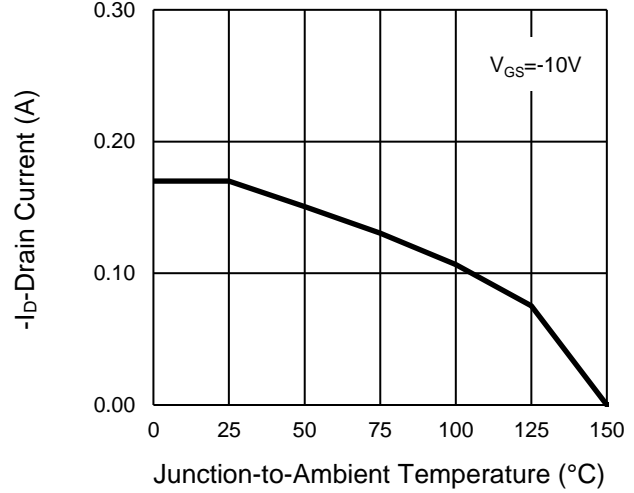
CHARACTERISTICS CURVES

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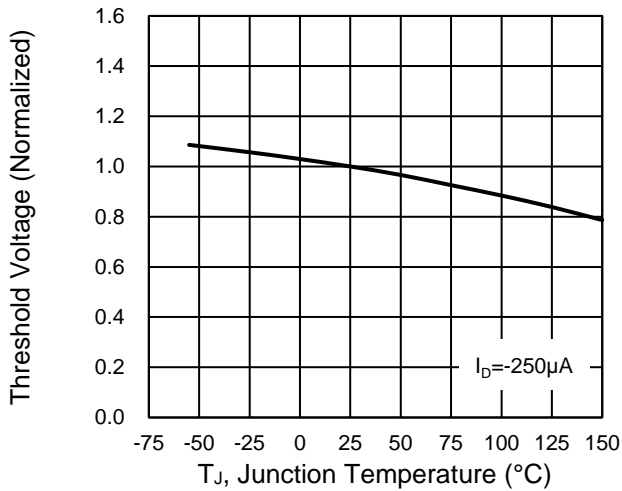
Power Dissipation



Drain Current

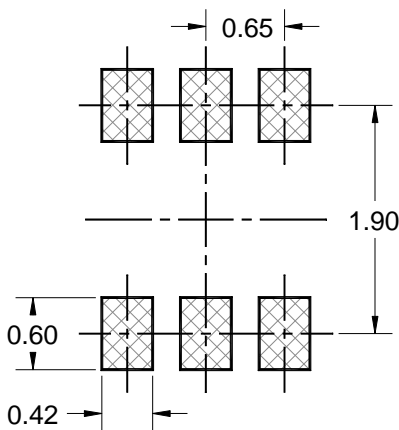
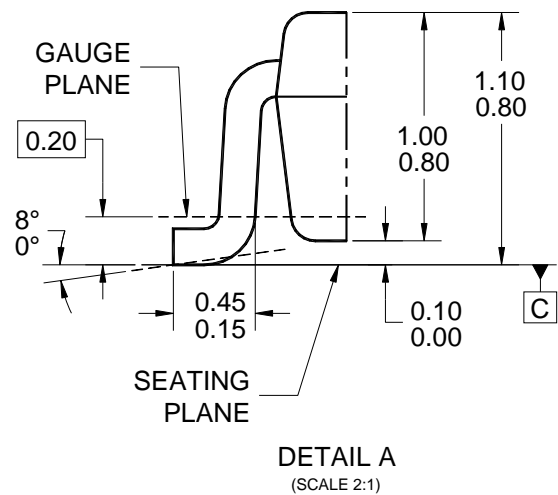
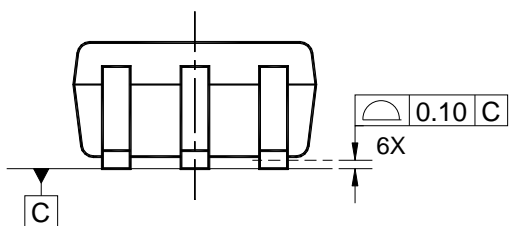
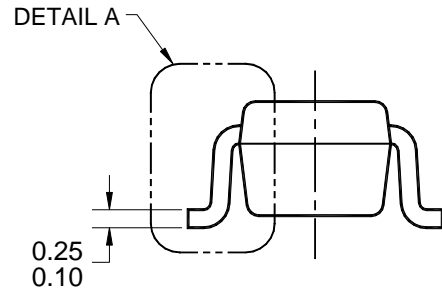
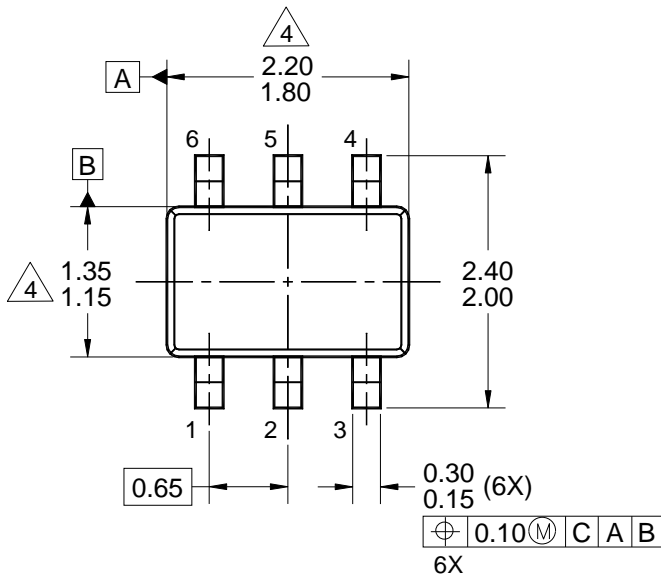


Normalized gate threshold voltage vs Temperature



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

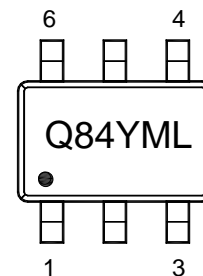
SOT-363



SUGGESTED PAD LAYOUT

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500A, EIAJ SC-88.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-SOT363-097 REV A.



MARKING DIAGRAM

- Y = Year Code
- M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code (1-9,A-Z)

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