FEATURES

- 650 V enhancement mode power transistor
- 850 V transient drain-to-source voltage
- Bottom-cooled 8x8 mm PDFN package
- $R_{DS(on)(Typ)}$ = 150 mΩ
- $D_{S(max)}$ = 11 A / $I_{DS(Max\ pulse)}$ = 19A
- Ultra-low FOM
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- High switching frequency (> 1 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Source Sense (SS) pin for optimized gate drive
- ROHS Compliant
- Halogen-free

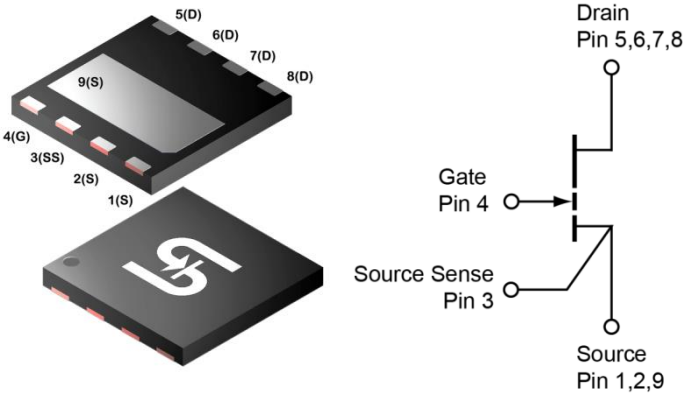
KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		650	V
$R_{DS(on)}$ (max)	V_{GS} = 6V	195	mΩ
Q_g		2.2	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Power Adapters
- LED Lighting Drivers
- Fast Battery Charging
- Power Factor Correction
- Appliance Motor Drives
- Wireless Power Transfer
- Industrial Power Supplies

PDFN88



ABSOLUTE MAXIMUM RATINGS (Tcase = 25 °C except as noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	650	V
Drain-to-Source Voltage – transient (Note 1)		$V_{DS(transient)}$	850	V
Gate-Source Voltage		V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)		$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current	T_C = 25°C	I_{DS}	11	A
	T_C = 100°C		7.2	
Pulse Drain Current (Pulse width 10 μs, V_{GS} = 6 V) (Note 2)		$I_{DS\ Pulse}$	19	
Operating Junction Temperature		T_J	-55 to +150	°C
Storage Temperature Range		T_S	-55 to +150	°C

Notes:

1. For ≤1 μs
2. Defined by product design and characterization. Value is not tested to full current in production.

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.4	°C/W
Junction to Ambient Thermal Resistance(Note 3)	$R_{\Theta JA}$	36	°C/W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

Notes:

3. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Drain-to-Source Blocking Voltage	V_{GS} = 0 V, I_{DSS} ≤ 18 µA	$V_{(BL)DSS}$	650	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.4mA	$V_{GS(TH)}$	1.1	1.7	2.6	V
Gate-to-Source Current	V_{GS} = 6 V, V_{DS} = 0 V	I_{GS}	--	57	--	µA
Drain-Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C	I_{DSS}	--	0.7	18	µA
	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C		--	143	--	
Drain-Source On-State Resistance	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 3.2 A	$R_{DS(on)}$	--	150	195	mΩ
	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 3.2 A		--	380	--	
Total Gate Charge	V_{GS} = 0 to 6 V V_{DS} = 400 V	Q_g	--	2.2	--	nC
Gate-Source Charge		Q_{gs}	--	0.7	--	
Gate-Drain Charge		Q_{gd}	--	0.7	--	
Output Charge	V_{GS} = 0 V, V_{DS} = 400 V	Q_{OSS}	--	19	--	
Gate Plateau Voltage	V_{DS} = 400 V,I_{DS} = 11 A	Vplat	--	3.5	--	V
Input Capacitance	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz	C_{iss}	--	70	--	pF
Output Capacitance		C_{oss}	--	20	--	
Reverse Transfer Capacitance		C_{rss}	--	0.4	--	
Effective Output Capacitance Energy Related (Note 4)	V_{GS} = 0 V V_{DS} = 0 to 400 V	$C_{O(ER)}$	--	30	--	
Effective Output Capacitance Time Related (Note 5)		$C_{O(TR)}$	--	47	--	
Internal Gate Resistance	f = 5 MHz	R_G		1.4		Ω
Reverse Recovery Charge		Qrr	--	0	--	nC

Notes:

4. $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.
5. $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Turn-On Delay	V_{DD} = 400 V, V_{GS} = 0-6 V, I_{DS} = 6 A, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 2 Ω, L = 300 µH, L_P = 9 nH (Notes 6 , 7, 8)	$t_{D(on)}$	--	5	--	nS
Rise Time		t_R	--	5	--	
Turn-Off Delay		$t_{D(off)}$	--	8	--	
Turn-Off Fall Time		t_F	--	10	--	
Switching Energy during turn-on		E_{on}	--	20	--	µJ
Switching Energy during turn-off		E_{off}	--	5.8	--	
Output Capacitance Stored Energy	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz	E_{OSS}	--	2.4	--	

Notes:

6. See Figure 16 for switching test circuit diagram.
7. See Figure 17 for switching time definition waveforms.
8. L_P = parasitic inductance

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSG65N195CE RVG	PDFN88	3000pcs / 13" Reel

Electrical Performance Graphs

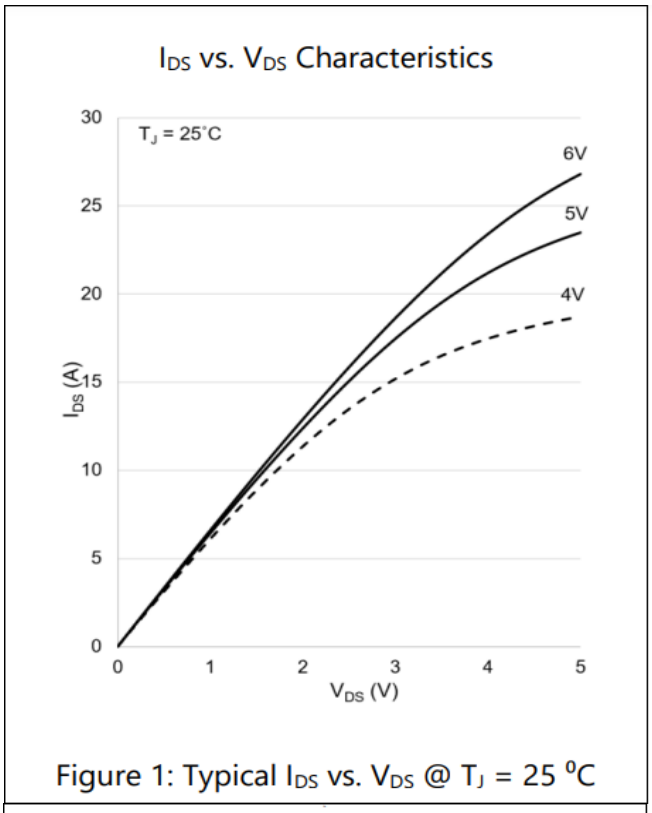


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

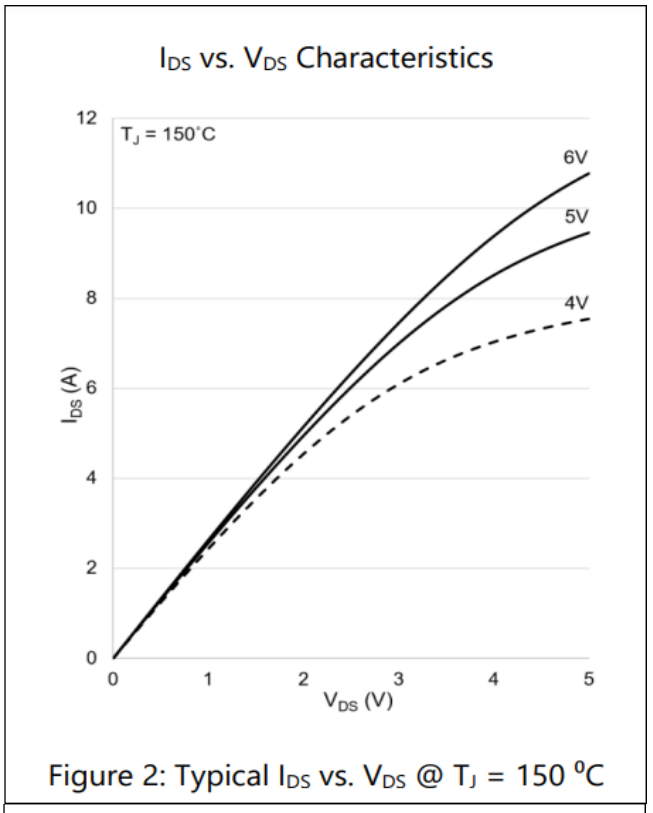


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

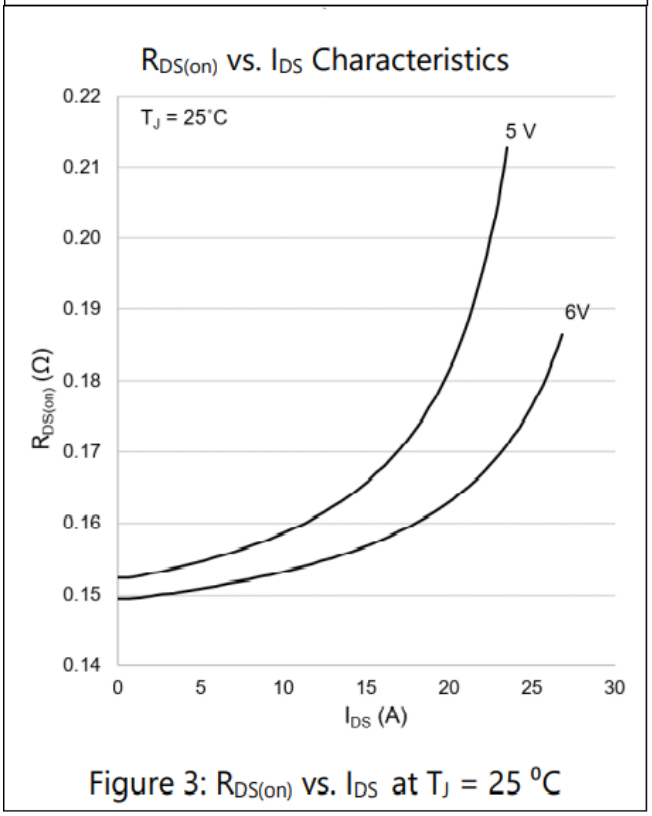


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

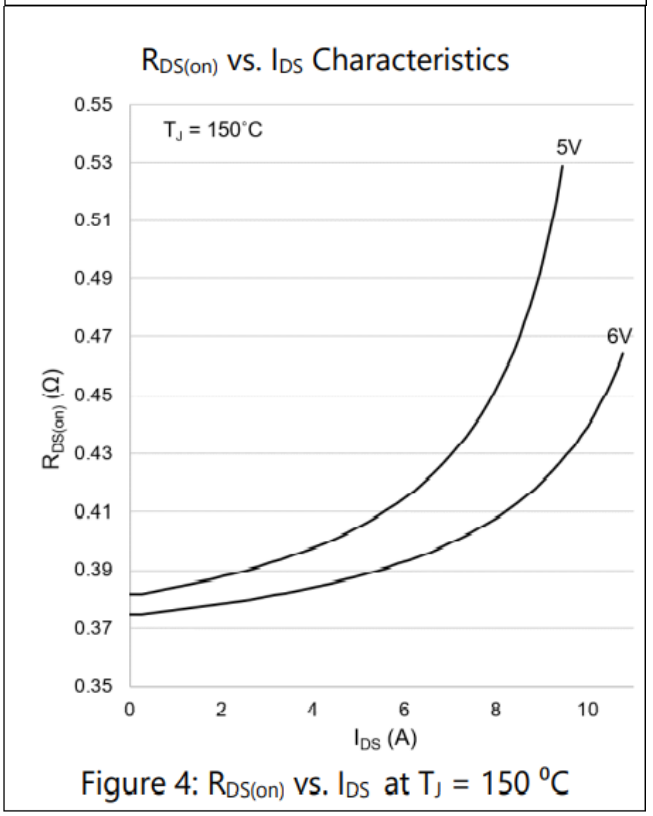


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

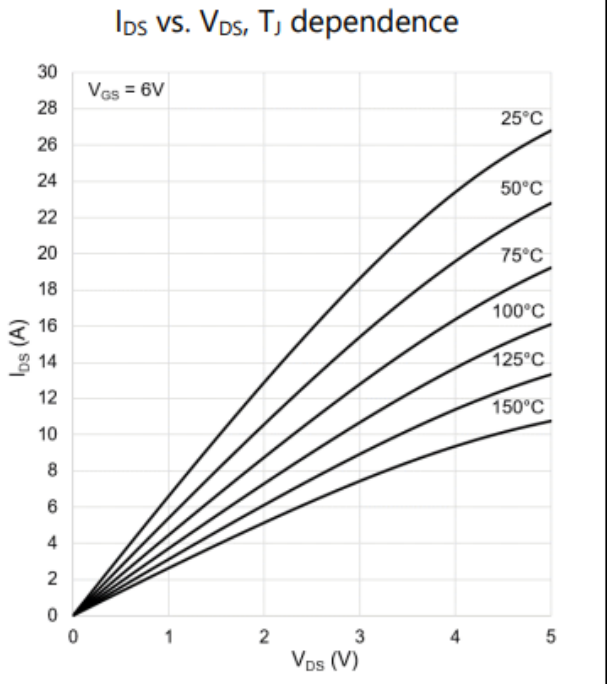


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

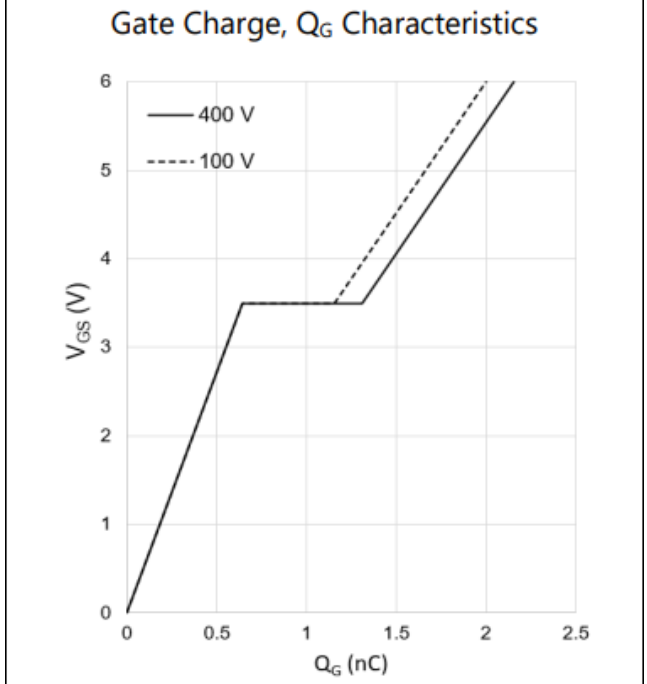


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} =100, 400 V

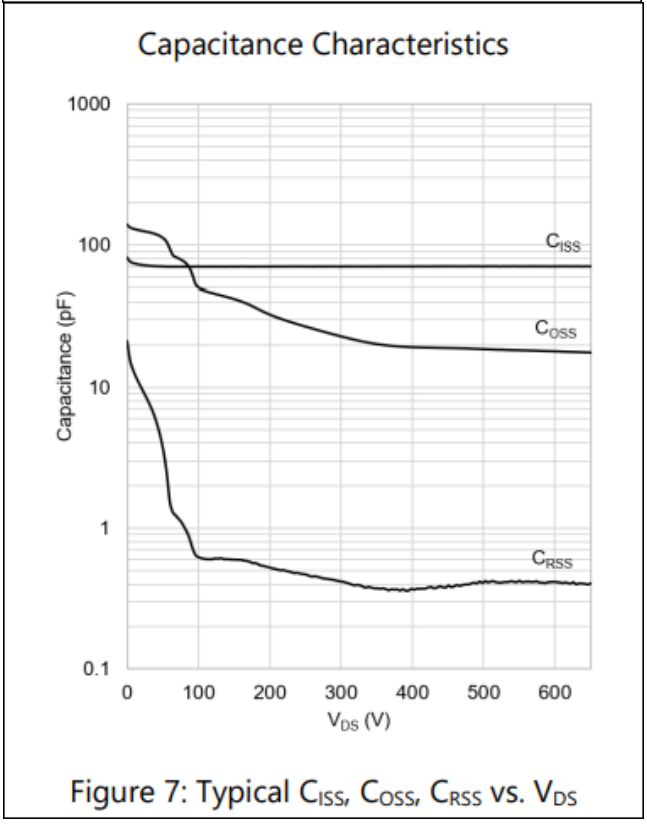


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

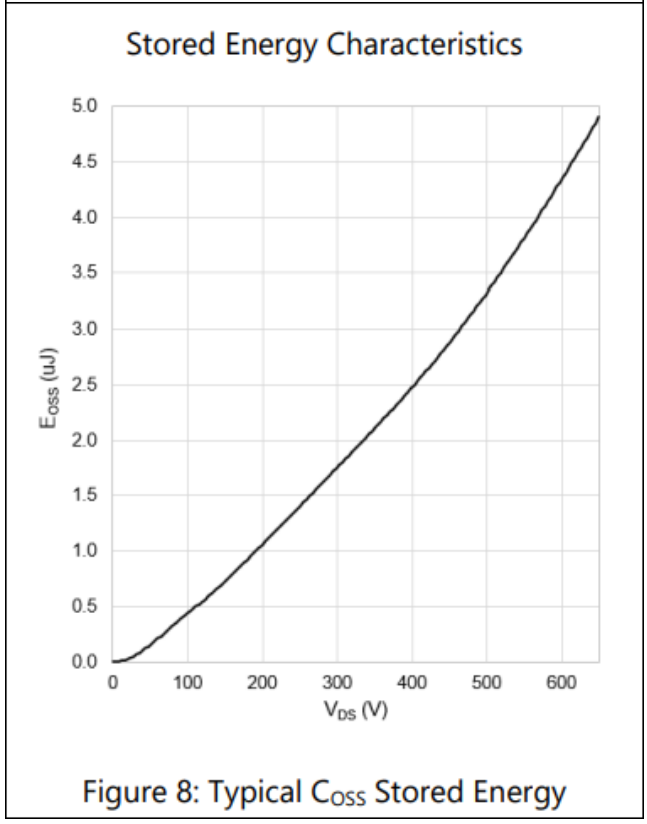


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

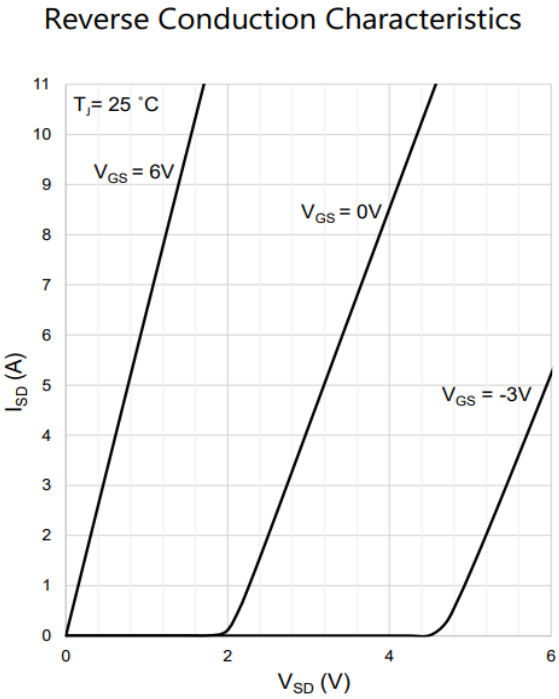


Figure 9: Typical I_{SD} vs. V_{SD} @ T_J = 25 °C

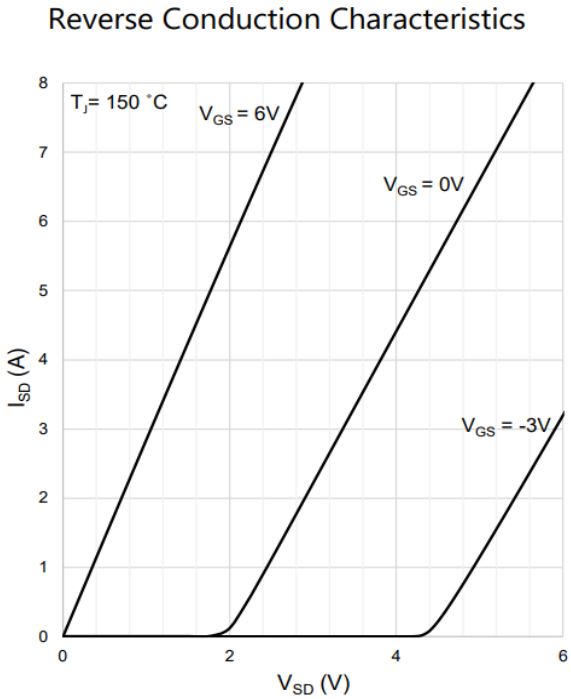


Figure 10: Typical I_{SD} vs. V_{SD} @ T_J = 150 °C

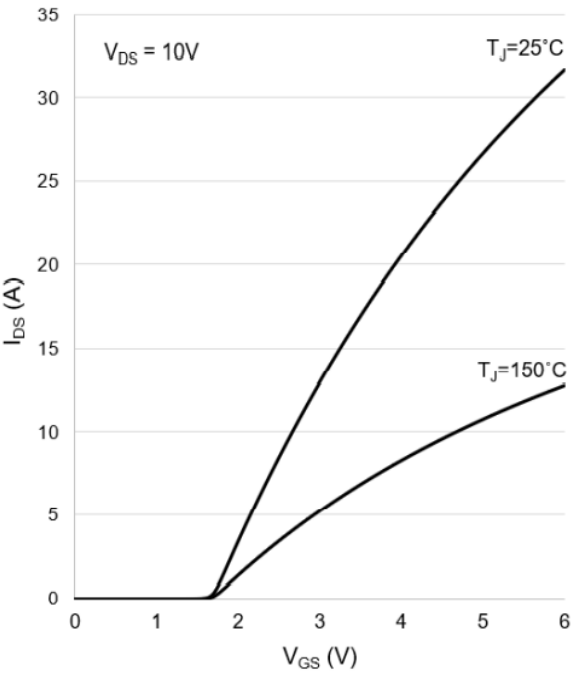


Figure 11: Typical I_{DS} vs. V_{GS}

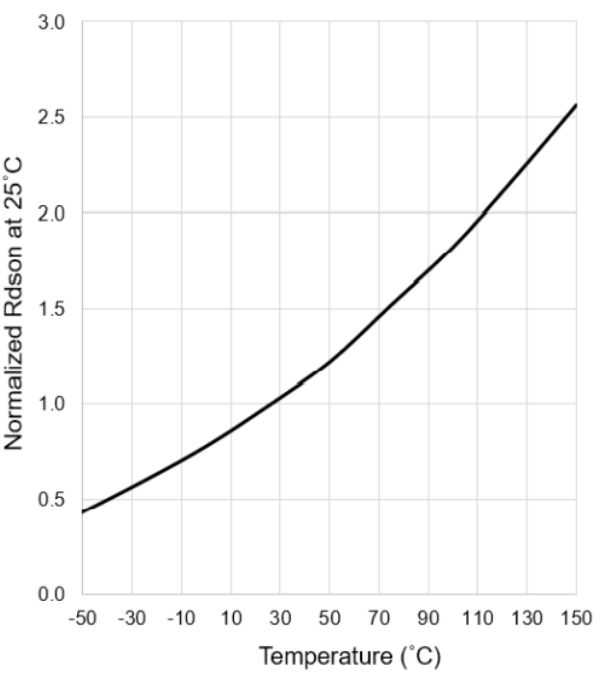


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

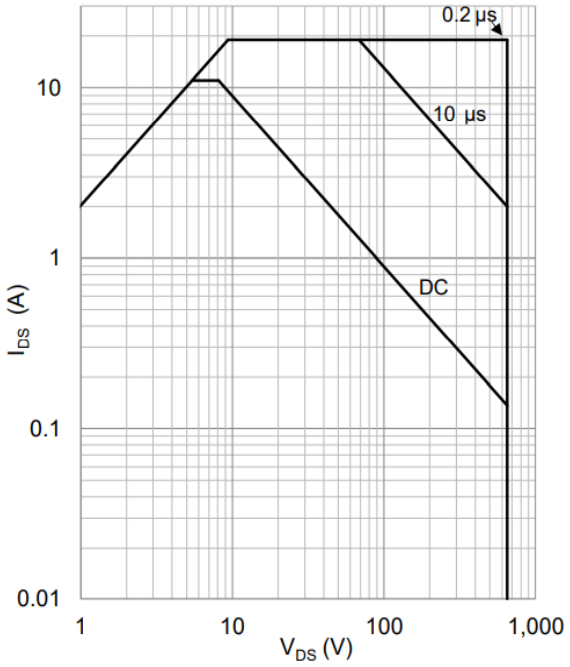


Figure 13: Safe Operating Area @ T_{case} = 25 °C

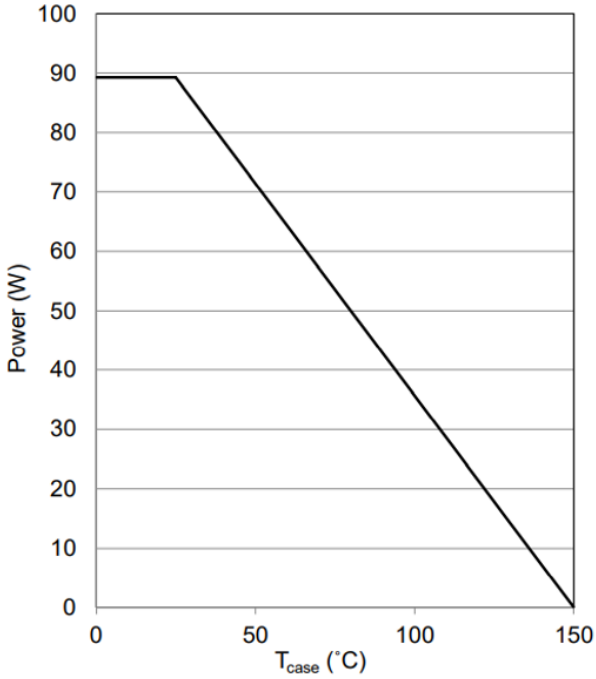


Figure 14: Power Derating vs. T_{case}

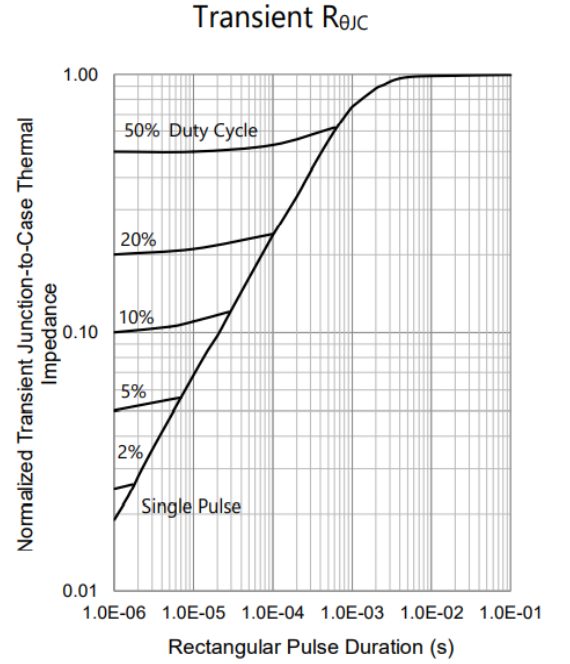


Figure 15: Transient Thermal Impedance

(1.00 = Nominal DC thermal impedance)

Test Circuits

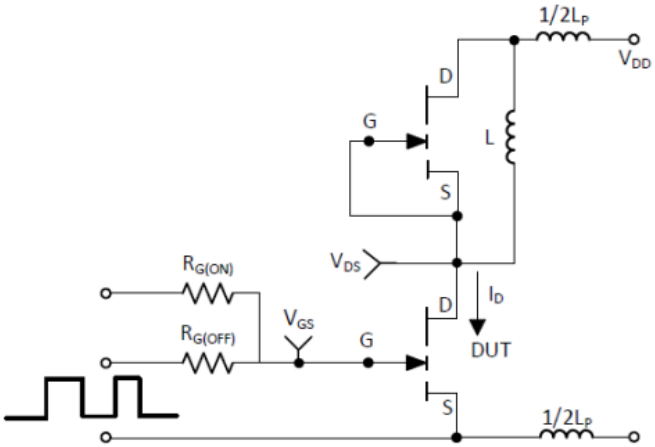
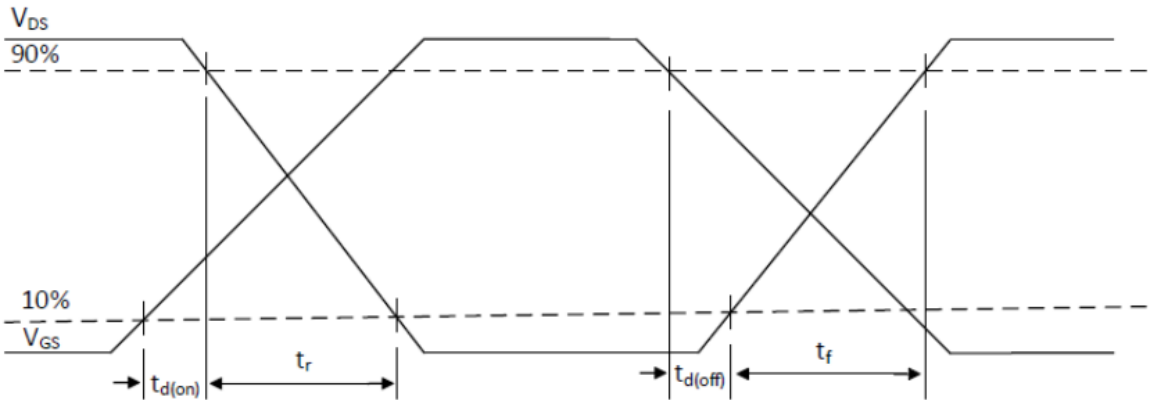
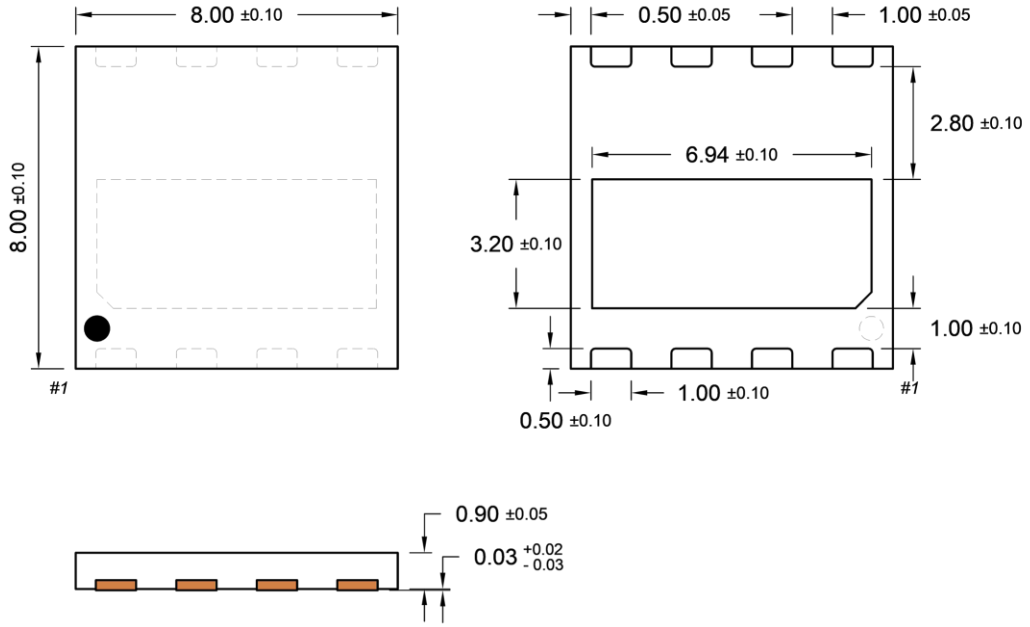


Figure 16: Switching Test Circuit

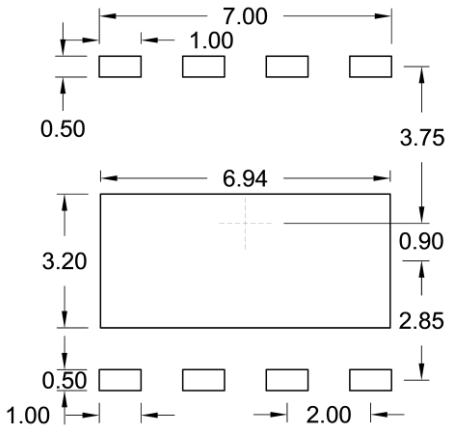


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN88



Recommended PCB Footprint



MARKING DIAGRAM

Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

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