

## N-Channel Power MOSFET

600V, 1.2A, 10Ω

### FEATURES

- Low RDS(ON) 9.4Ω (Typ.)
- Low gate charge typical @ 7.7nC (Typ.)
- Low Crss typical @ 8pF (Typ.)
- RoHS Compliant
- Halogen-free

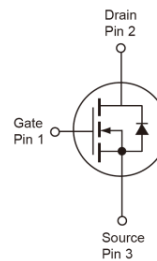
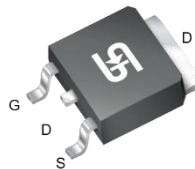
### APPLICATIONS

- Power Supply
- Lighting
- Charger

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V <sub>DS</sub>	600	V
R <sub>DS(on)</sub> (max)	10	Ω
Q <sub>g</sub>	7.7	nC



TO-252 (DPAK)



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	600	V
Gate-Source Voltage	V <sub>GS</sub>	±30	V
Continuous Drain Current	I <sub>D</sub>	1.2	A
T <sub>C</sub> = 25°C			
Pulsed Drain Current (Note 1)	I <sub>DM</sub>	4.8	A
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>D</sub>	35	W
Single Pulse Avalanche Energy (Note 2)	E <sub>AS</sub>	20	mJ
Single Pulse Avalanche Current (Note 2)	I <sub>AS</sub>	1.4	A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	R <sub>θJC</sub>	3.6	°C/W
Junction to Ambient Thermal Resistance (Note 3)	R <sub>θJA</sub>	62	°C/W

**Notes:**

1. Pulse Width ≤ 100μs.
2. L = 20mH, VGS = 10V, RG = 25Ω, Starting T<sub>J</sub> = 25°C.
3. Device on a PCB FR4 with 1 in<sup>2</sup> (single layer, 2 oz thick) copper area for drain connection.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.5	3.1	4.5	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	$I_{DSS}$	--	--	10	$\mu A$
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.6A$	$R_{DS(on)}$	--	9.4	10	$\Omega$
Forward Transconductance	$V_{DS} = 10V, I_D = 0.6A$	$g_{fs}$	--	1.5	--	S
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 480V, I_D = 0.29A,$ $V_{GS} = 10V$	$Q_g$	--	7.7	--	nC
Gate-Source Charge		$Q_{gs}$	--	1	--	
Gate-Drain Charge		$Q_{gd}$	--	4.6	--	
Input Capacitance	$V_{DS} = 300V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	$C_{iss}$	--	150	--	pF
Output Capacitance		$C_{oss}$	--	11	--	
Reverse Transfer Capacitance		$C_{rss}$	--	8	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	--	4.1	--	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 300V, R_G = 3.3\Omega,$ $I_D = 0.29A, V_{GS} = 10V$	$t_{d(on)}$	--	4.5	--	ns
Turn-On Rise Time		$t_r$	--	3.7	--	
Turn-Off Delay Time		$t_{d(off)}$	--	13	--	
Turn-Off Fall Time		$t_f$	--	64	--	
<b>Source-Drain Diode</b>						
Body-Diode Continuous Forward Current		$I_S$	--	--	1.2	A
Body-Diode Pulsed Current (Note 1)		$I_{SM}$	--	--	4.8	A
Forward Voltage (Note 4)	$I_S = 0.6A, V_{GS} = 0V$	$V_{SD}$	--	0.8	1.4	V

**Notes:**

- Pulse test: Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

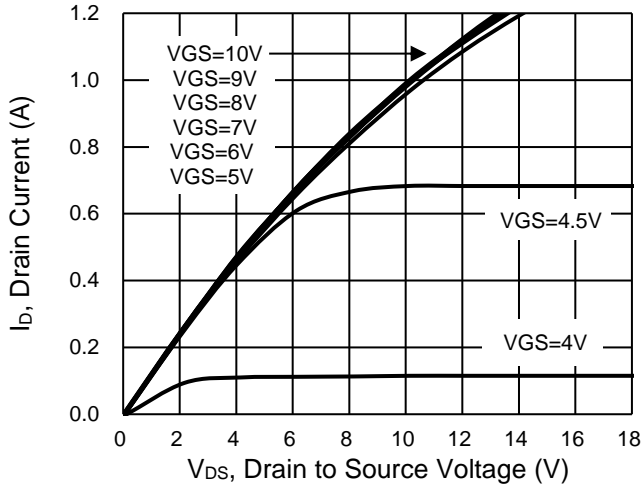
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TSM1NB60CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

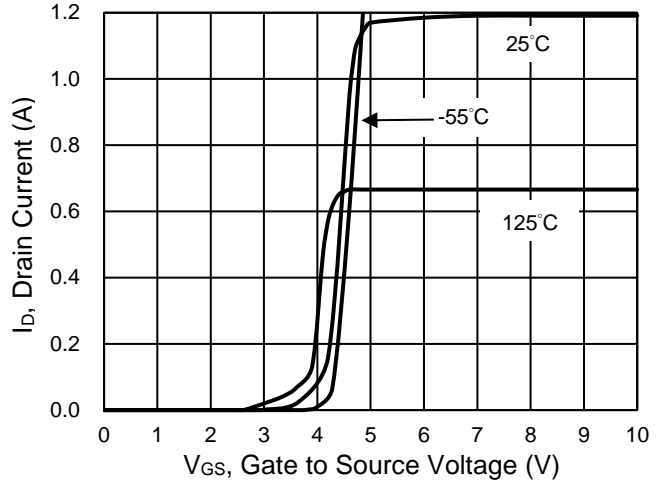
**CHARACTERISTICS CURVES**

( $T_c = 25^\circ\text{C}$  unless otherwise noted)

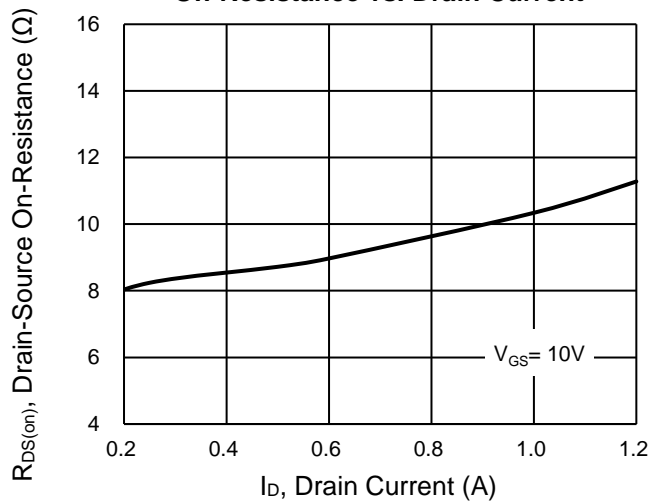
**Output Characteristics**



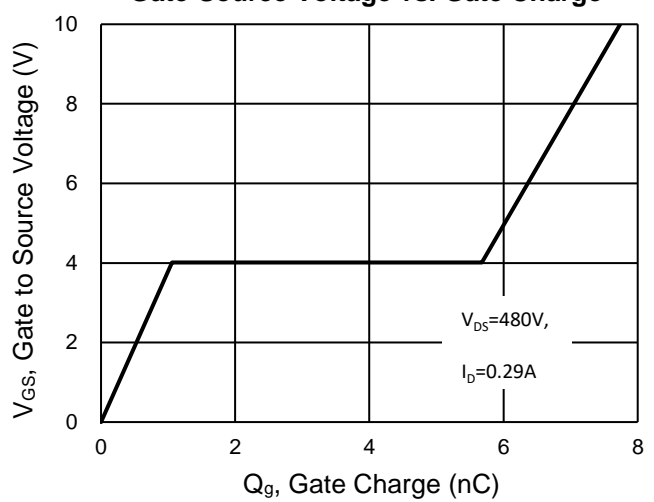
**Transfer Characteristics**



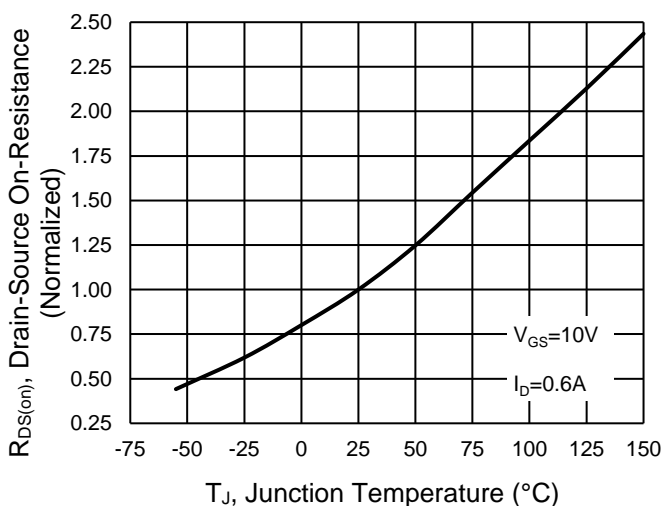
**On-Resistance vs. Drain Current**



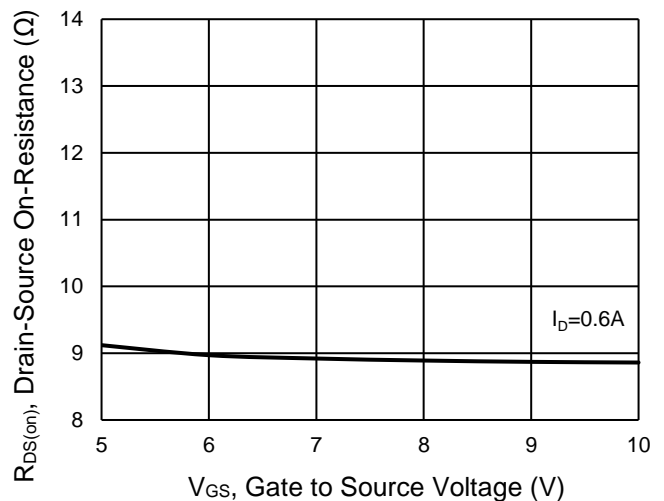
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



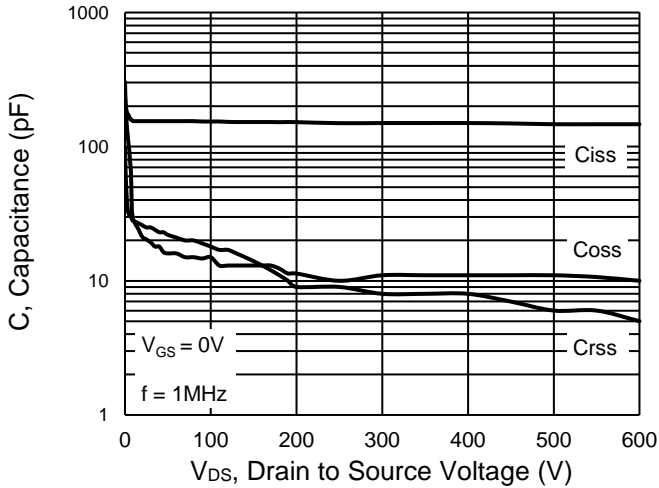
**On-Resistance vs. Gate-Source Voltage**



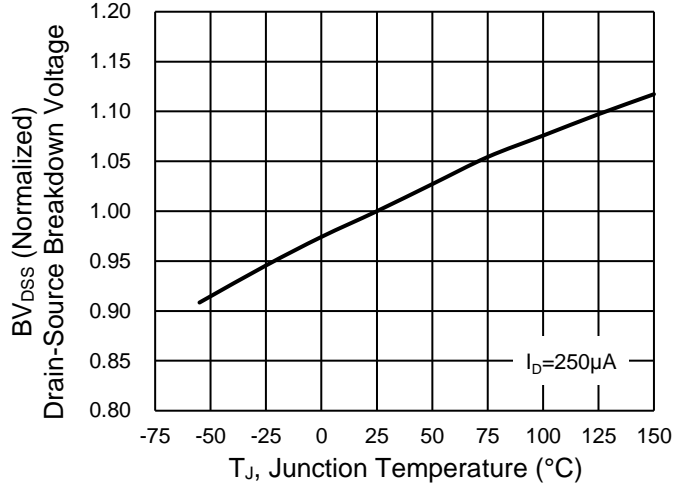
**CHARACTERISTICS CURVES**

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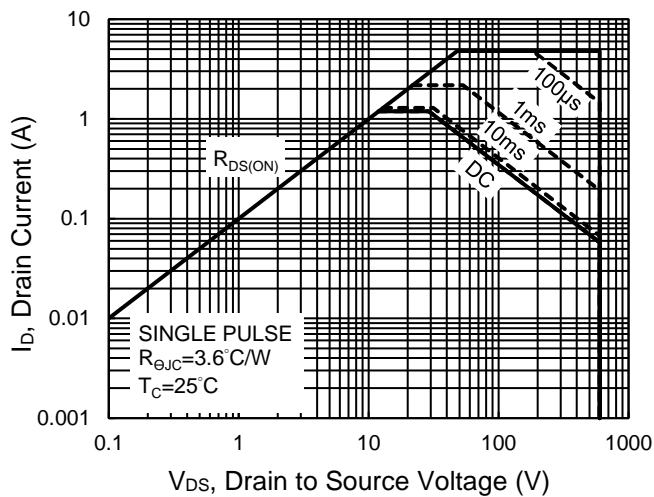
**Capacitance vs. Drain-Source Voltage**



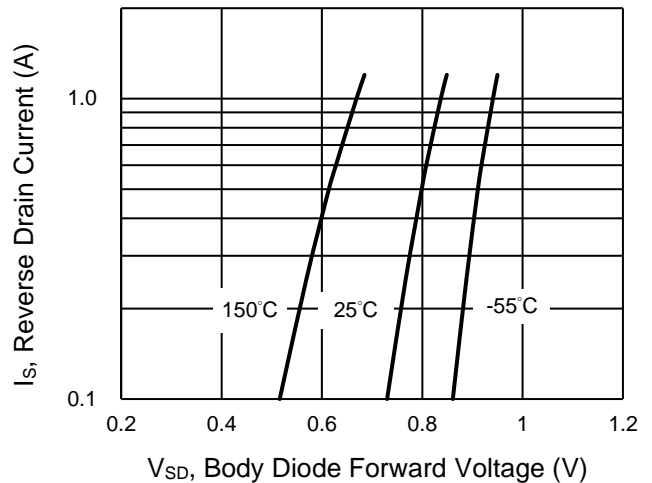
**BV<sub>DSS</sub> vs. Junction Temperature**



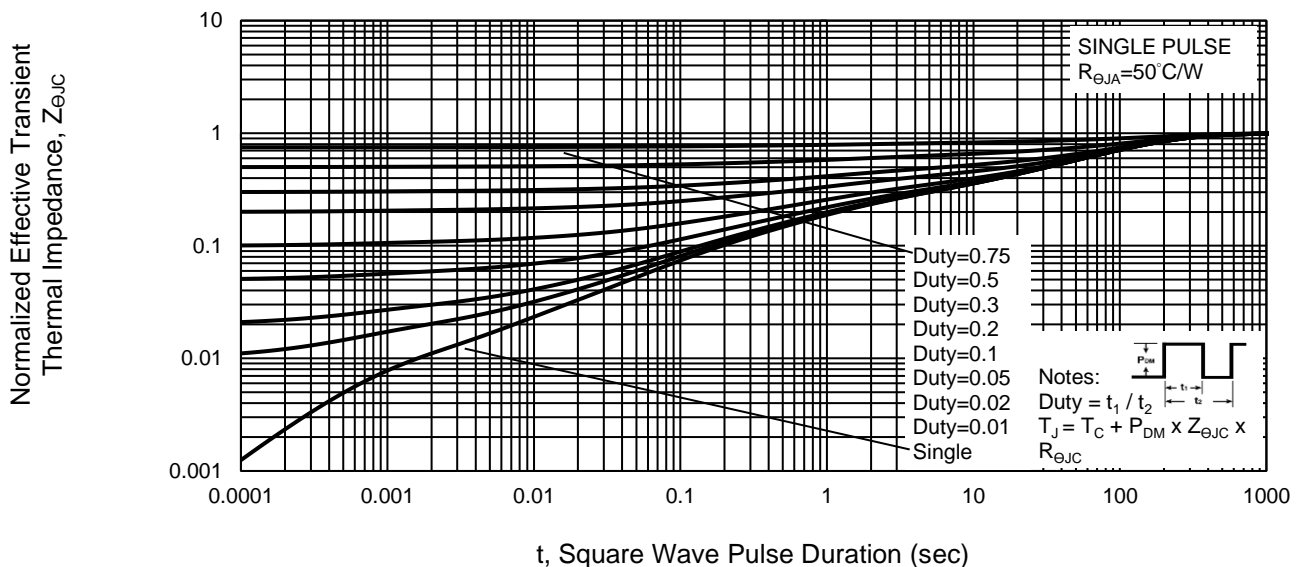
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**



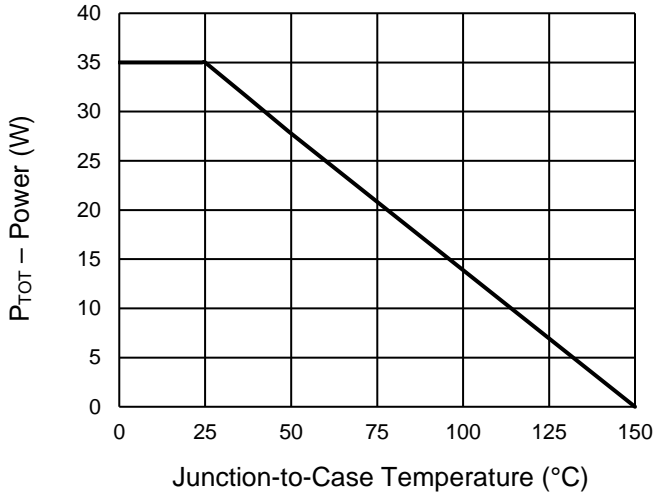
**Normalized Thermal Transient Impedance, Junction-to-Case**



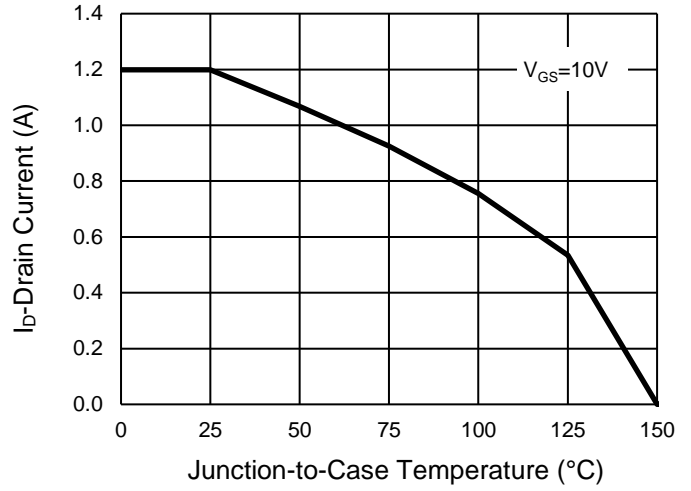
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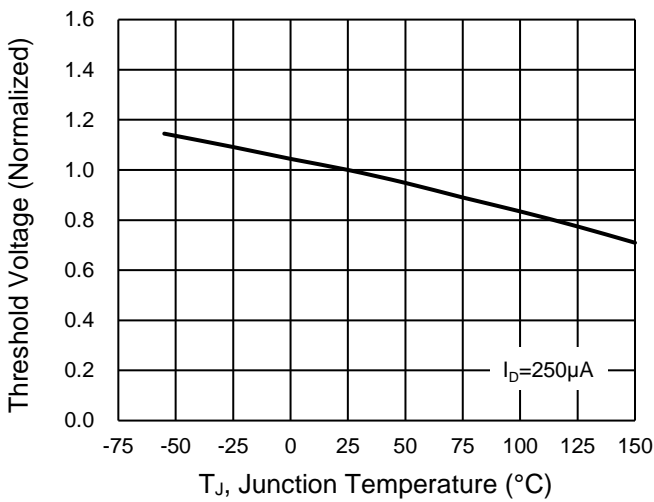
**Power Dissipation**



**Drain Current**

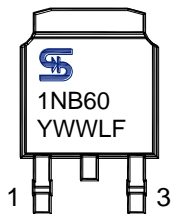
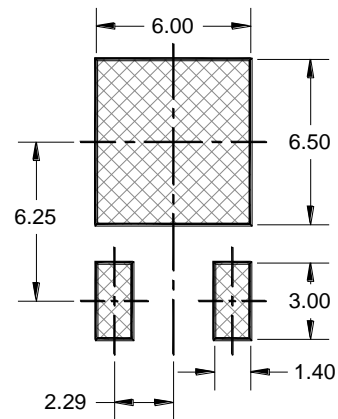
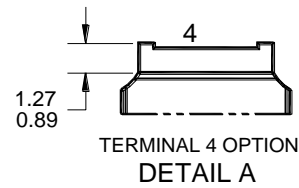
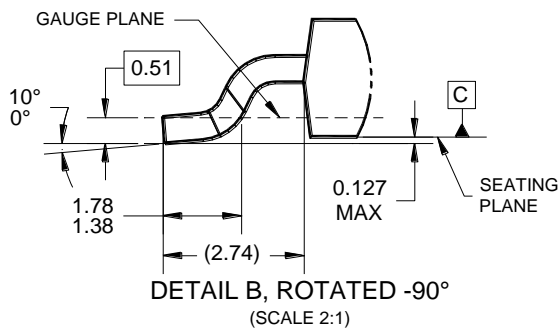
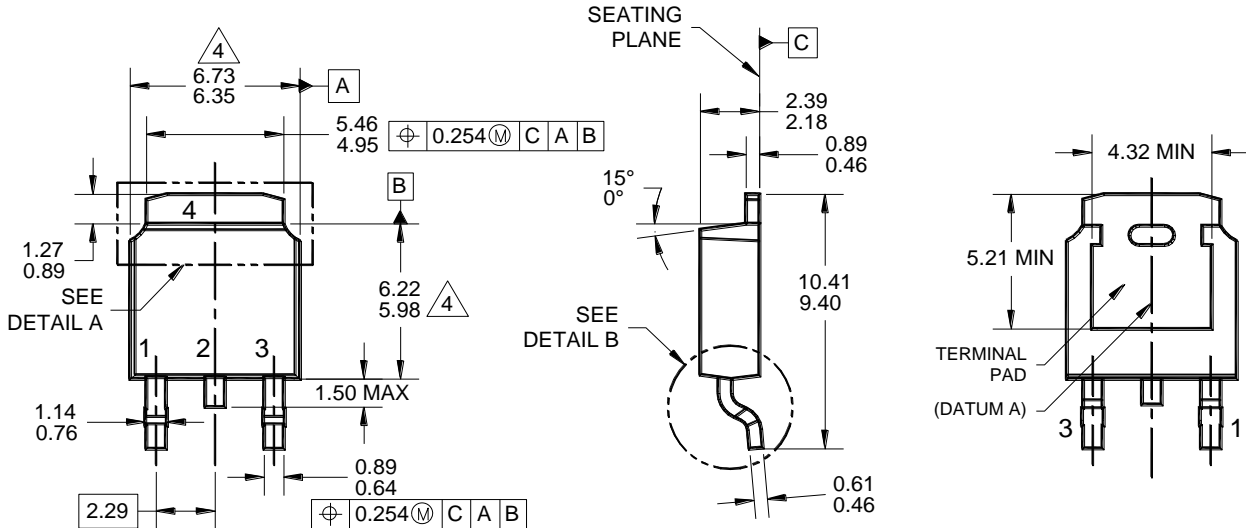


**Normalized gate threshold voltage vs Temperature**



**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

**TO-252 (DPAK)**



**MARKING DIAGRAM**

- P/N = MARKING CODE
- Y = YEAR CODE
- WW = WEEK CODE (01 ~ 52)
- L = LOT CODE (1~9, A~Z)
- F = FACTORY CODE

**NOTES: UNLESS OTHERWISE SPECIFIED**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-TO252AA-013 REV B.

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