

N-Channel Power MOSFET

FEATURES

- Low gate charge for fast power switching
- Low $R_{DS(on)}$ to minimize conductive losses
- RoHS compliant
- Halogen-free

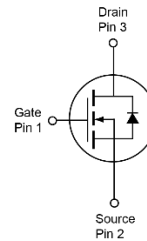
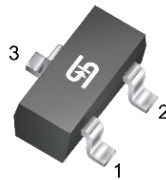
APPLICATIONS

- Switching mode power
- Battery protection

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	20	V
$R_{DS(on)}$ (max)	$V_{GS} = 4.5V$	65
	$V_{GS} = 2.5V$	95
Q_g	5.9	nC



SOT-23



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	$T_A = 25^\circ C$	I_D	3.2
Pulsed Drain Current (Note 1)		I_{DM}	12.8
Total Power Dissipation	$T_A = 25^\circ C$	P_D	1.04
	$T_A = 70^\circ C$		0.67
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ C$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance (Note 2)	$R_{\theta JA}$	120	$^\circ C/W$

Notes:

1. Pulse Width $\leq 100\mu s$.
2. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.65	0.8	1.2	V
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
	$V_{DS} = 20V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$				100	μA
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 3.2A$	$R_{DS(on)}$	--	22	65	m Ω
	$V_{GS} = 2.5V, I_D = 2.7A$			28	95	
Forward Transconductance	$V_{DS} = 10V, I_D = 0.8A$	g_{fs}	--	11	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{DS} = 10V, I_D = 3.2A,$ $V_{GS} = 4.5V$	Q_g	--	5.9	--	nC
Gate-Source Charge		Q_{gs}	--	0.8	--	
Gate-Drain Charge		Q_{gd}	--	1.6	--	
Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	446	--	pF
Output Capacitance		C_{oss}	--	76	--	
Reverse Transfer Capacitance		C_{rss}	--	63	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	2.2	--	Ω
Switching (Note 5)						
Turn-On Delay Time	$V_{DD} = 10V, R_G = 2\Omega,$ $I_D = 3.2A, V_{GS} = 4.5V$	$t_{d(on)}$	--	4.8	--	ns
Turn-On Rise Time		t_r	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17	--	
Turn-Off Fall Time		t_f	--	2.1	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$I_S = 3.2A, V_{GS} = 0V$	V_{SD}	--	0.8	1.2	V
Reverse Recovery Time	$I_S = 3.2A,$ $di/dt = 100A/\mu s$	t_{rr}	--	16	--	ns
Reverse Recovery Charge		Q_{rr}	--	6.4	--	nC

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

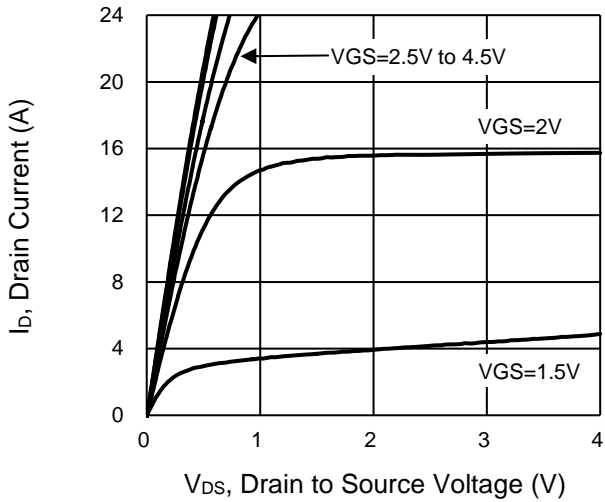
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM2302CX RFG	SOT-23	3kpcs / 7" Reel

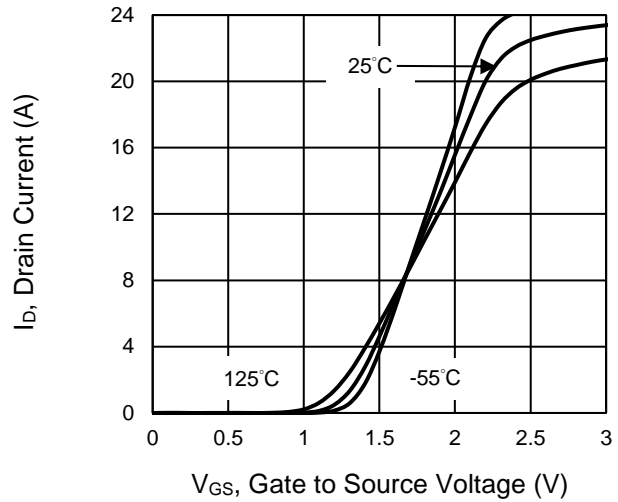
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

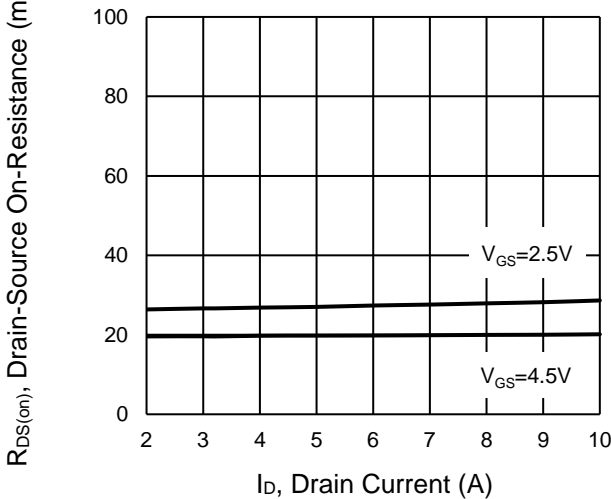
Output Characteristics



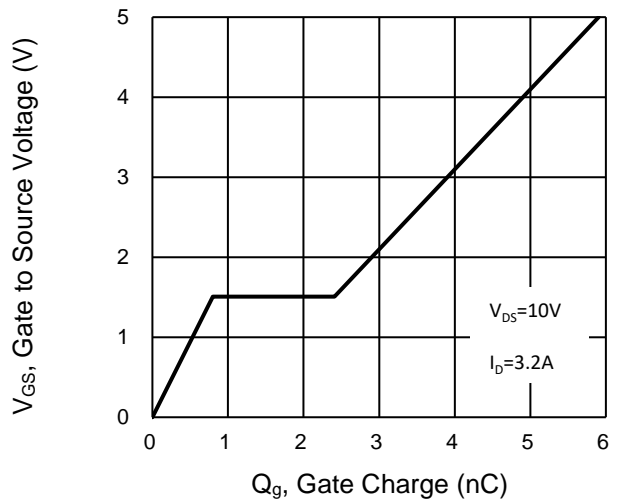
Transfer Characteristics



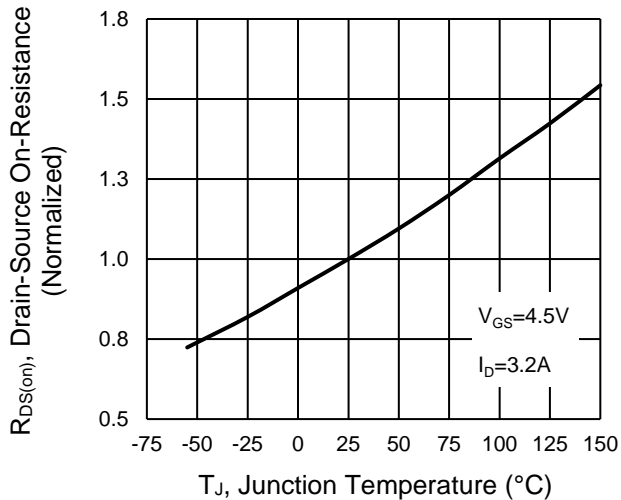
On-Resistance vs. Drain Current



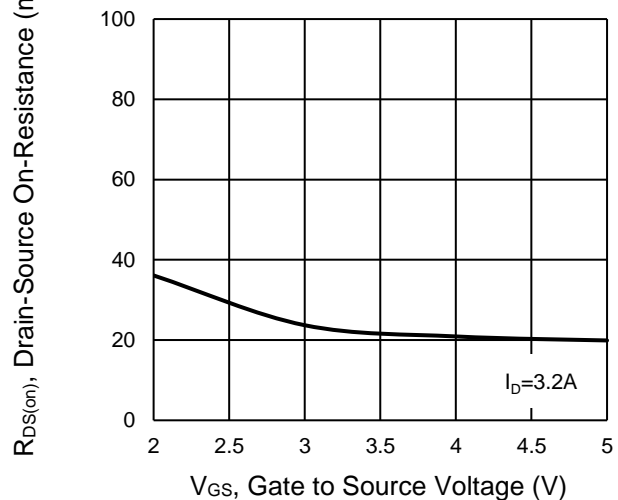
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



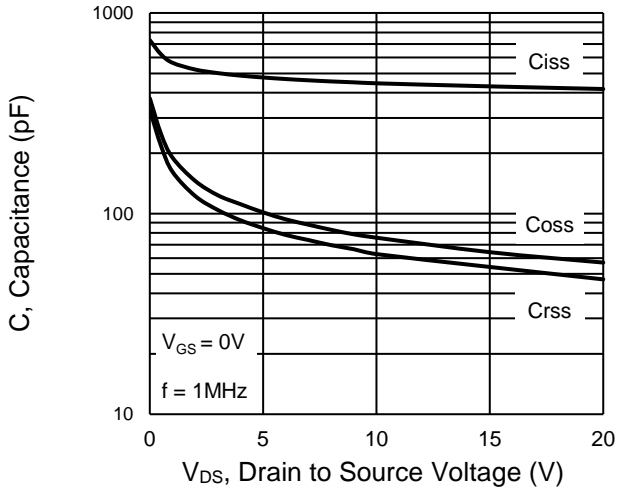
On-Resistance vs. Gate-Source Voltage



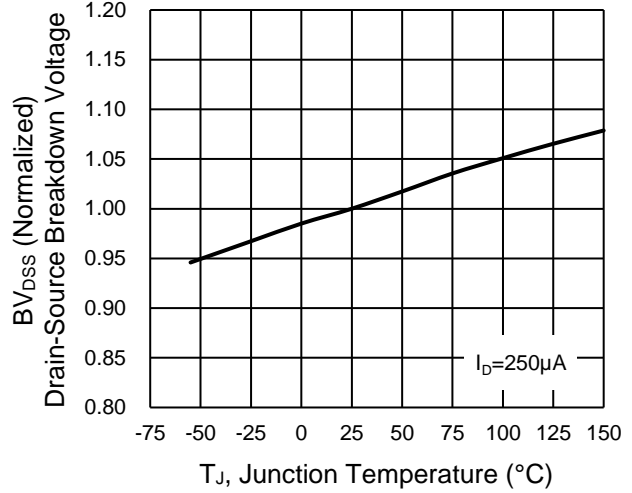
CHARACTERISTICS CURVES

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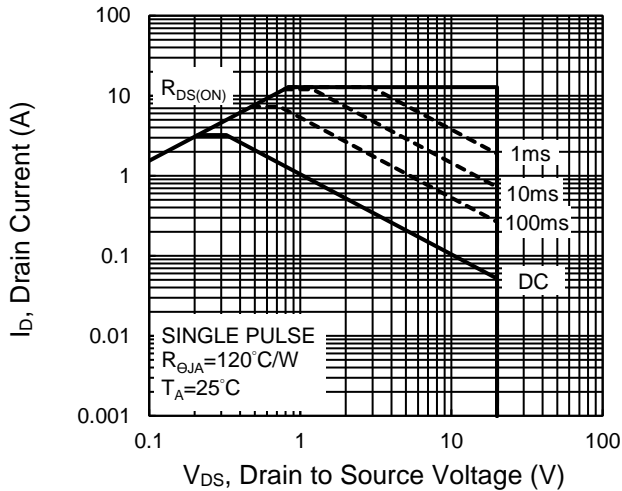
Capacitance vs. Drain-Source Voltage



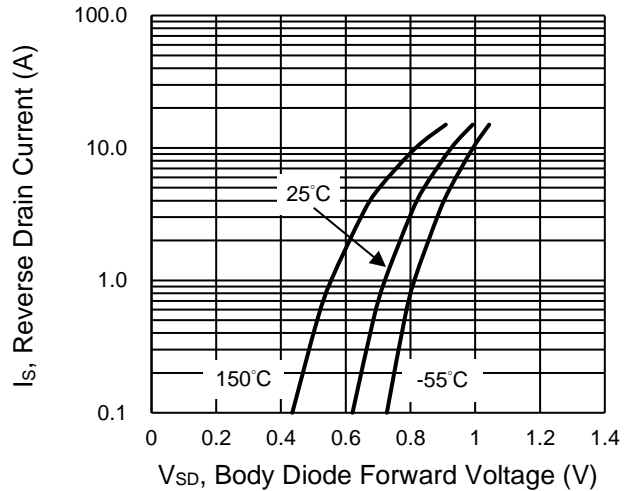
BV_{DSS} vs. Junction Temperature



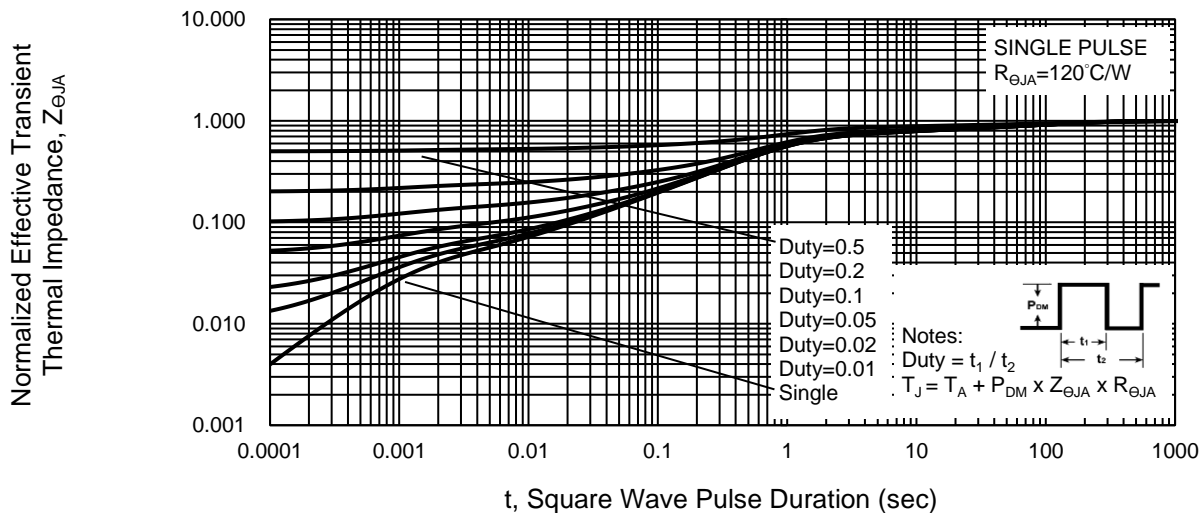
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage



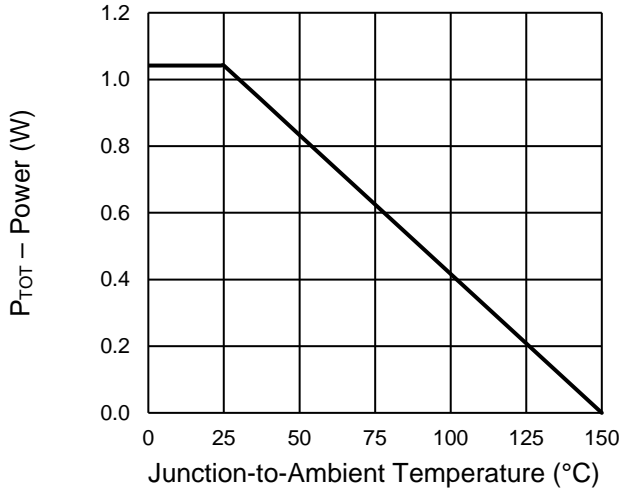
Normalized Thermal Transient Impedance, Junction-to-Ambient



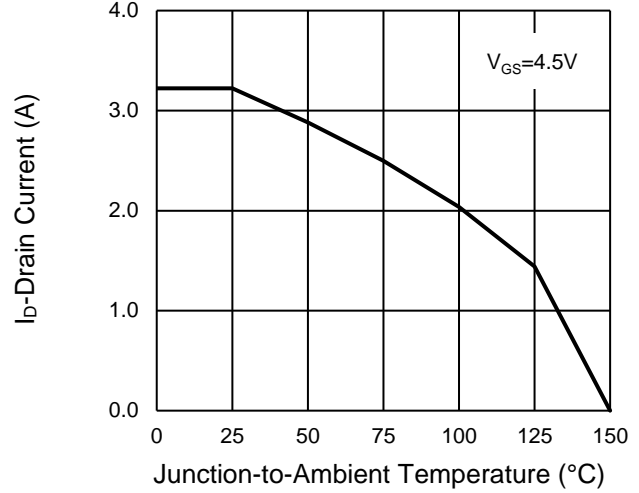
CHARACTERISTICS CURVES

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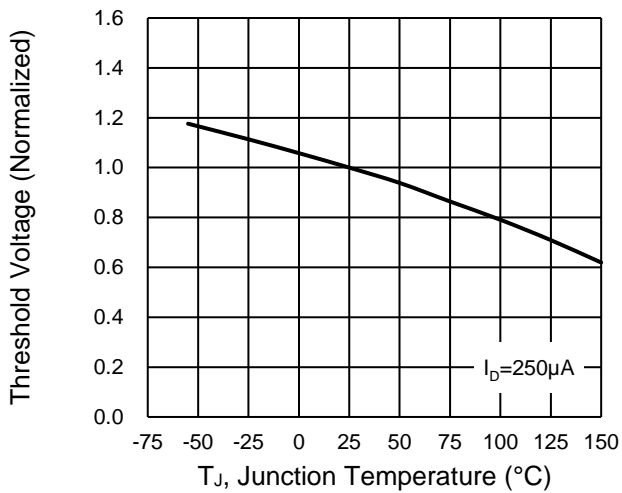
Power Dissipation



Drain Current

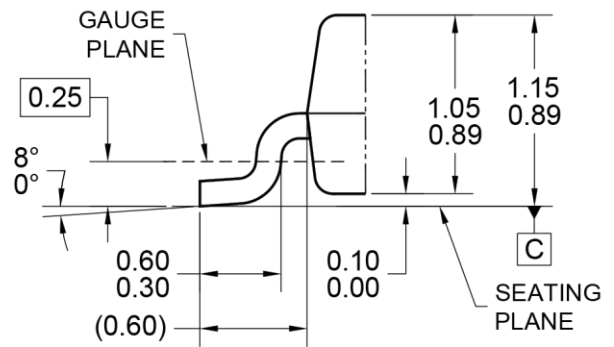
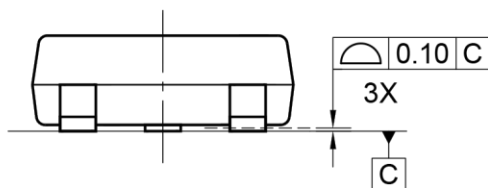
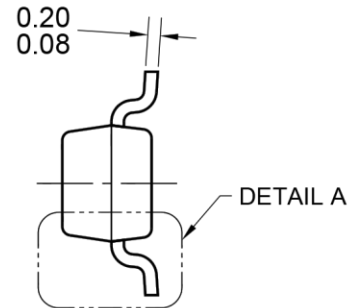
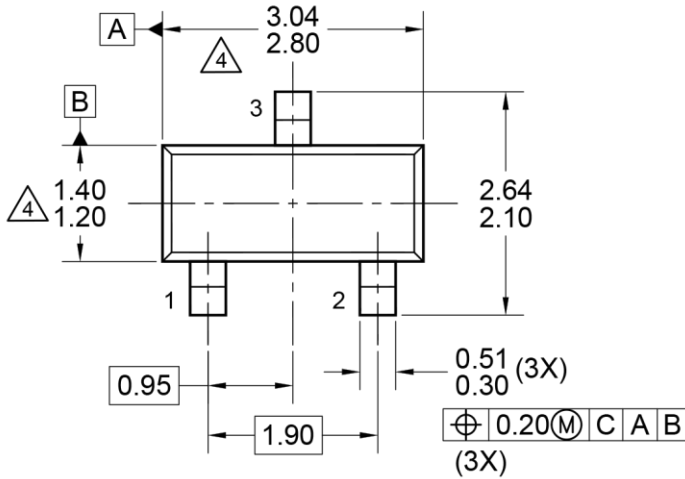


Normalized gate threshold voltage vs Temperature

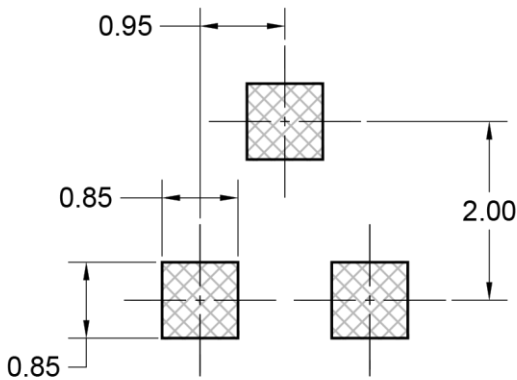


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

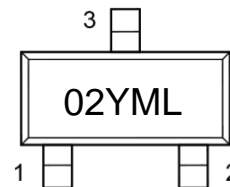
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DETAIL A, ROTATED -90°
(SCALE 2:1)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-236, ISSUE H, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-SOT23JEDEC-104 REV A.

- 02 = Device marking
- Y = Year Code
- M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code

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