

N-Channel Power MOSFET

60V, 5.9A, 55mΩ

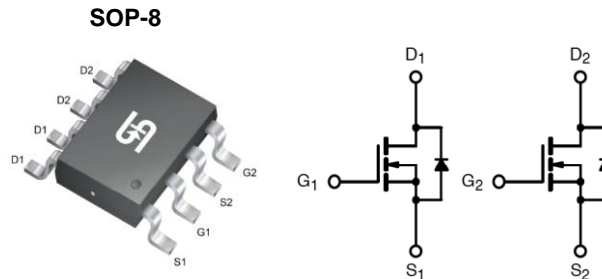
FEATURES

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- RoHS Compliant
- Halogen-free

APPLICATIONS

- High-Side DC/DC Conversion
- Notebook
- Sever

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	60	V
$R_{DS(on)}$ (max)	55	mΩ
Q_g	21	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	5.9	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	4.5	A
Pulsed Drain Current		I_{DM}	30	A
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2	W
	$T_A = 75^\circ\text{C}$		1.2	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	32	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. The $R_{\theta JA}$ limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1	--	3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}	--	--	2	μA
Drain-Source On-State Resistance (Note 2)	$V_{GS} = 10V, I_D = 4.5A$	$R_{DS(on)}$	--	45	55	m Ω
	$V_{GS} = 4.5V, I_D = 3.9A$		--	55	75	
Forward Transconductance (Note 2)	$V_{DS} = 15V, I_D = 4.5A$	g_{fs}	--	13	--	S
Dynamic (Note 3)						
Total Gate Charge	$V_{DS} = 30V, I_D = 4.5A,$ $V_{GS} = 10V$	Q_g	--	19	30	nC
Gate-Source Charge		Q_{gs}	--	4	--	
Gate-Drain Charge		Q_{gd}	--	3	--	
Input Capacitance	$V_{DS} = 24V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	1203	--	pF
Output Capacitance		C_{oss}	--	63	--	
Reverse Transfer Capacitance		C_{rss}	--	45	--	
Switching (Note 4)						
Turn-On Delay Time	$V_{DD} = 30V, R_G = 6\Omega,$ $I_D = 1A, V_{GS} = 10V$	$t_{d(on)}$	--	13	20	ns
Turn-On Rise Time		t_r	--	11	20	
Turn-Off Delay Time		$t_{d(off)}$	--	36	60	
Turn-Off Fall Time		t_f	--	11	20	
Source-Drain Diode						
Diode Forward Voltage (Note 2)	$I_S = 2A, V_{GS} = 0V$	V_{SD}	--	0.9	1.2	V

Notes:

1. Package current limit.
2. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Defined by design. Not subject to production test.
4. Switching time is essentially independent of operating temperature.

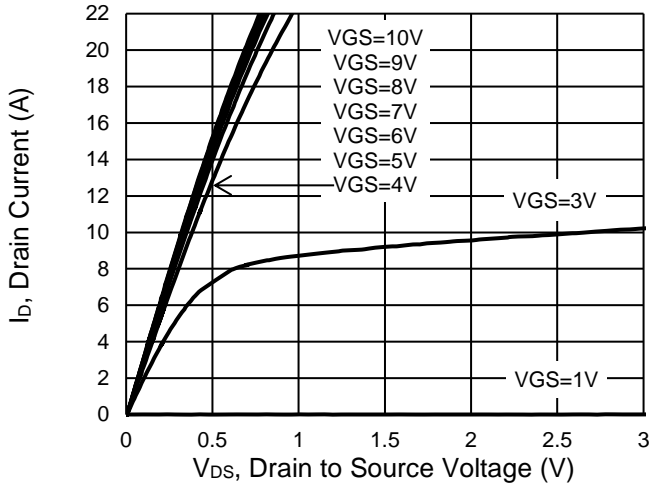
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM4946DCS RLG	SOP-8	2.5Kpcs / 13" Reel

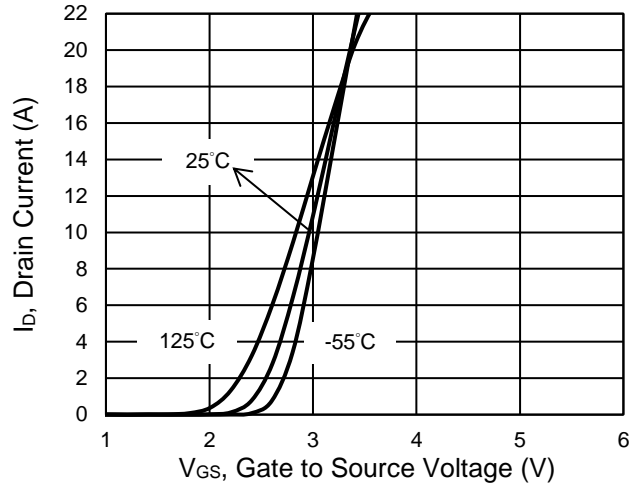
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

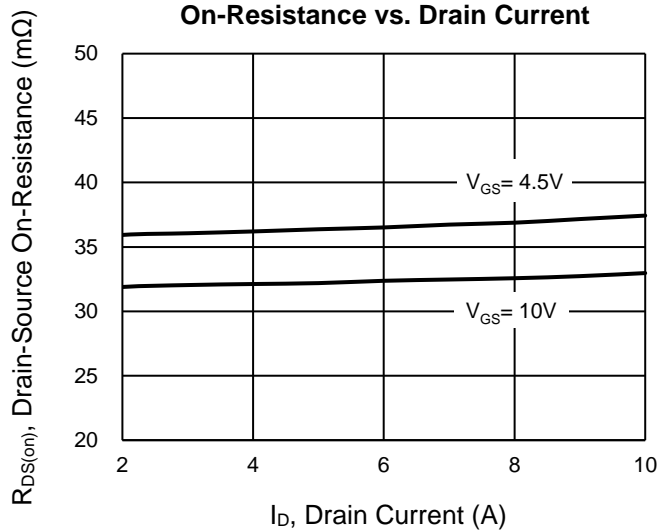
Output Characteristics



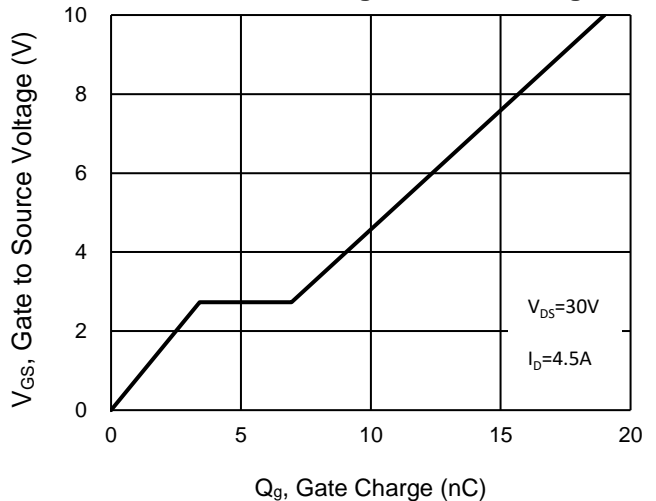
Transfer Characteristics



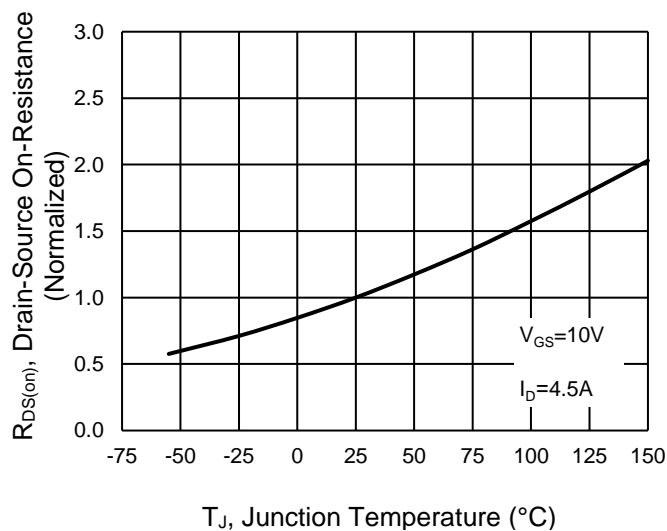
On-Resistance vs. Drain Current



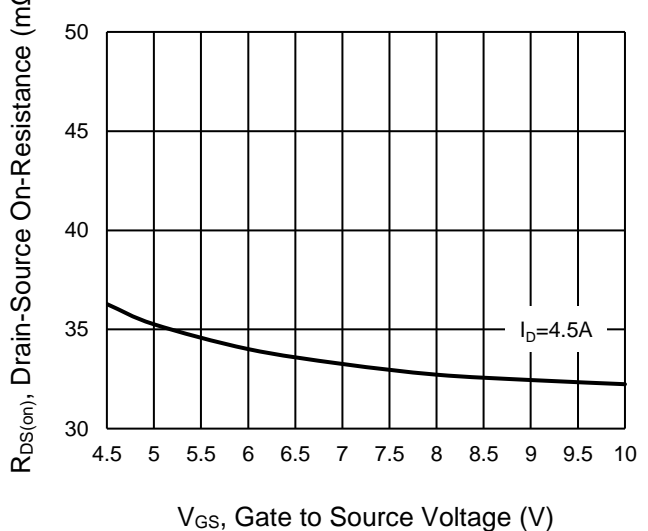
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



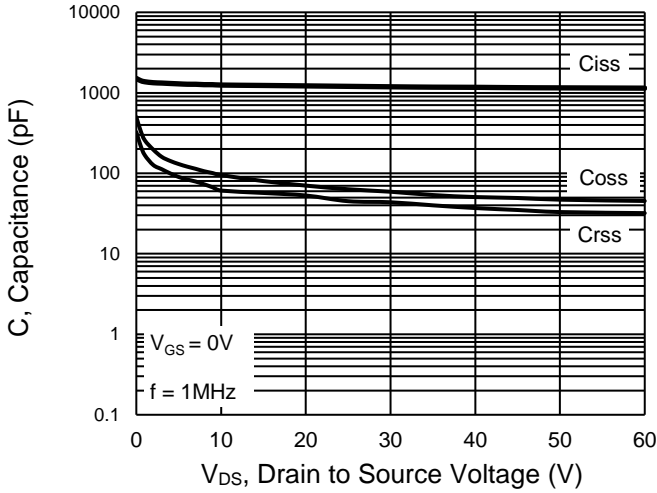
On-Resistance vs. Gate-Source Voltage



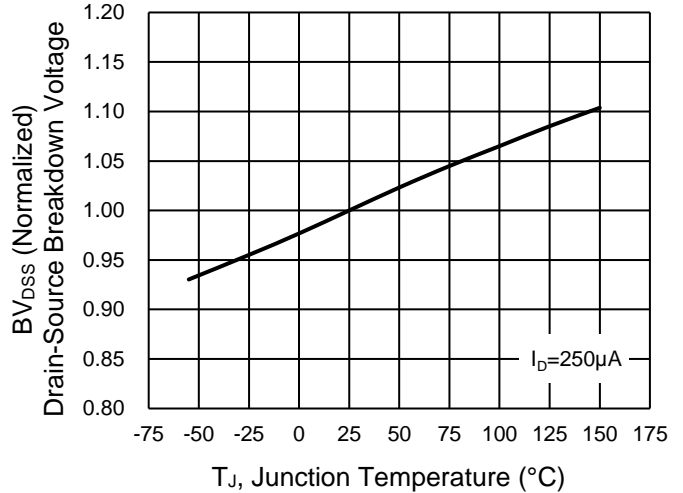
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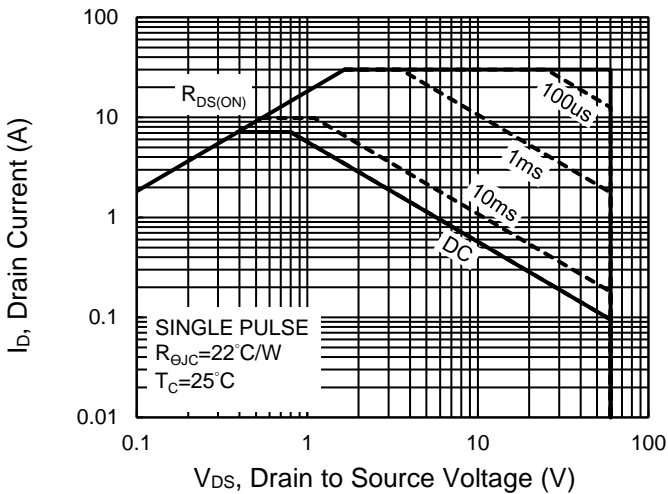
Capacitance vs. Drain-Source Voltage



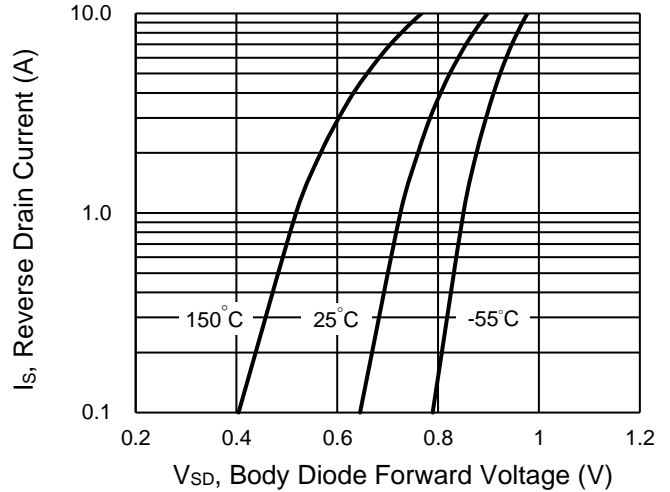
BV_{DSS} vs. Junction Temperature



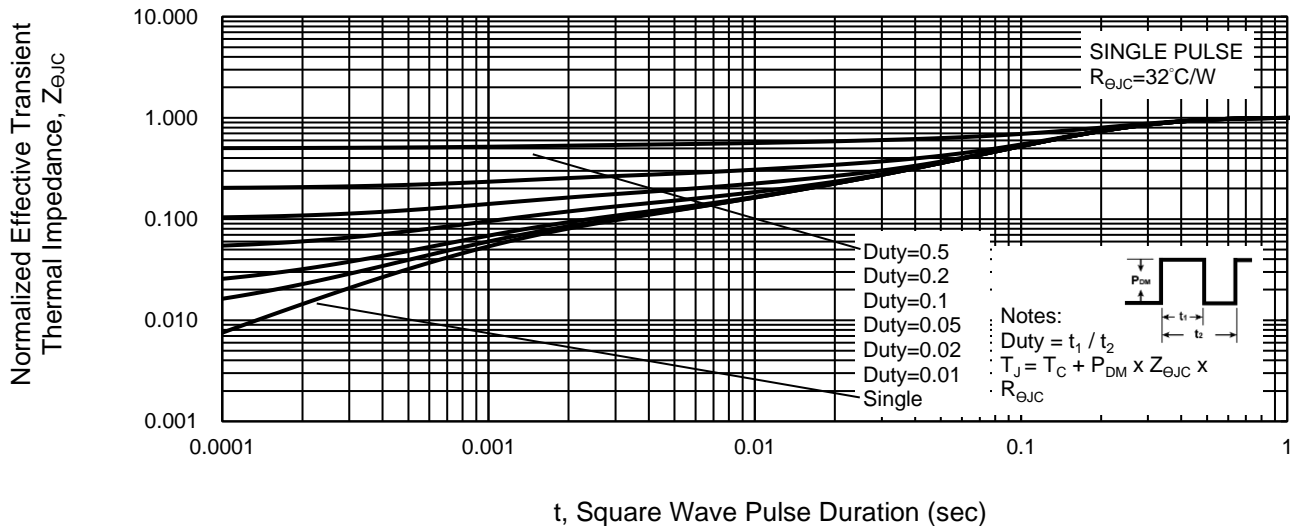
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



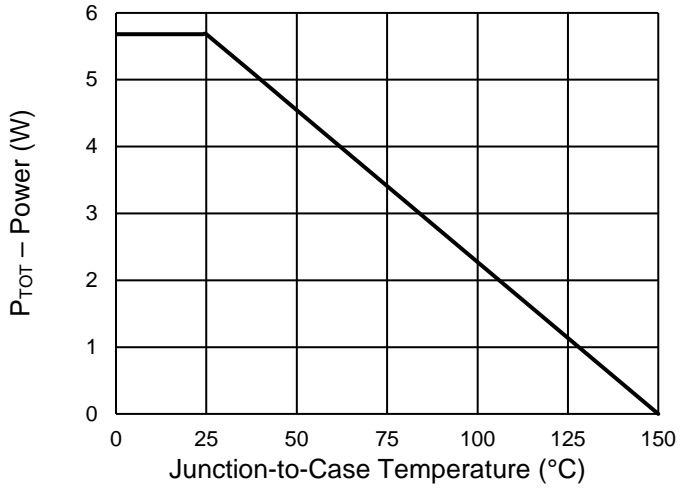
Normalized Thermal Transient Impedance, Junction-to-Case



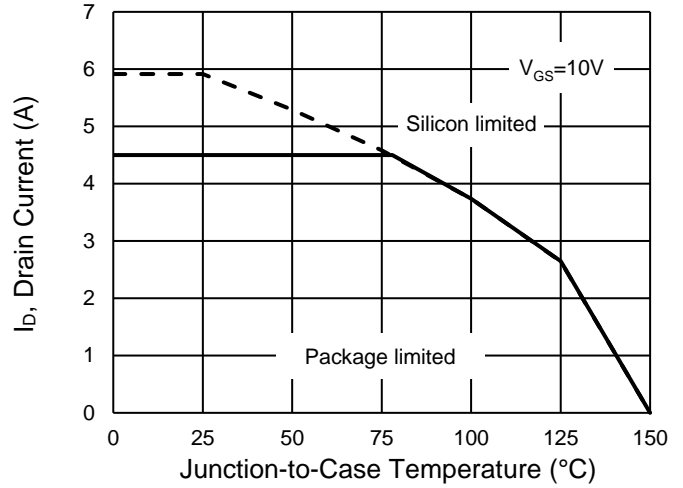
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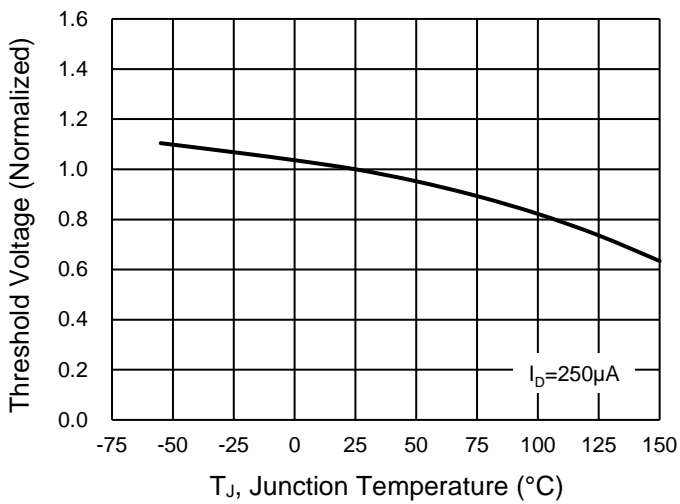
Power Dissipation



Drain Current



Normalized gate threshold voltage vs Temperature



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