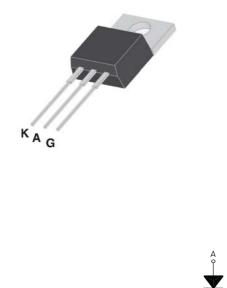


TO-220-AB



On-State Current

Gate Trigger Current

8 Amp

 $< 200 \, \mu A$

Off-State Voltage

400 V ÷ 800 V

FEATURES

- Glass/passivated die junctions
- Low current SCR
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C

MECHANICAL DATA

- Case: TO-220-AB. Epoxy meets UL 94V-0 flammability rating.
- Polarity: As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

TYPICAL APPLICATIONS

Thanks to highly sensitive triggering levels, the FS02xxxN SCR series is suitable for all applications where available gate current is limited, such as ground fault circuit interruptors, pilot circuits in solid state relays, stand-by mode power supplies, smoke and alarm detectors.

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
I _{T(RMS)}	On-state Current	180 ° Conduction Angle, T _C = 110 °C	8	А
I _{T(AV)}	Average On-state Current	180 ° Conduction Angle, T _C = 110 °C	5	А
I _{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	73	А
I _{TSM}	Non-repetitive On-State Current	Halfl Cycle, 50 Hz	70	А
I ² t	Fusing Current	tp = 10 ms, Half Cycle	24.5	A ² s
I _{GM}	Peak Gate Current	20 μs max.	4	А
P _{GM}	Peak Gate Dissipation	20 μs max.	3	W
P _{G(AV)}	Gate Dissipation	20ms max.	0.2	W
T _j	Operating Temperature		(-40 to +125)	°C
T _{stg}	Storage Temperature		(-40 to +150)	°C
T _{sld}	Soldering Temperature	10s max.	260	°C

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			D	М	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1 \text{ k}\Omega$	400	600	800	V

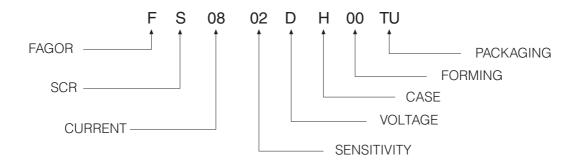
Revision: 1



Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS -		SENSITIVITY	· Unit
STIVIDOL	IAIIAIVILILII	CONDITIONS		02	Offit
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}$, $R_L = 140 \Omega$. $T_j = 25 ^{\circ}C$		200	μΑ
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}$, $R_L = 140 \Omega$, $T_j = 25 °C$	MAX	0.8	V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}$, $R_L = 3.3k\Omega$, $R_{GK} = 220\Omega$ $T_j = 125$ °C		0.1	V
V_{RGM}	Reverse Gate Voltage	$I_{RG} = 10\mu A$,	MIN	8	V
I _H	Holding Current	$I_T = 500 \text{ mA},$	MAX	5	mA
I _L	Latching Current	$I_G = 1.2 I_{GT}$	MAX	6	mA
dV / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}$, $R_{GK} = 1 \text{ k}\Omega$ $T_j = 125 ^{\circ}\text{C}$	MIN	5	V/µs
dl / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}$ tr \leq 100 ns, f = 60 Hz, $T_j = 125 ^{\circ}\text{C}$	MIN	50	A/µs
V_{TM}	On-state Voltage	at $I_T = 16$ Amp, tp = 380 µs, $T_j = 25$ °C	MAX	1.6	V
V _{t (o)}	Threshold Voltage	T _j = 125 °C	MAX	0.85	V
r _d	Dynamic resistance	T _j = 125 °C	MAX	46	m Ω
I _{DRM} / I _{RRM}		$V_D = V_{DRM}$, $R_{GK} = 1k\Omega$ $T_j = 125$ °C	MAX	1	mA
		$V_R = V_{RRM}$, $T_j = 25 ^{\circ}C$	MAX	5	μΑ
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC			1.3	°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC			60	°C/W

Part Number Information



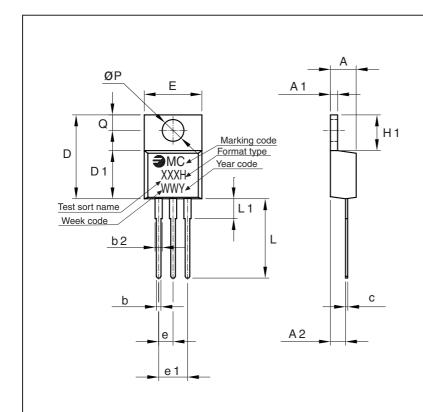
Revision: 1



Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FS0802DH 00TU	TU	TUBE	1000	2.30

Package Outline Dimensions: (mm) TO-220AB



	DIMENSIONS			
REF.	Milimeters			
	Min.	Max.		
А	4.47	4.67		
A1	1.17	1.37		
A2	2.52	2.82		
b	0.71	0.91		
b2	1.17	1.37		
С	0.31	0.53		
D	14.65	15.35		
D1	8.50	8.90		
Е	10.01	10.36		
е	2.51	2.57		
e1	4.98	5.18		
H1	6.15	6.45		
L	13.40	13.96		
L1	3.56	3.96		
Р	3.735	3.935		
Q	2.59	2.89		

Mounting Torque 0.8 N.m



Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum average power dissipation versus average on-state current.

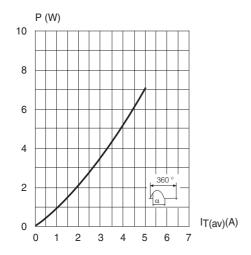


Fig. 3: Average and DC on-state current versus ambient temperature.

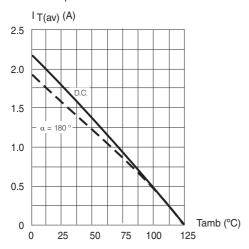


Fig. 5: Relative variation of gate trigger current, holding and latching current versus junction temperature.

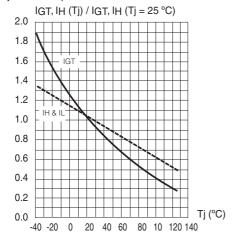


Fig. 2: Average and D.C. on-state current versus case temperature.

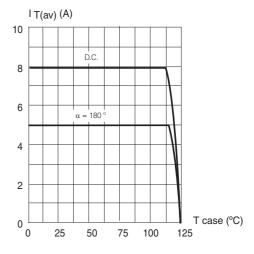


Fig. 4: Relative variation of thermal impedance junction to case versus pulse duration.

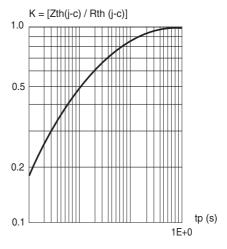


Fig. 6: Relative variation of holding current versus gate-cathode resistance (typical values).

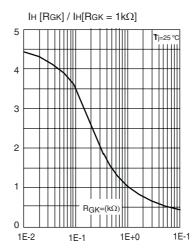




Fig.7: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

 $dV/dt [Rg\kappa] / dV/dt [Rg\kappa = 220\Omega]$

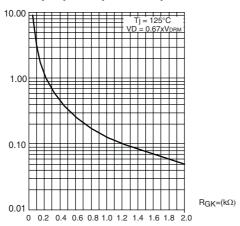


Fig. 8: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values).

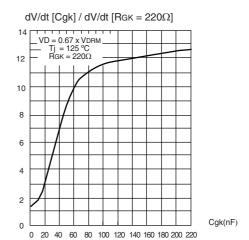


Fig. 9: Non repetitive surge peak on-state current versus number of cycles.

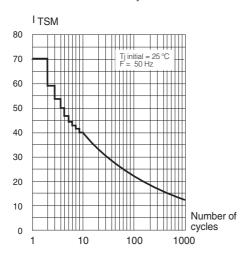


Fig. 10: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.

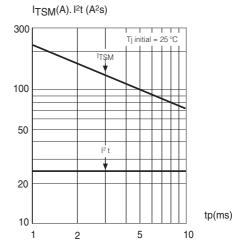
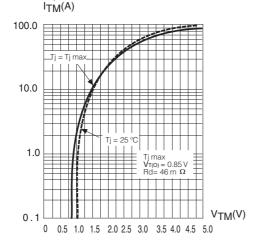


Fig. 11: On-state characteristics (maximum values).





Revision History

Date	Revision	Description of Changes
14-May-2013	0	Original Data Sheet
2-Apr-2014 1		200V and 700V eliminated & Fig. 3 Included

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All product, product specifications and data are subject to change without notice to improve reliability, function or design or otherwise.

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Revision: 1