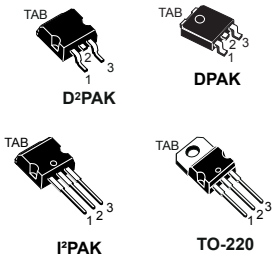
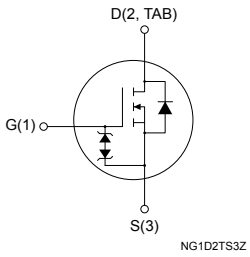
STB6N80K5, STD6N80K5
STI6N80K5, STP6N80K5

Datasheet

N-channel 800 V, 1.3 Ω typ., 4.5 A MDmesh K5 Power MOSFETs in D²PAK, DPAK, I²PAK and TO-220 packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB6N80K5	800 V	1.6 Ω	4.5 A	85 W
STD6N80K5				
STI6N80K5				
STP6N80K5				

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status links
STB6N80K5
STD6N80K5
STI6N80K5
STP6N80K5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.5	A
	Drain current (continuous) at T_C = 100 °C	2.8	
I_{DM} (1)	Drain current (pulsed)	18	A
P_{TOT}	Total power dissipation at T_C = 25 °C	85	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 4.5 A, di/dt=100 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value				
		D^2PAK	DPAK	I^2PAK	TO-220	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.47				°C/W
R_{thJA}	Thermal resistance, junction-to-ambient			62.50		
R_{thJB} (1)	Thermal resistance, junction-to-board	30	50			

1. *When mounted on an 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	1.5	A
E_{AS} (2)	Single pulse avalanche energy	85	mJ

1. *Pulse width limited by T_J max.*
2. *Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1.3	1.6	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	270	-	pF
C_{oss}	Output capacitance		-	25	-	
C_{rss}	Reverse transfer capacitance		-	0.7	-	
$C_{o(tr)}$ (1)	Equivalent output capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	38	-	pF
$C_{o(er)}$ (2)	Equivalent output capacitance energy related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	16	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7.5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 4.5 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	
Q_{gd}	Gate-drain charge		-	9.6	-	

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 2.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	7.5	-	
$t_{d(off)}$	Turn-off delay time		-	28.5	-	
t_f	Fall time		-	16	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		18	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 4.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	450		ns
Q_{rr}	Reverse recovery charge		-	3.15		µC
I_{RRM}	Reverse recovery current		-	14		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK, I²PAK and TO-220

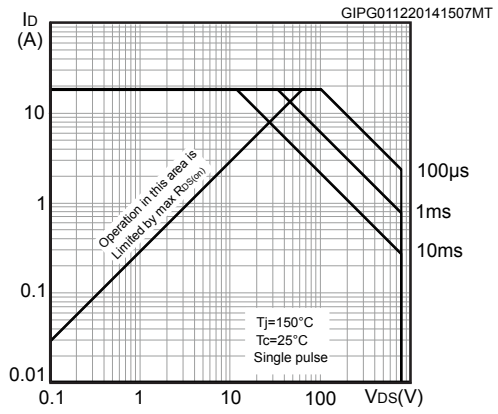


Figure 2. Normalized transient thermal impedance for D²PAK, I²PAK and TO-220

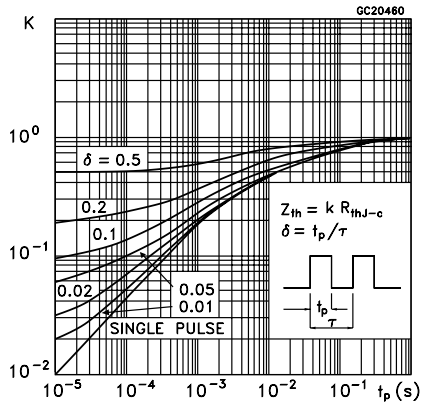


Figure 3. Safe operating area for DPAK

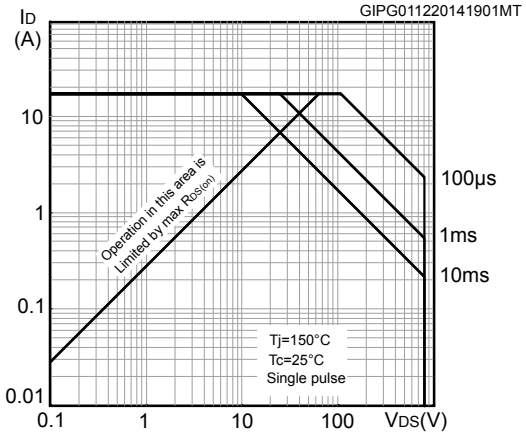


Figure 4. Normalized transient thermal impedance for DPAK

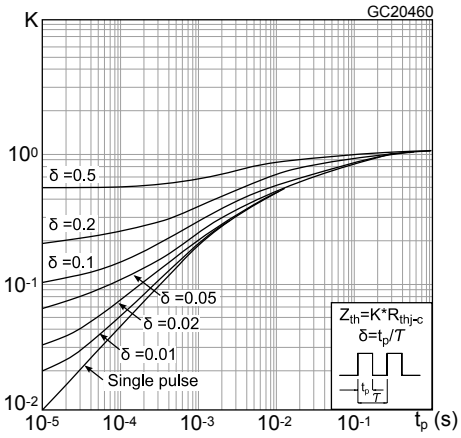


Figure 5. Typical output characteristics

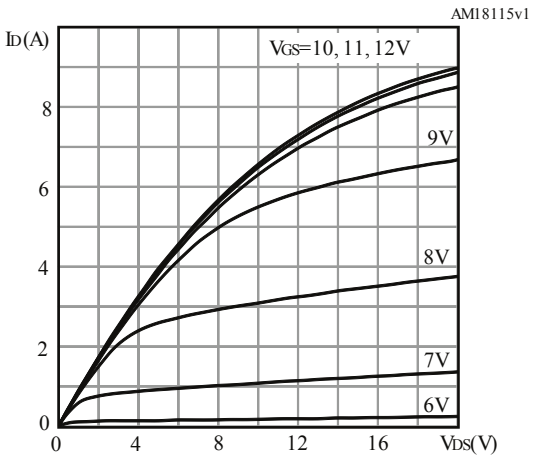


Figure 6. Typical transfer characteristics

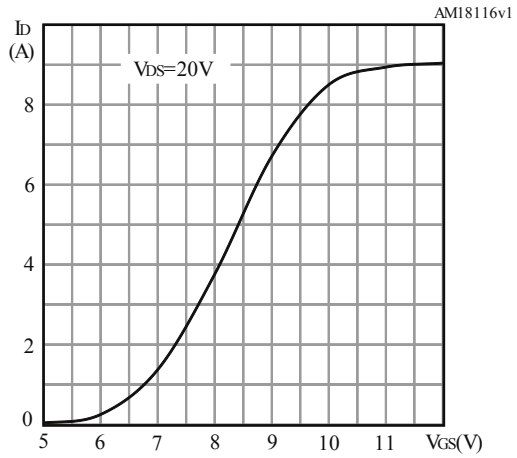


Figure 7. Typical gate charge characteristics

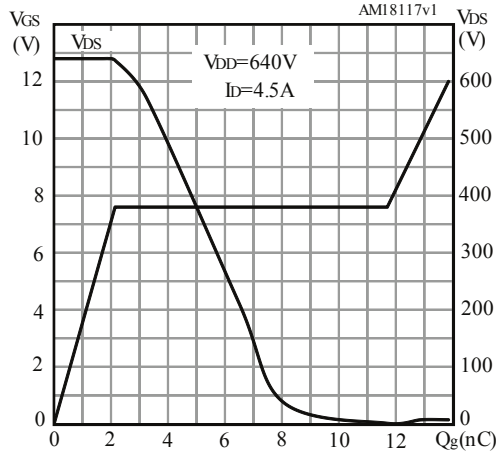


Figure 8. Typical drain-source on-resistance

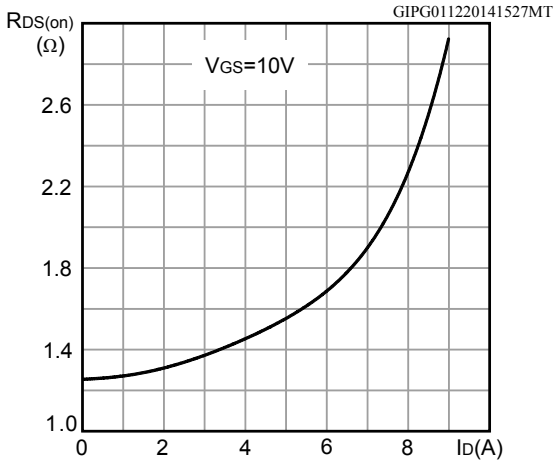


Figure 9. Typical capacitance characteristics

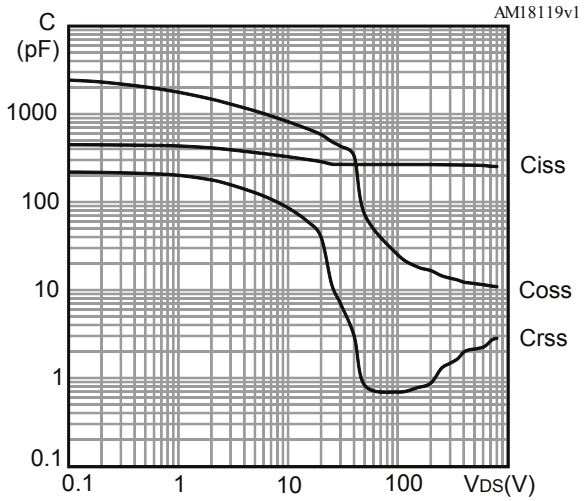


Figure 10. Normalized gate threshold vs temperature

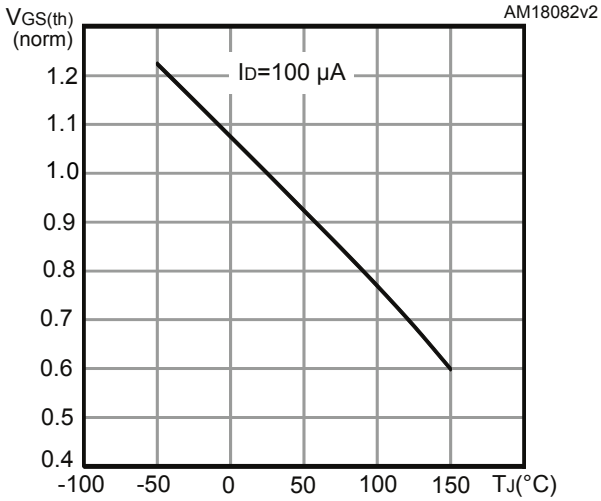


Figure 11. Normalized on-resistance vs temperature

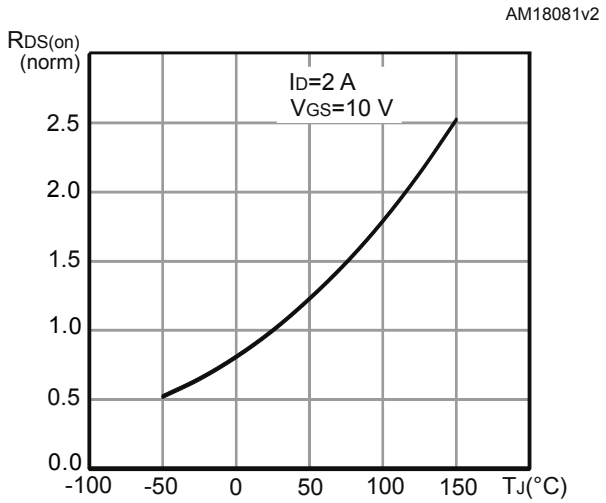


Figure 12. Normalized breakdown voltage vs temperature

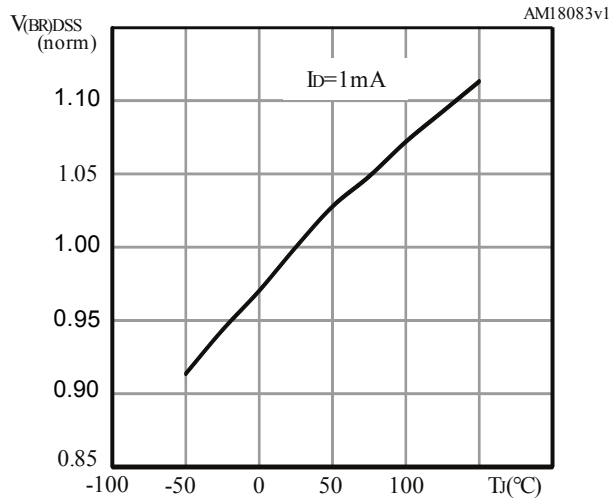


Figure 13. Typical output capacitance stored energy

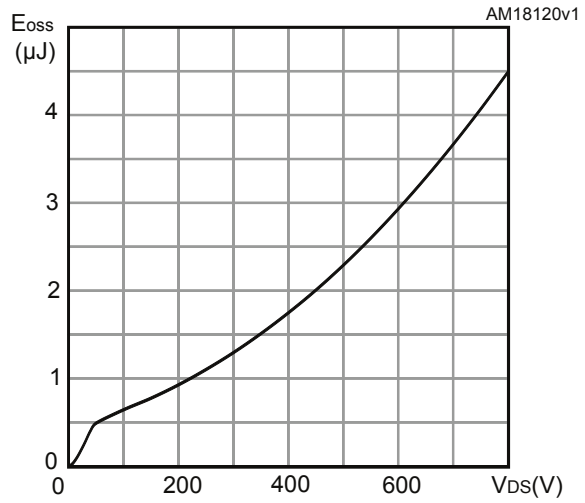
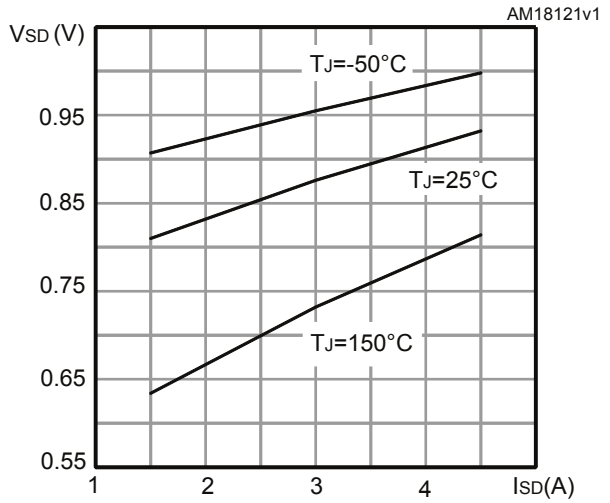


Figure 14. Typical reverse diode forward characteristics



3 Test circuits

Figure 15. Test circuit for resistive load switching times

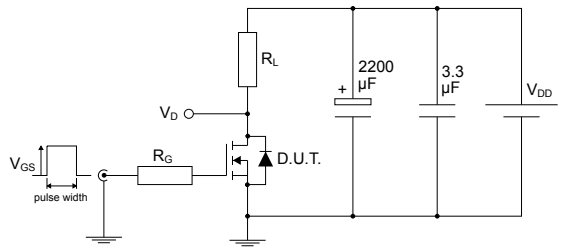


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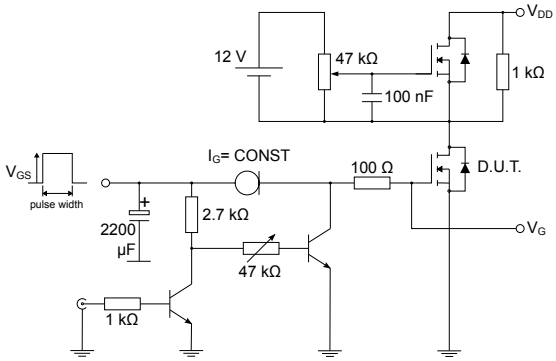
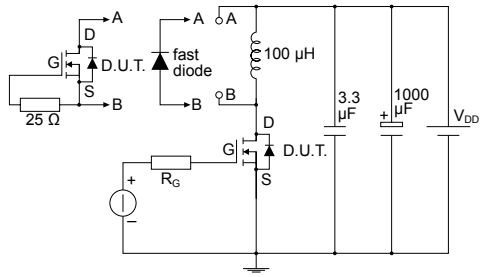
Figure 16. Test circuit for gate charge behavior



AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 18. Unclamped inductive load test circuit

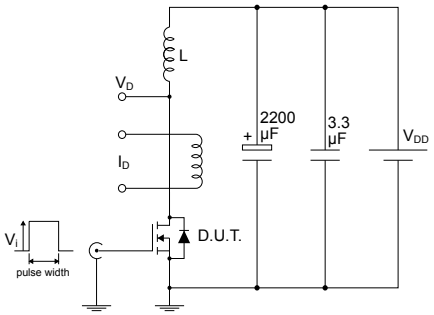


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Figure 19. Unclamped inductive waveform

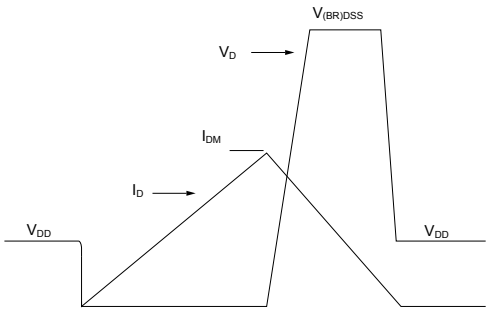

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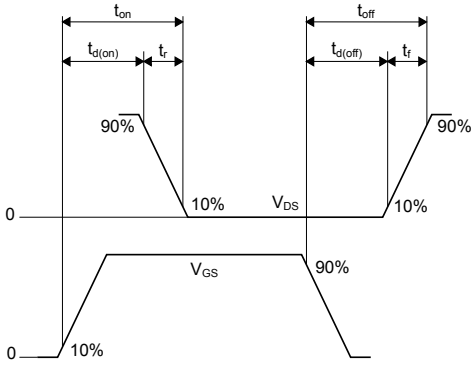
Figure 20. Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. **D²PAK (TO-263) type A package outline**

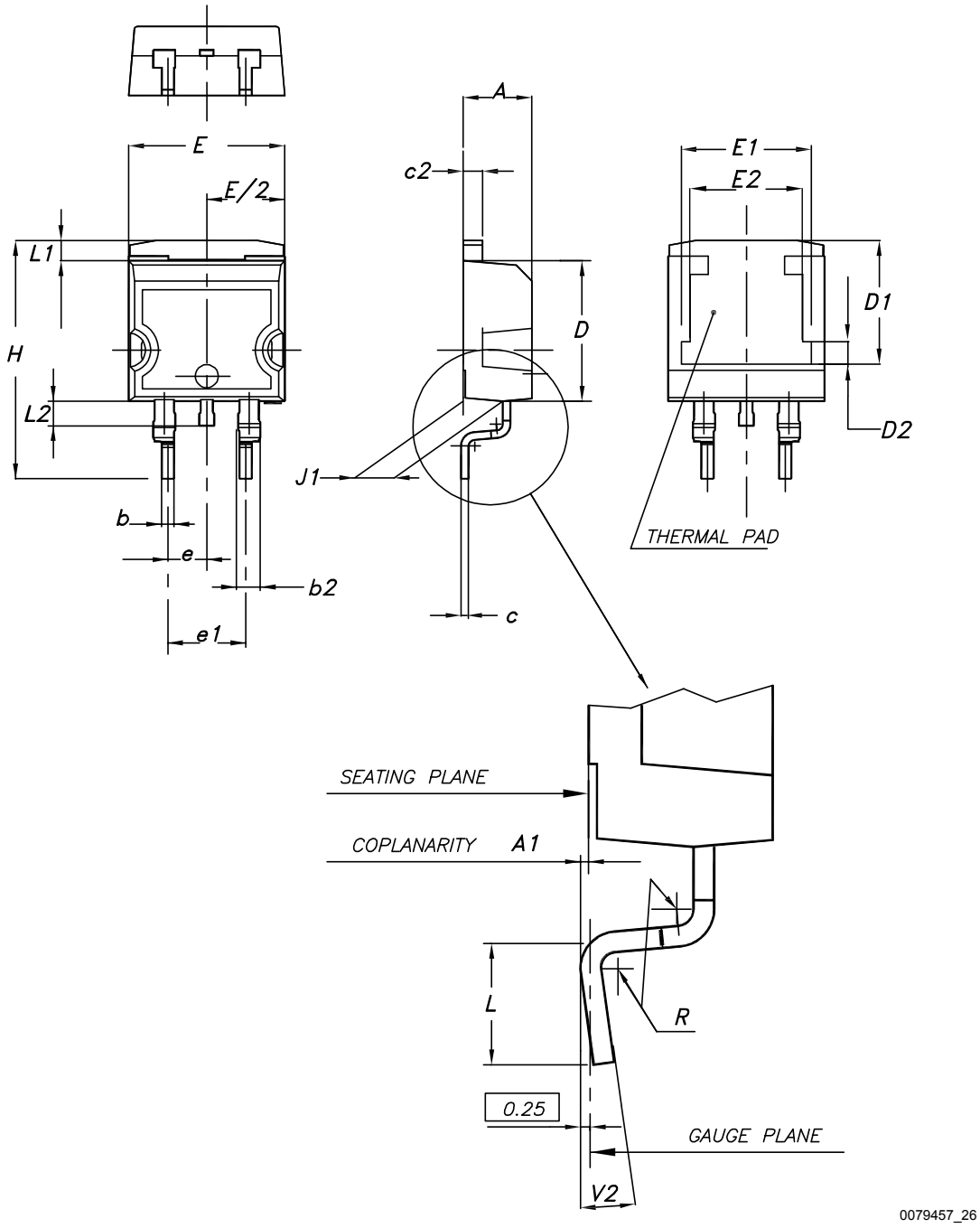


Table 9. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

Figure 22. D²PAK (TO-263) type B package outline

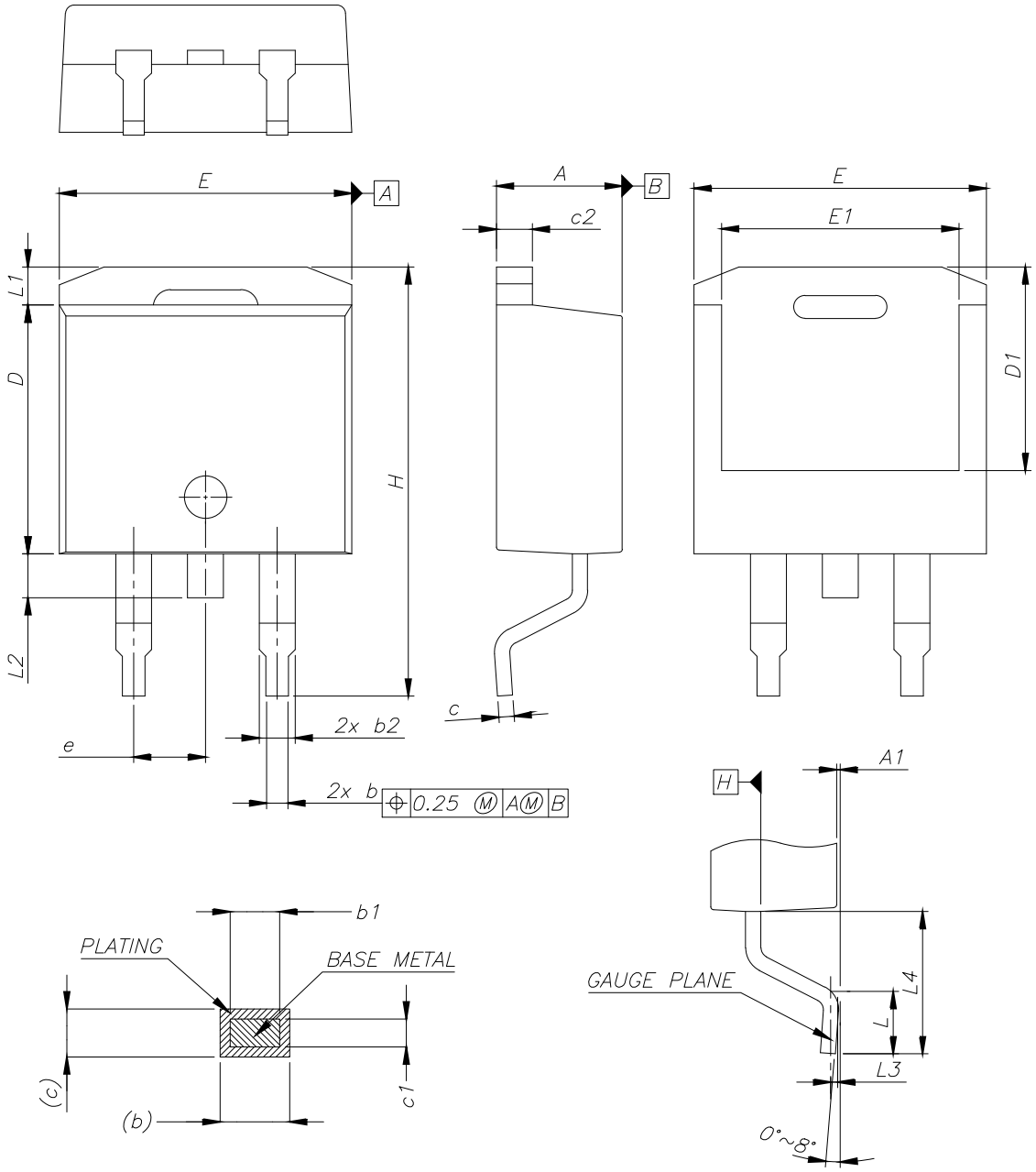


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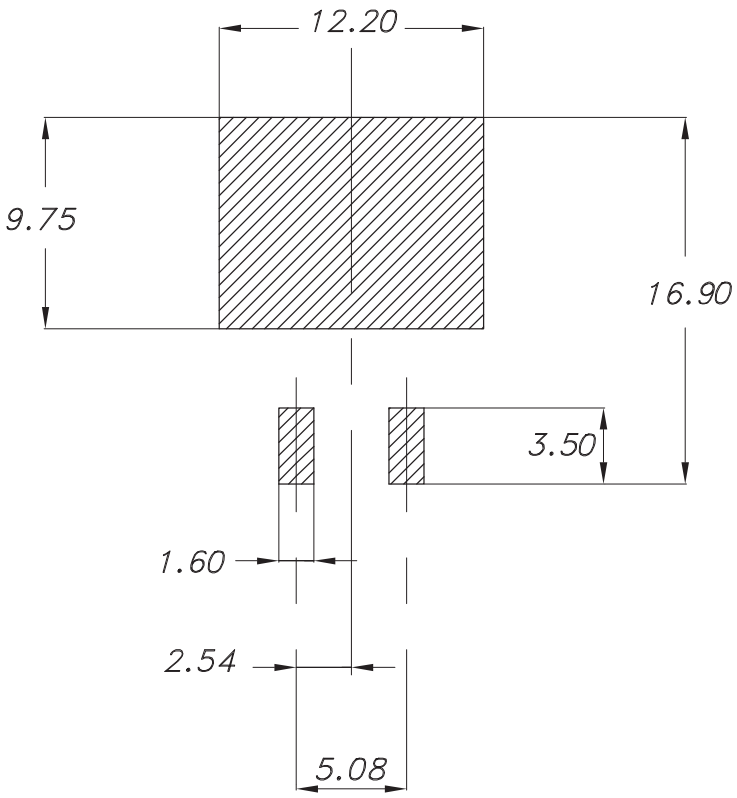
Table 10. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e		2.54 BSC	
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 23. **D²PAK (TO-263) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) type A2 package information

Figure 24. DPAK (TO-252) type A2 package outline

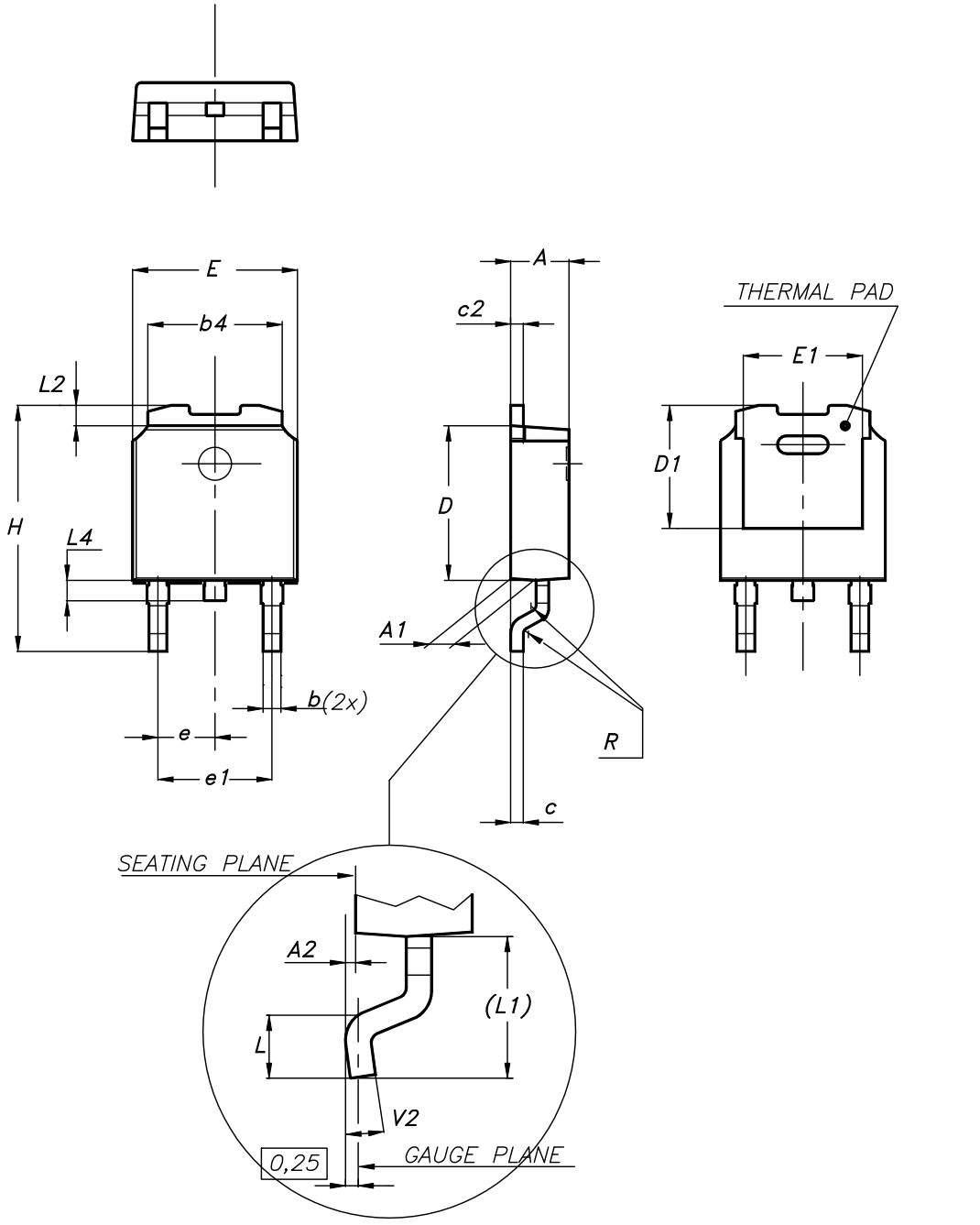
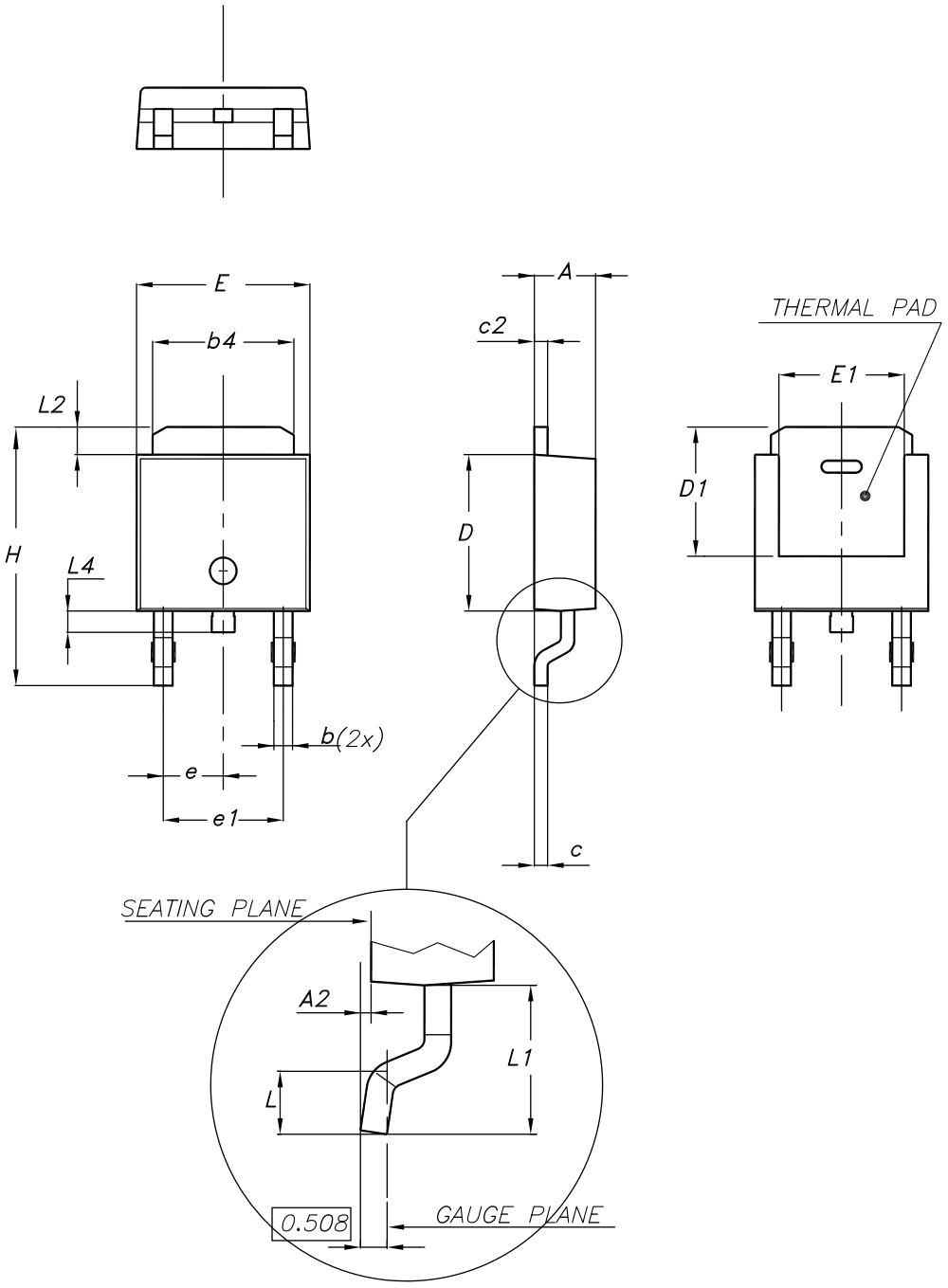


Table 11. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.4 DPAK (TO-252) type E package information

Figure 25. **DPAK (TO-252) type E package outline**

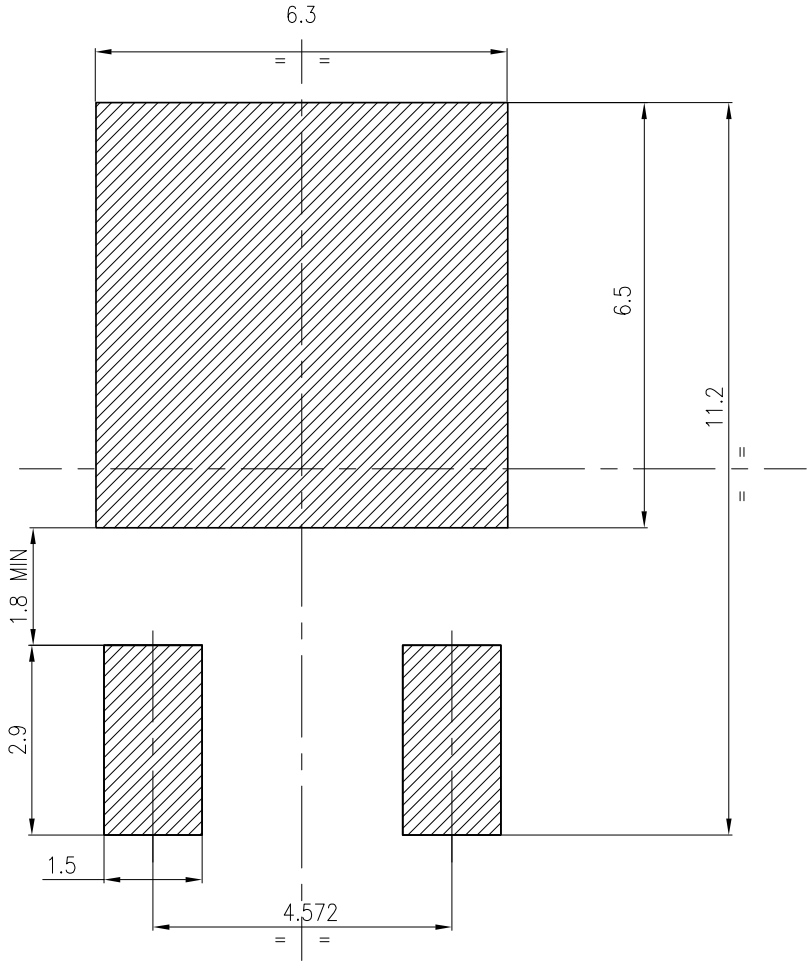


0068772_typeE_rev.30

Table 12. **DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 26. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



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4.5 I²PAK package information

Figure 27. I²PAK package outline

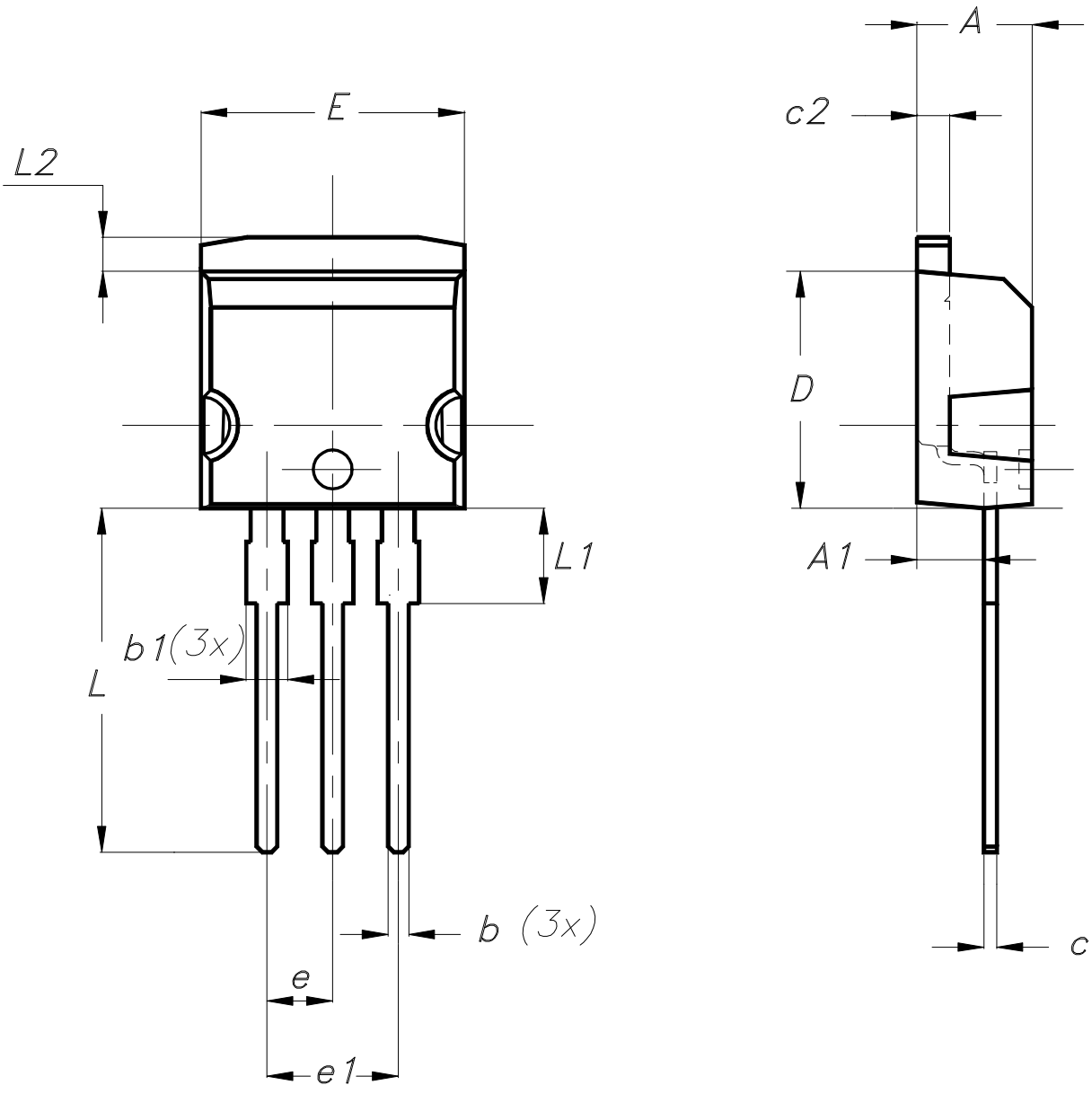

Table 13. **I²PAK package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10.00	-	10.40
L	13.00	-	14.00
L1	3.50	-	3.93
L2	1.27	-	1.40

4.6 TO-220 type A package information

Figure 28. **TO-220 type A package outline**

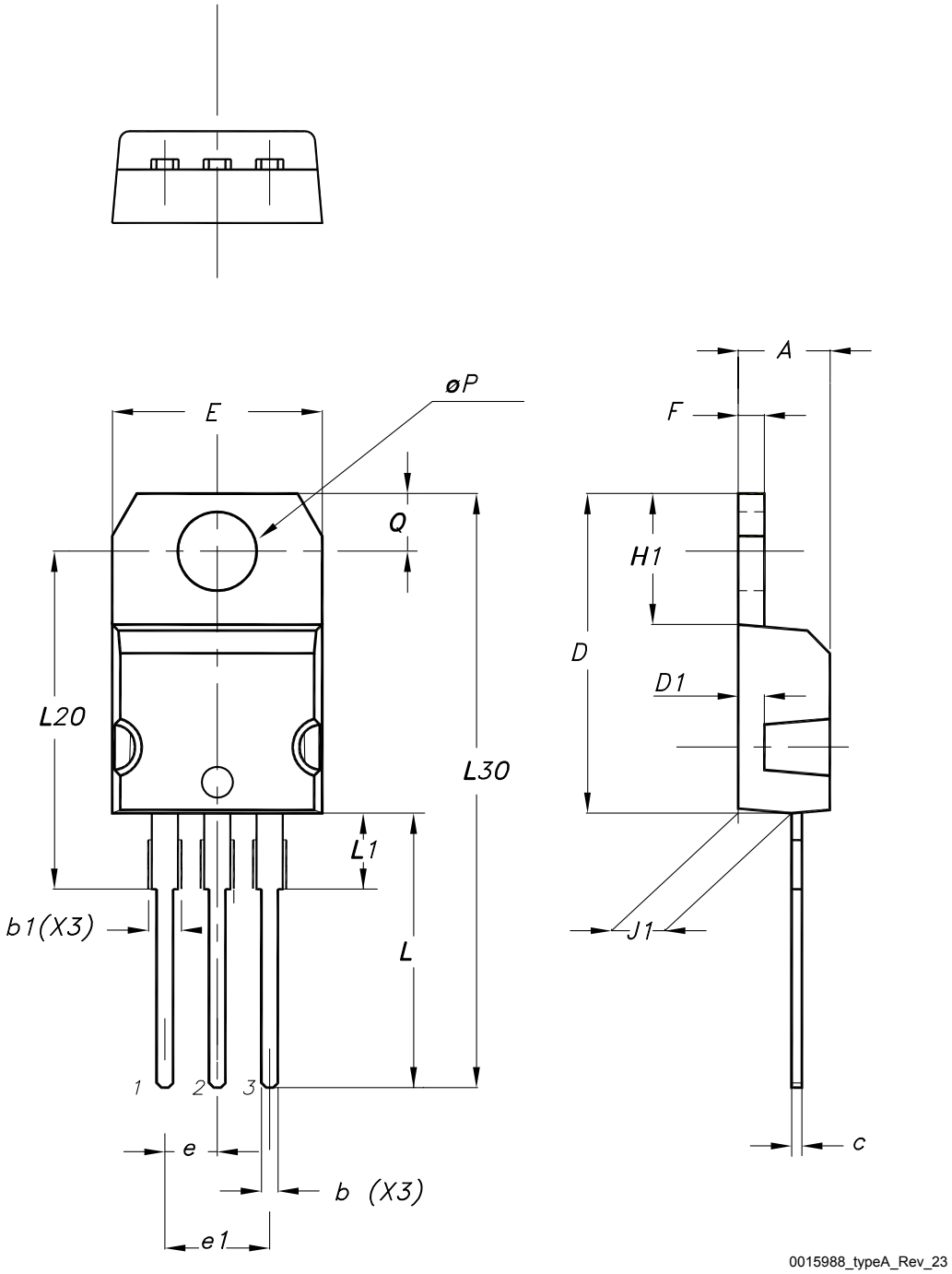

Table 14. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.7 D²PAK type A packing information

Figure 29. D²PAK tape outline

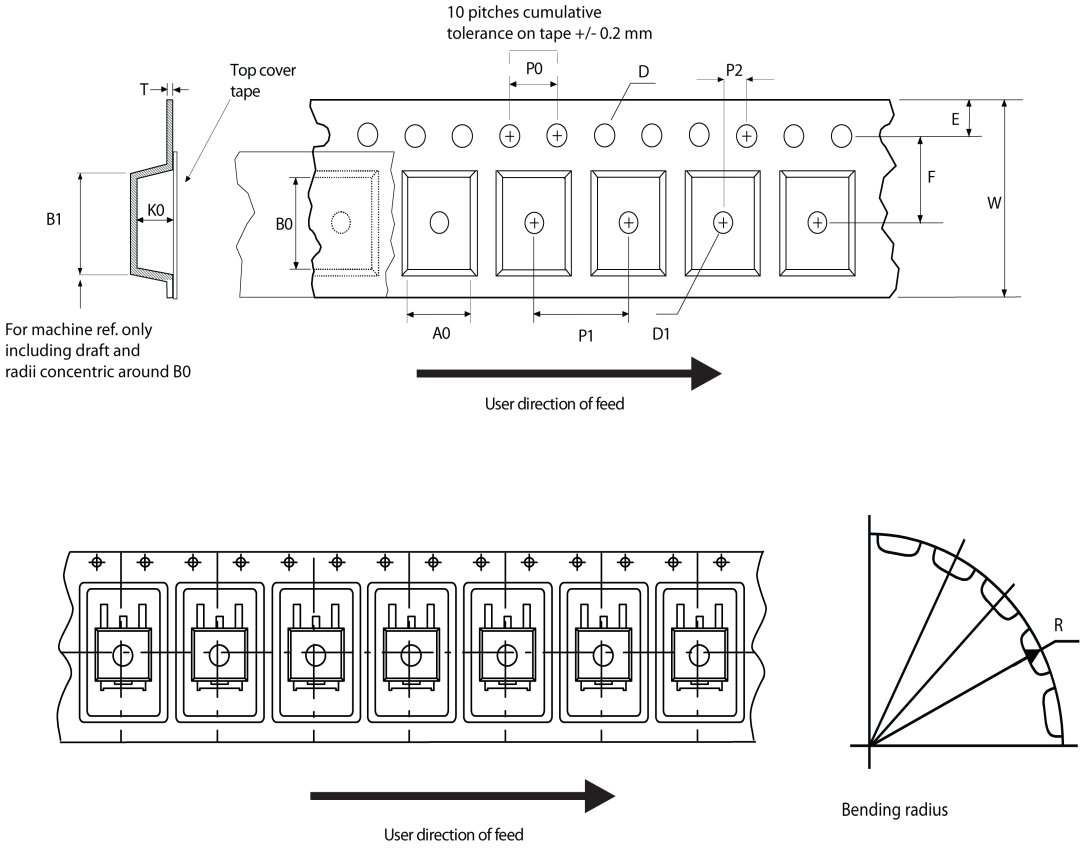

Figure 30. **D²PAK reel outline**

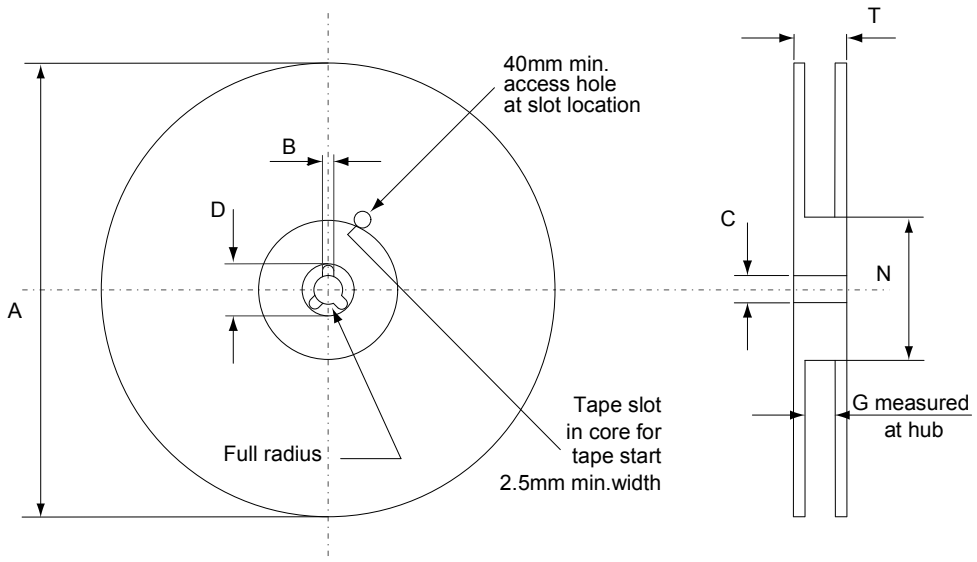

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Table 15. **D²PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.8 D²PAK type B packing information

Figure 31. D²PAK type B tape outline

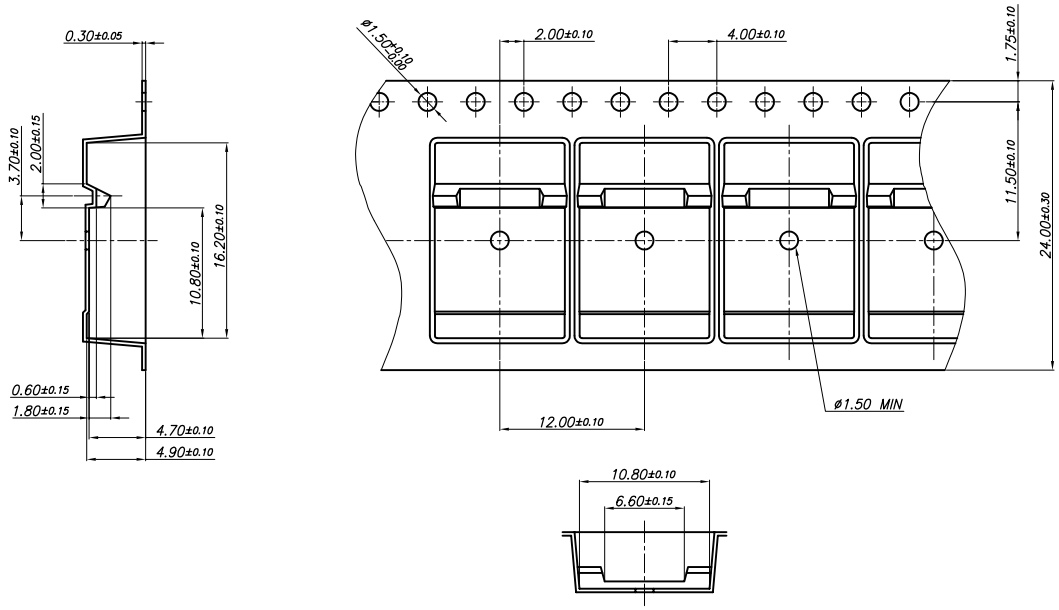

Figure 32. D²PAK type B reel outline

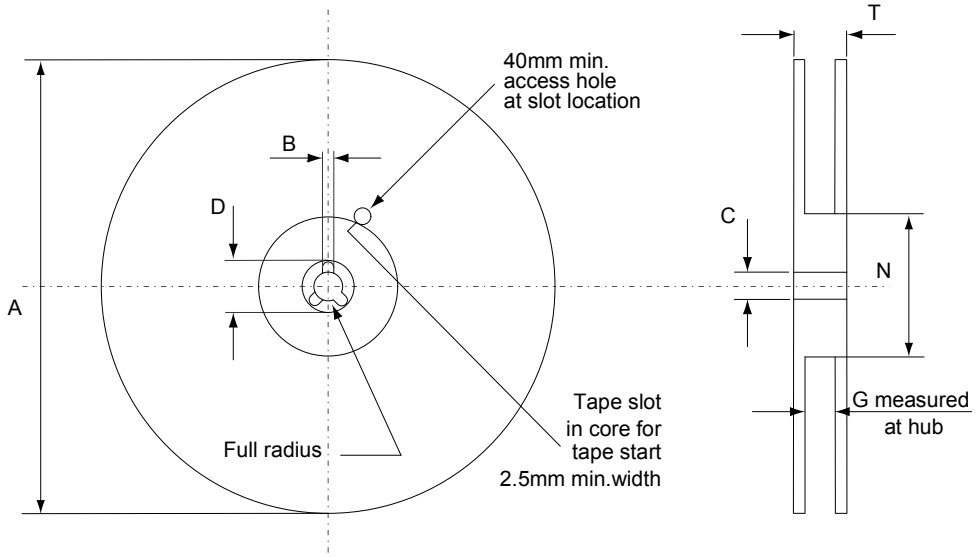

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Table 16. D²PAK type B reel mechanical data

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

4.9 DPAK (TO-252) packing information

Figure 33. DPAK (TO-252) tape outline

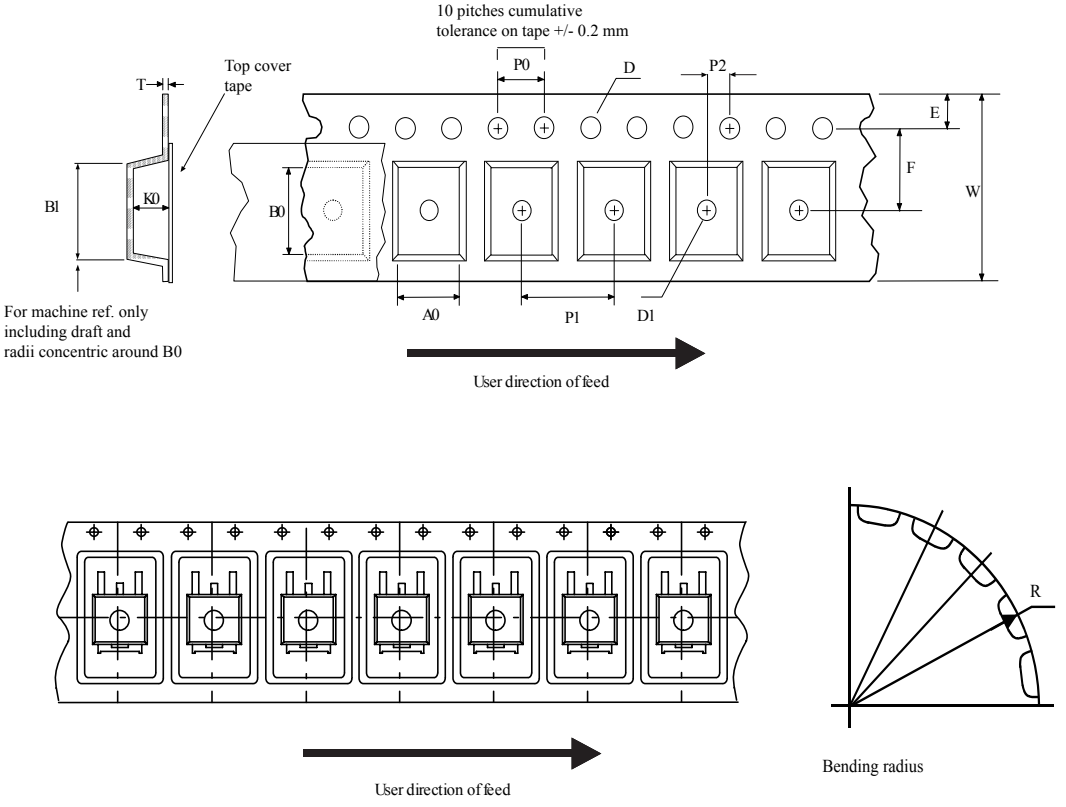

Figure 34. **DPAK (TO-252) reel outline**

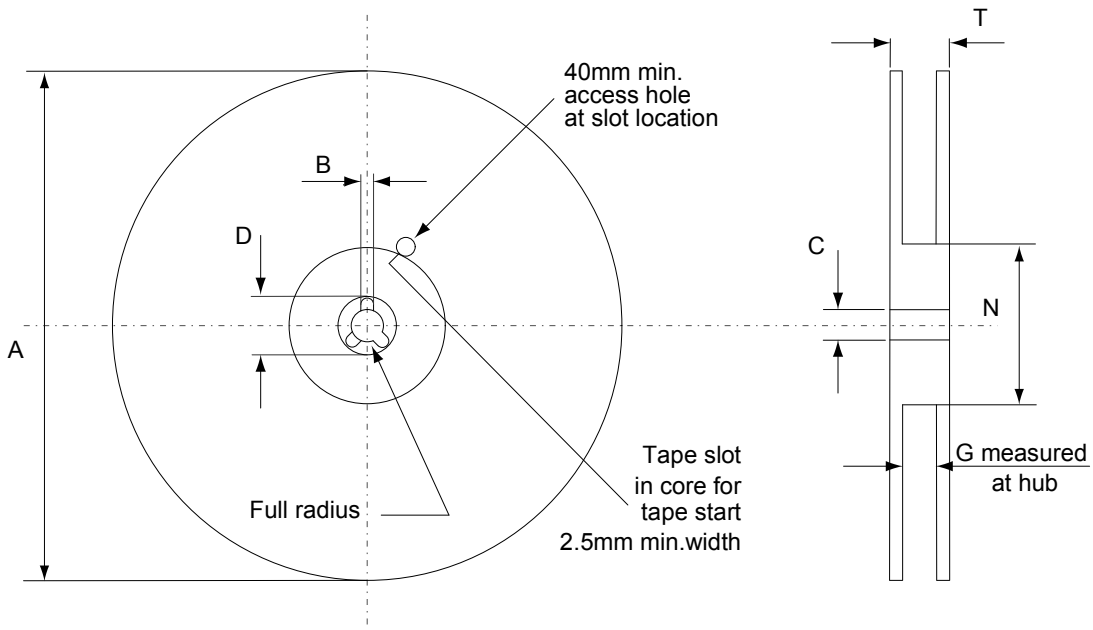

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Table 17. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Ordering information

Table 18. **Order codes**

Order codes	Marking	Package	Packing
STB6N80K5	6N80K5	D²PAK	Tape and reel
STD6N80K5		DPAK	
STI6N80K5		I²PAK	Tube
STP6N80K5		TO-220	

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
28-May-2013	1	First release.
05-Dec-2014	2	Updated title, features and description in cover page. Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package information.* Minor text changes.
27-Mar-2015	3	Updated *Section 4: Package information.* Minor text changes.
10-Dec-2021	4	Updated Section 4 Package information. Minor text changes.

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