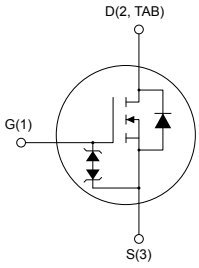
N-channel 400 V, 1.45 Ω typ., 3 A SuperMESH™ Power MOSFETs in IPAK and DPAK packages

IPAK

DPAK



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	P_{TOT}	Package
STD5NK40Z-1	400 V	1.80 Ω	45 W	IPAK
STD5NK40ZT4				DPAK

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STD5NK40Z-1
STD5NK40ZT4

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	3	A
I_D	Drain current (continuous) at T_C = 100 °C	1.9	A
I_{DM} (1)	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	2.8	kV
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 3 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

SymbolParameter		Value		Unit
		IPAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.78		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb		50	°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	130	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	400			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 400 V			1	µA
		V_{GS} = 0 V, V_{DS} = 400 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.5 A		1.45	1.80	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	305		pF
C_{oss}	Output capacitance			57		
C_{rss}	Reverse transfer capacitance			11.5		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 V to 320 V	-	44		
Q_g	Total gate charge	V_{DD} = 320 V, I_D = 3 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	11.7	17	nC
Q_{gs}	Gate-source charge			2.8		
Q_{gd}	Gate-drain charge			5.8		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS}increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	9.2	-	ns
t_r	Rise time			6		
$t_{d(off)}$	Turn-off delay time			22.5		
t_f	Fall time			11		
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 320 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)		8.5		
t_f	Fall time			7.5		
t_c	Cross-over time			14.5		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
I_{SDM} (1)	Source-drain current (pulsed)		-		12	
V_{SD} (2)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3 A, di/dt = 100 A/µs	-	145		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 40 V, T_j = 150 °C	-	464		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	6.4		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

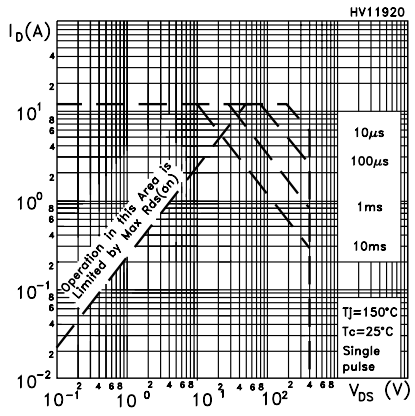


Figure 2. Thermal impedance

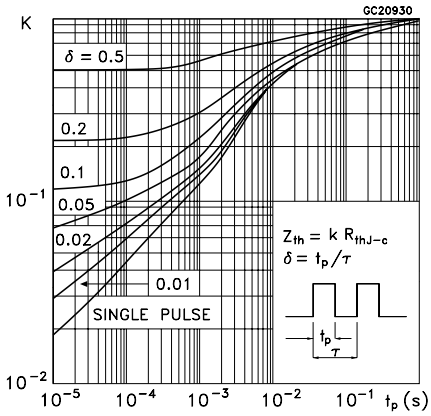


Figure 3. Output characterisics

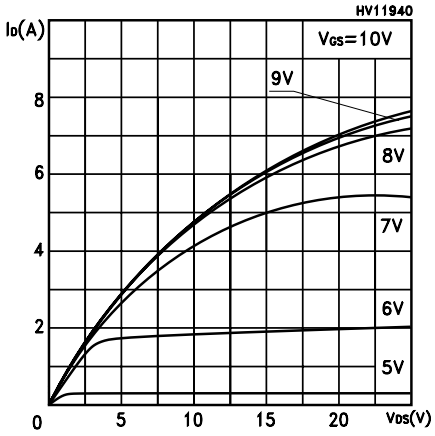


Figure 4. Transfer characteristics

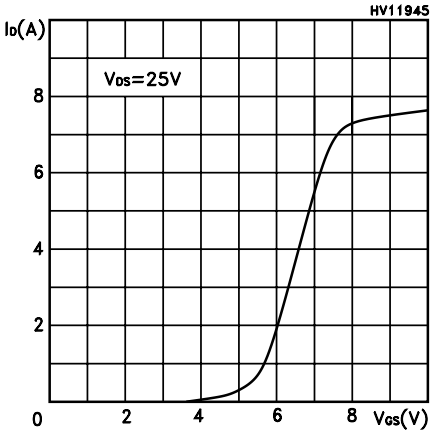


Figure 5. Capacitance variations

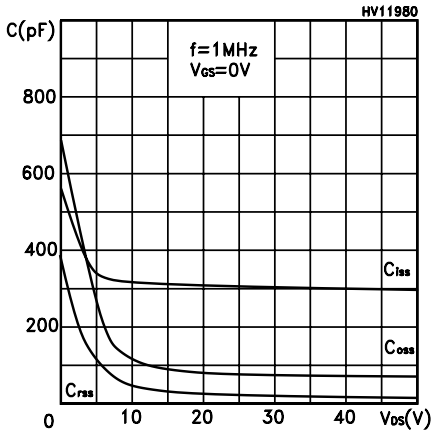


Figure 6. Gate charge vs gate-source voltage

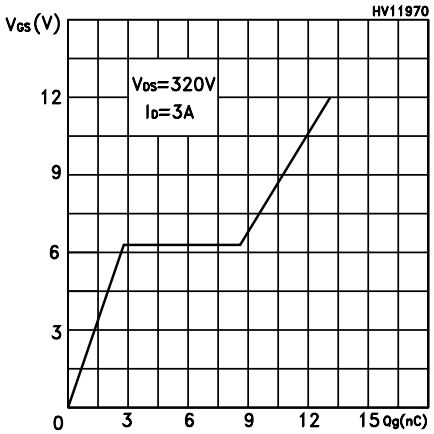


Figure 7. Normalized gate threshold voltage vs temperature

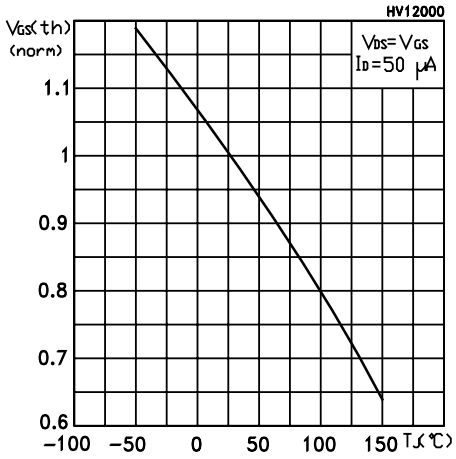


Figure 8. Static drain-source on resistance

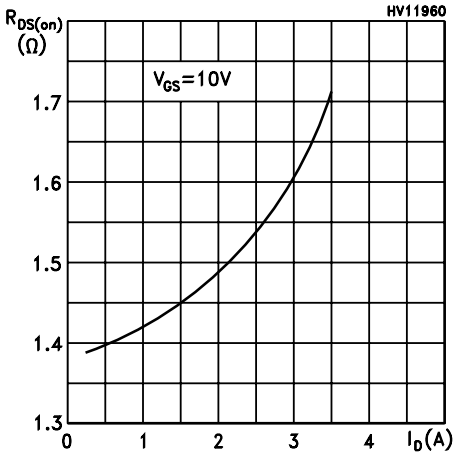


Figure 9. Source-drain diode forward characteristic

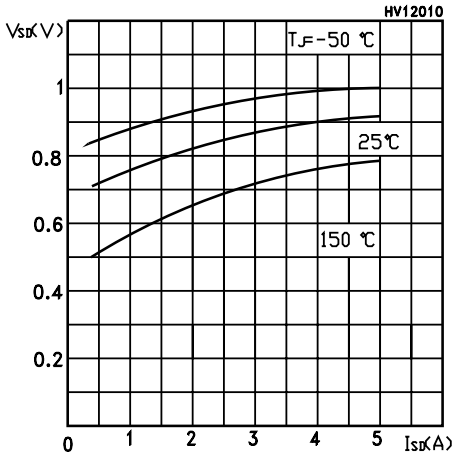


Figure 10. Maximum avalanche energy vs temperature

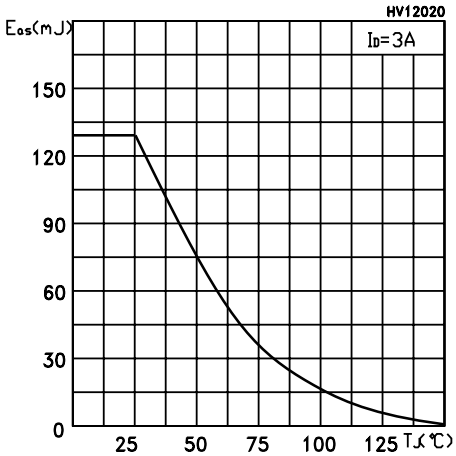


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

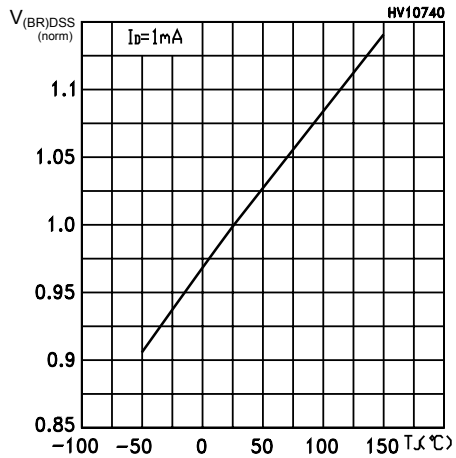
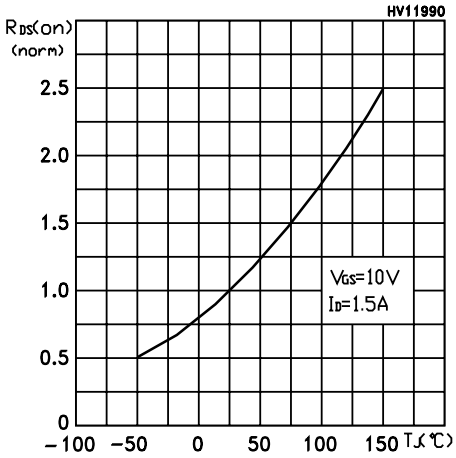


Figure 12. Normalized on resistance vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

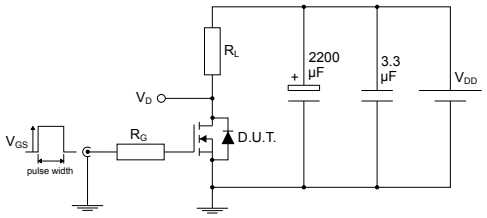


Figure 14. Test circuit for gate charge behavior

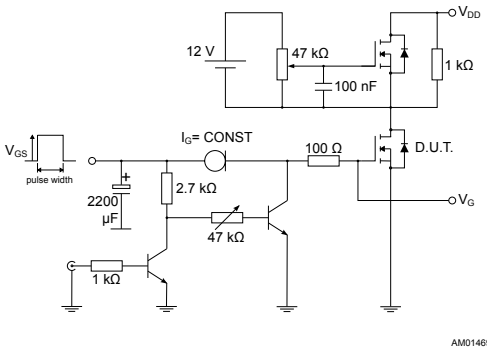


Figure 15. Test circuit for inductive load switching and diode recovery times

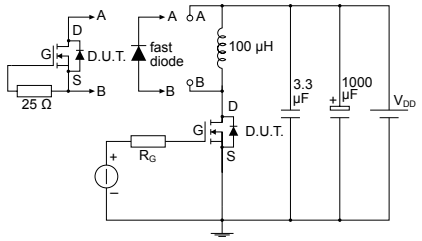


Figure 16. Unclamped inductive load test circuit

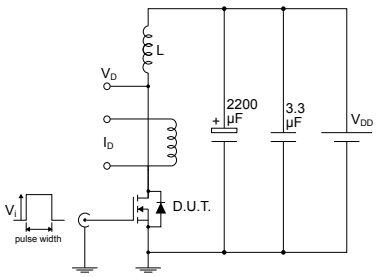


Figure 17. Unclamped inductive waveform

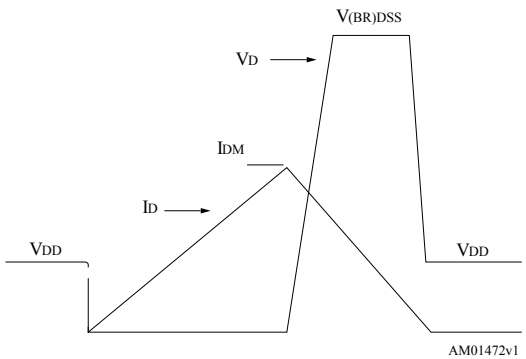
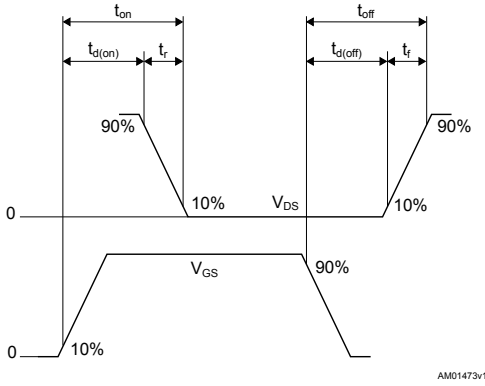


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 IPAK (TO-251) type A package information

Figure 19. **IPAK (TO-251) type A package outline**

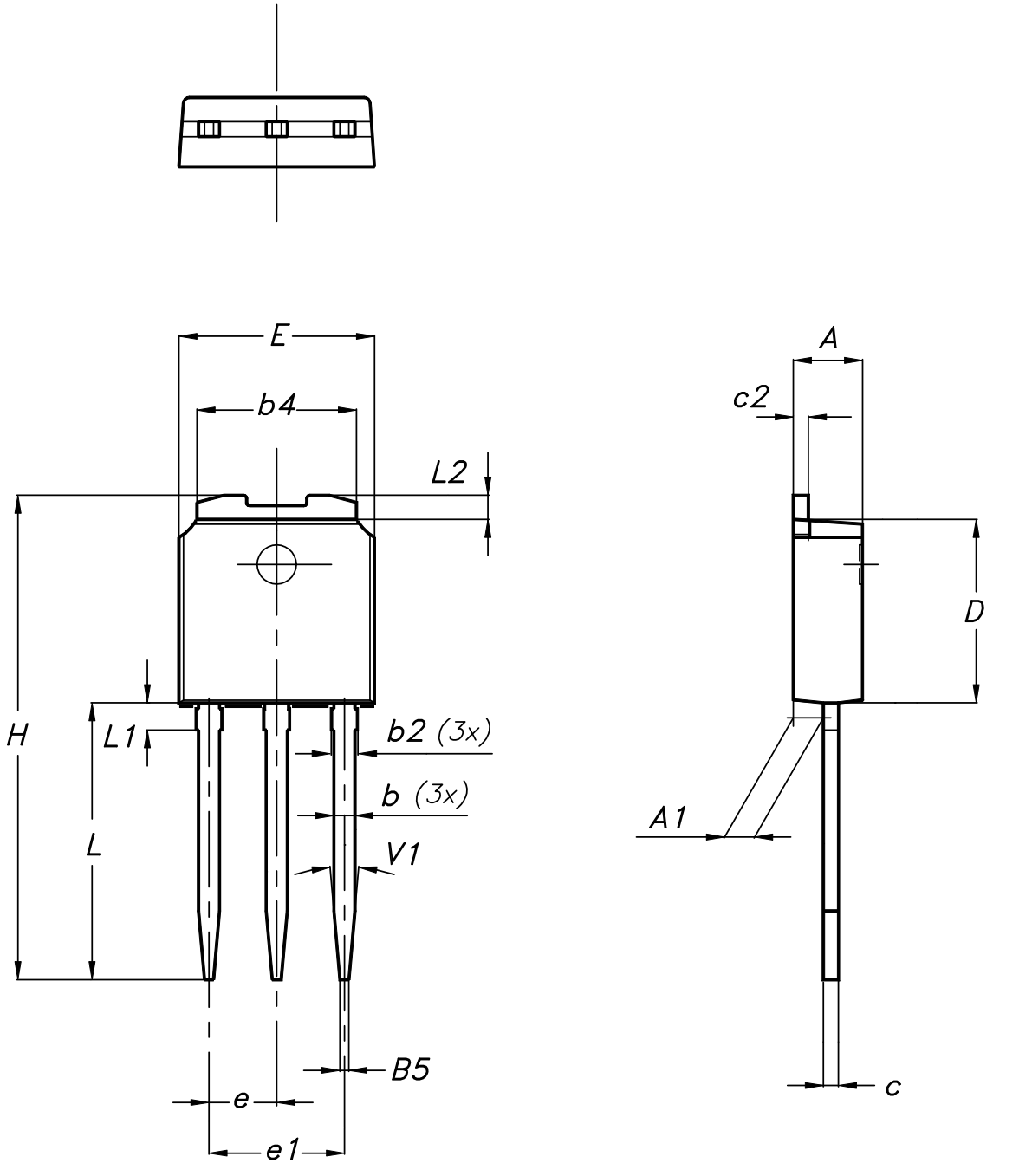


Table 9. **IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.2 IPAK (TO-251) type C package information

Figure 20. **IPAK (TO-251) type C package outline**

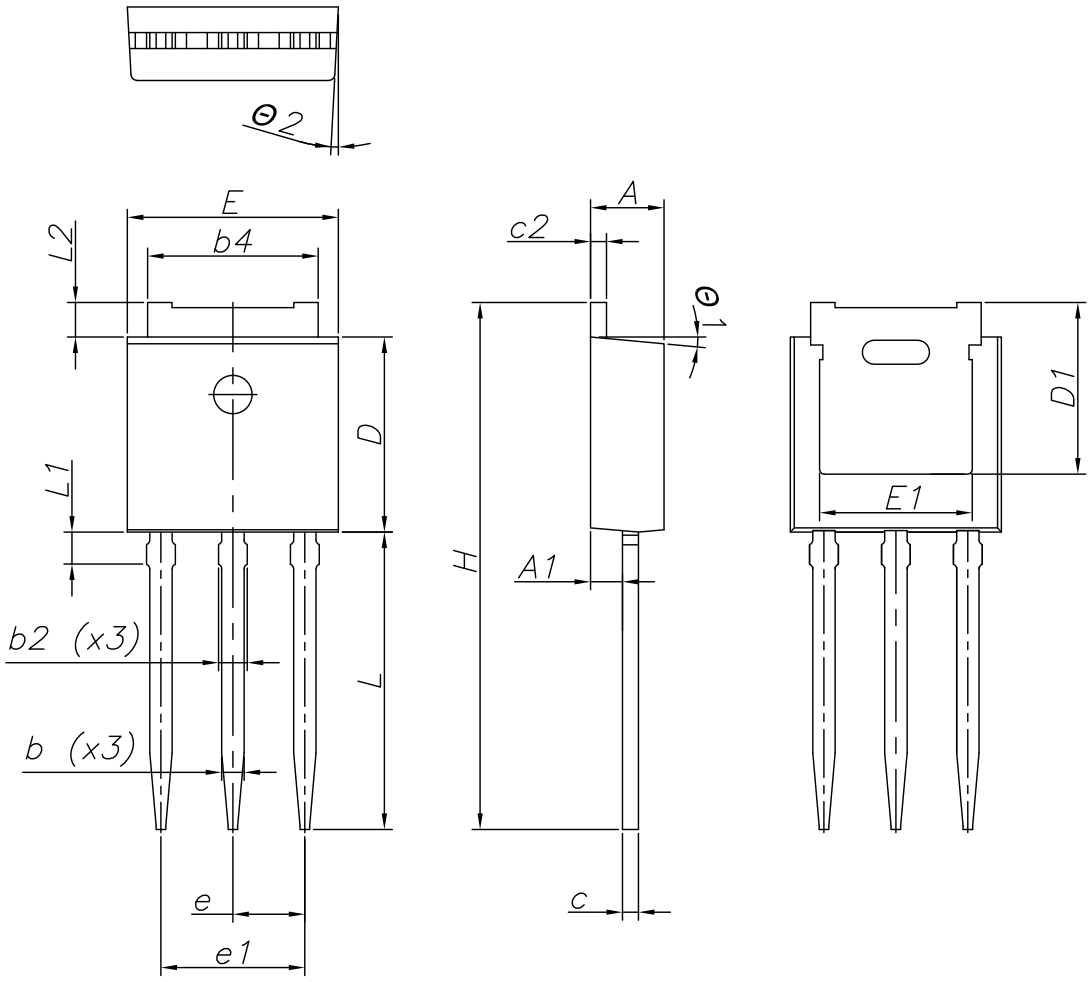


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Table 10. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

4.3 DPAK (TO-252) type A package information

Figure 21. **DPAK (TO-252) type A package outline**

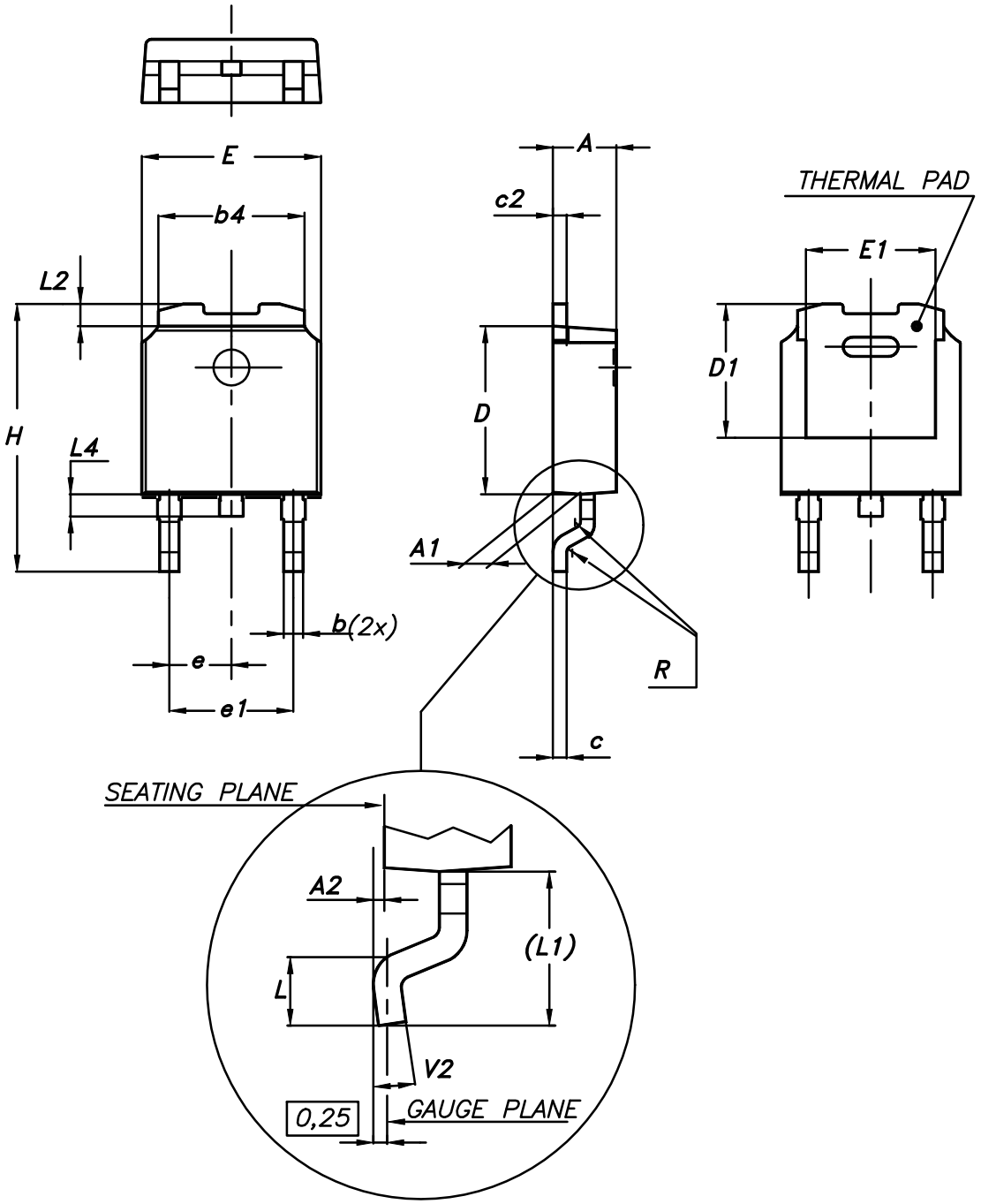

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Table 11. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.4 DPAK (TO-252) type C package information

Figure 22. **DPAK (TO-252) type C package outline**

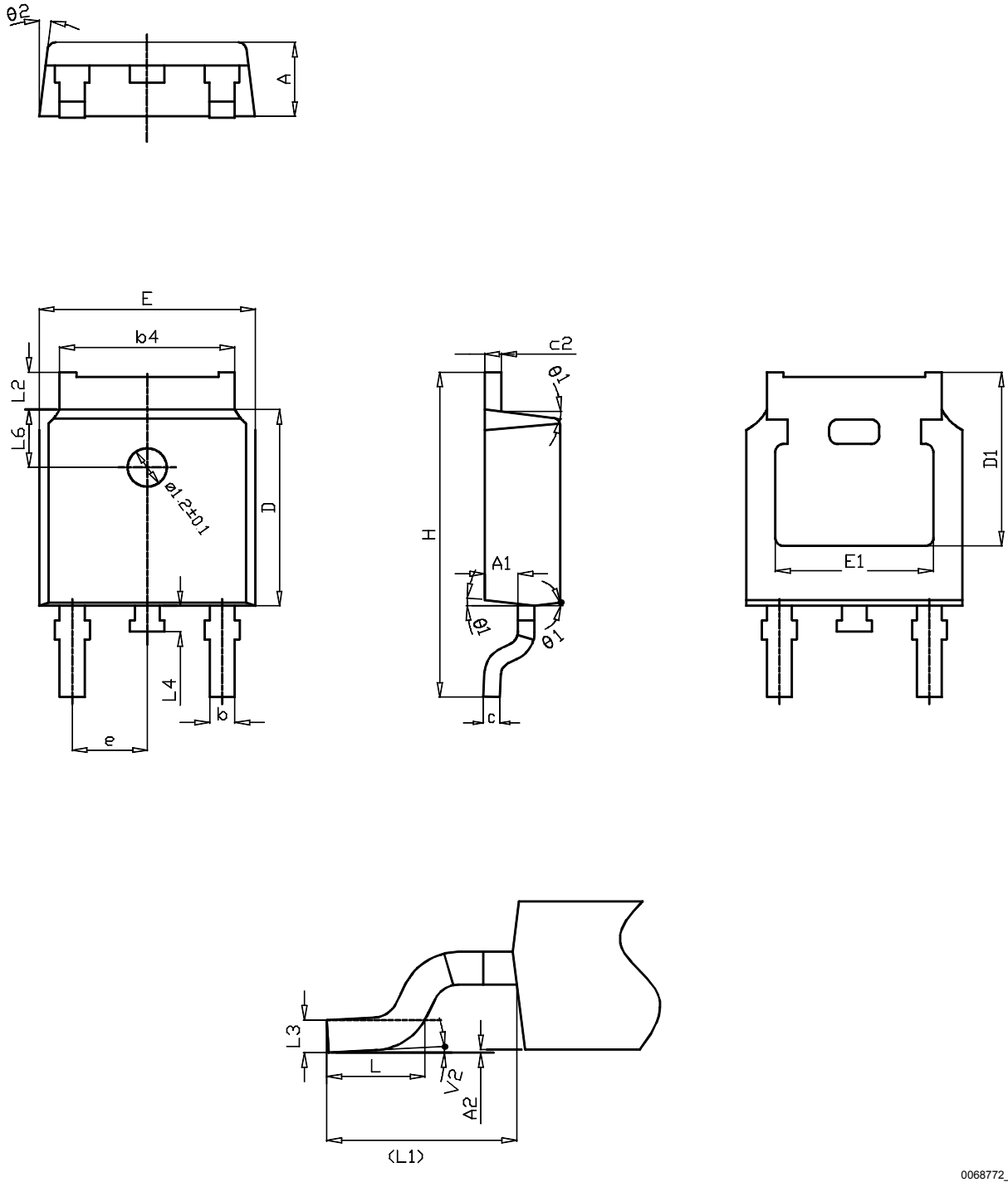

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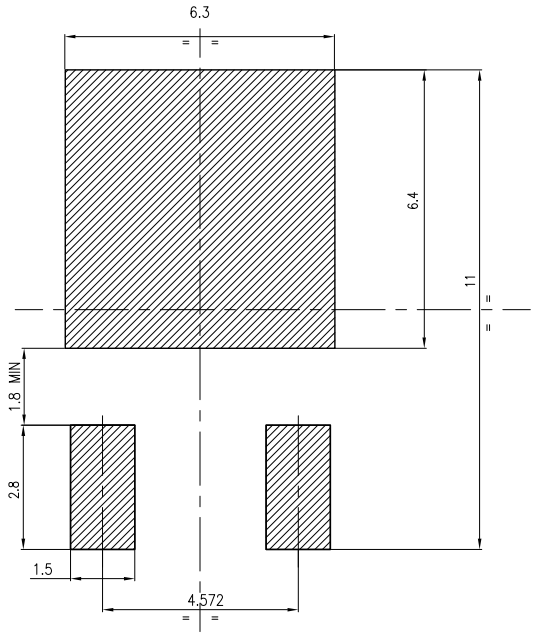
Table 12. **DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



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4.5 DPAK (TO-252) packing information

Figure 24. **DPAK (TO-252) tape outline**

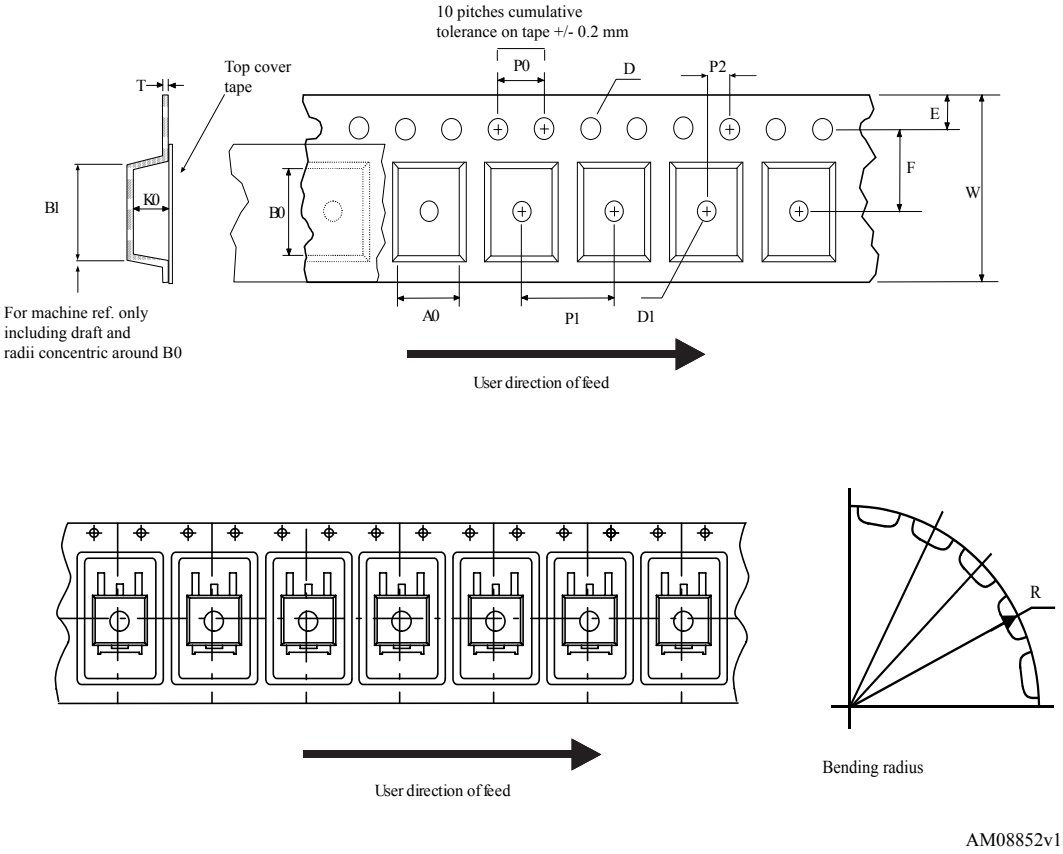

Figure 25. **DPAK (TO-252) reel outline**

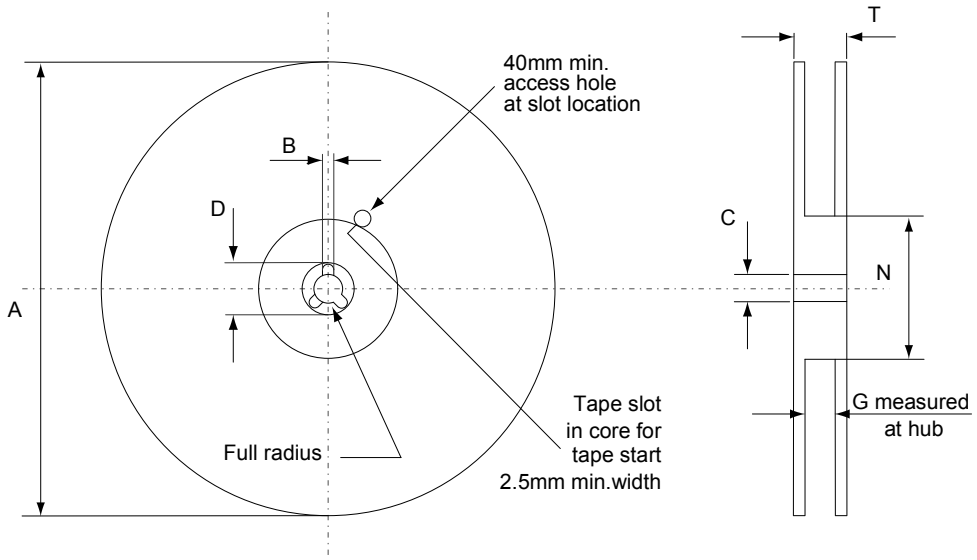

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Table 13. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Ordering information

Table 14. **Order codes**

Order code	Marking	Package	Packing
STD5NK40Z-1	D5NK40Z	IPAK	Tube
STD5NK40ZT4		DPAK	Tape and reel

Revision history

Table 15. **Document revision history**

Date	Version	Changes
11-Sep-2018	4	The part numbers STP5NK40Z and STP5NK40ZFP have been moved to a separate datasheet. Updated Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.

Contents