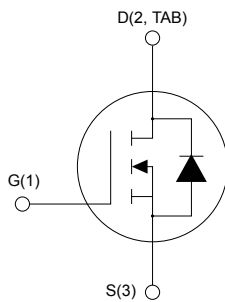
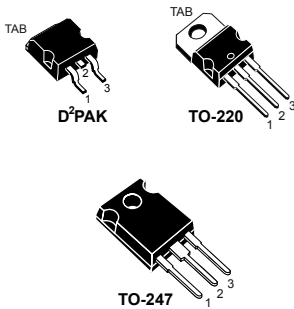




N-channel 650 V, 90 mΩ typ., 28 A MDmesh M5 Power MOSFETs in a D²PAK, TO-220 and TO-247 packages



AM01475v1_noZen



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB34N65M5	650 V	110 mΩ	28 A
STP34N65M5			
STW34N65M5			

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low R_{DS(on)}
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links

[STB34N65M5](#)

[STP34N65M5](#)

[STW34N65M5](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	28	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	17.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	112	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Maximum operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 28\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DD} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.66			$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	62.5	50	$^\circ\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	510	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$	-	-	100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$	-	90	110	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2700	-	pF
C_{oss}	Output capacitance		-	75	-	
C_{rSS}	Reverse transfer capacitance		-	6.3	-	
$C_{o(tr)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	220	-	pF
$C_{o(er)}^{(2)}$	Equivalent output capacitance energy related		-	63	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	1.95	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 14\text{ A}$,	-	62.5	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	17	-	
Q_{gd}	Gate-drain charge	(see the Figure 17. Test circuit for gate charge behavior)	-	28	-	

1. $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

2. $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 18\text{ A}$,	-	59	-	ns
$t_{r(v)}$	Voltage rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8.7	-	
$t_{c(off)}$	Crossing time off	(see the Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	12	-	
$t_{f(i)}$	Current fall time		-	7.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	28	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	112	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 28 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	350	-	ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ (see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	5.6	-	μC
I_{RRM}	Reverse recovery current		-	32	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 28 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	422	-	ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	7.4	-	μC
I_{RRM}	Reverse recovery current		-	35	-	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

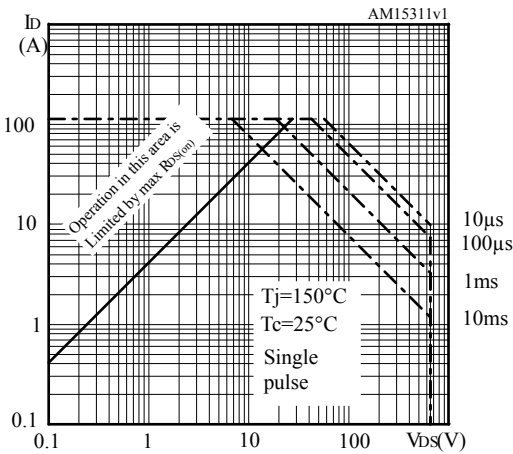
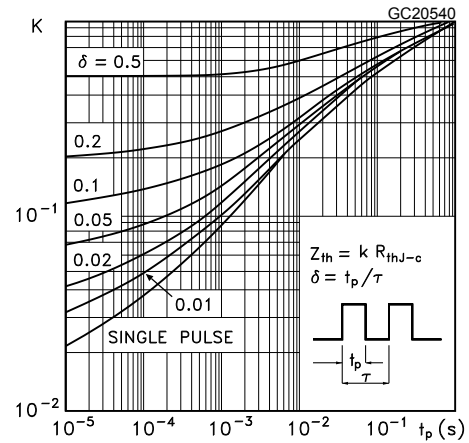
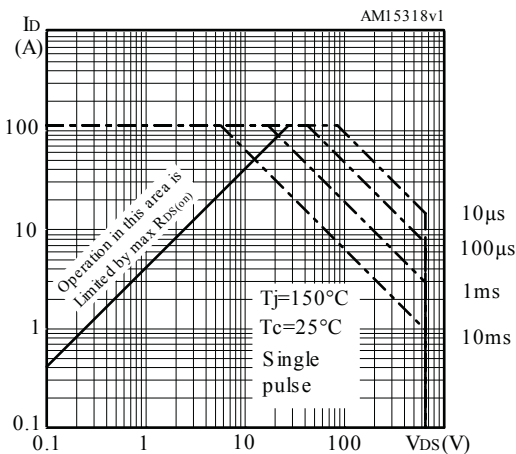
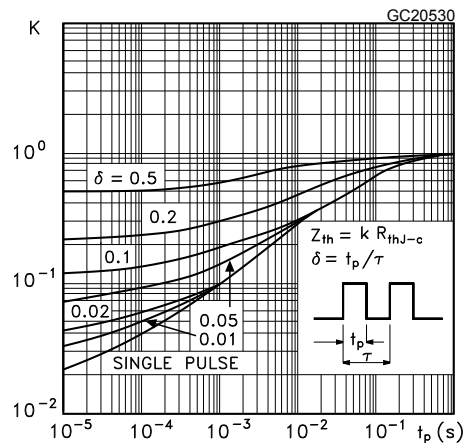
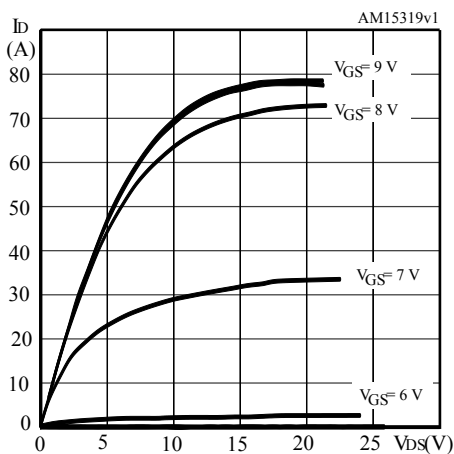
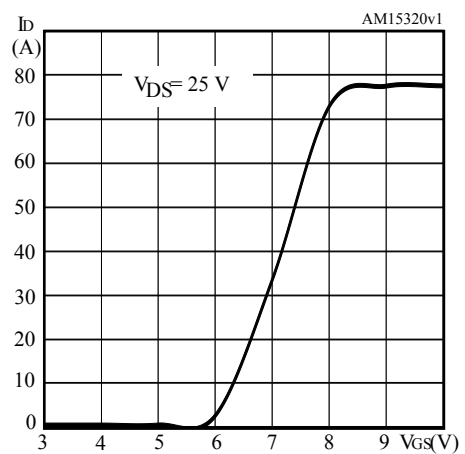
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area for D²PAK and TO-220

Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

Figure 3. Safe operating area for TO-247

Figure 4. Normalized transient thermal impedance for TO-247

Figure 5. Output characteristics

Figure 6. Transfer characteristics


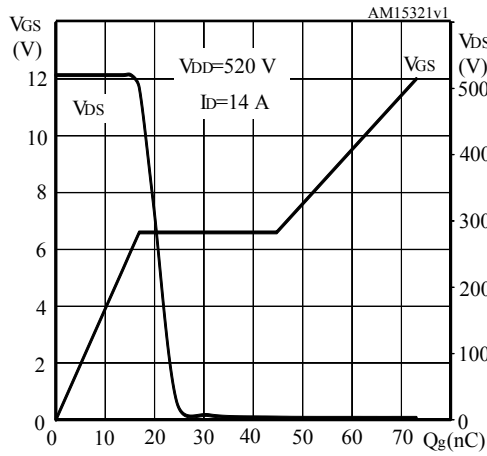
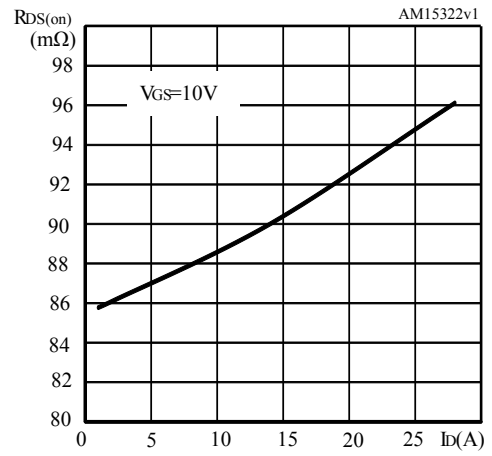
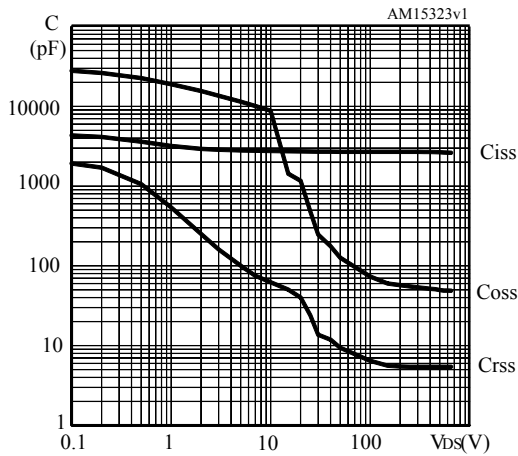
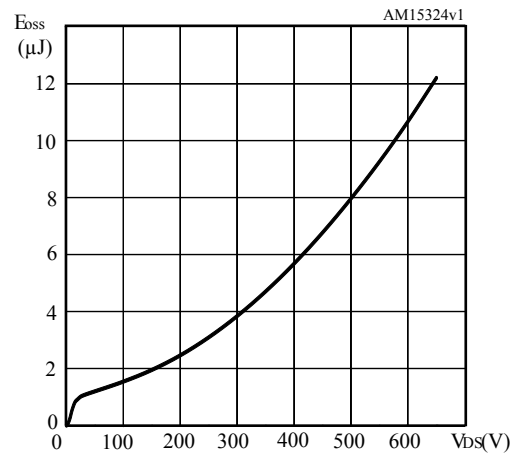
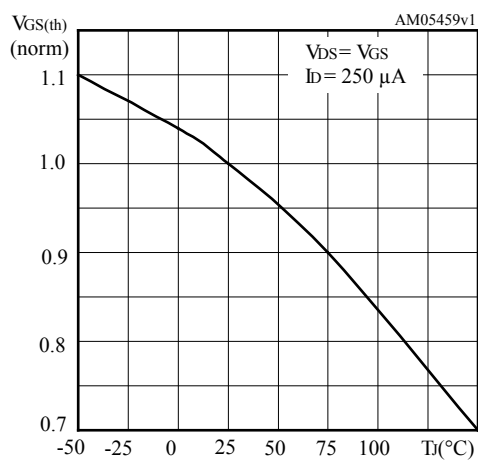
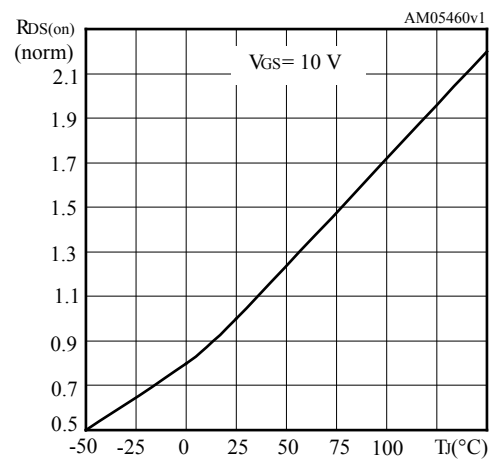
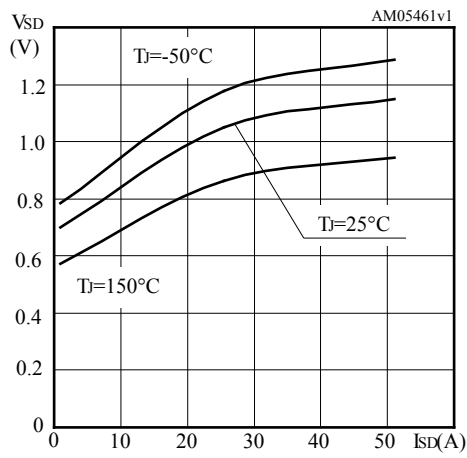
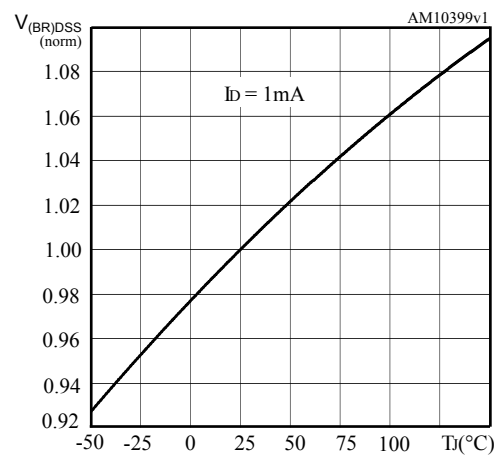
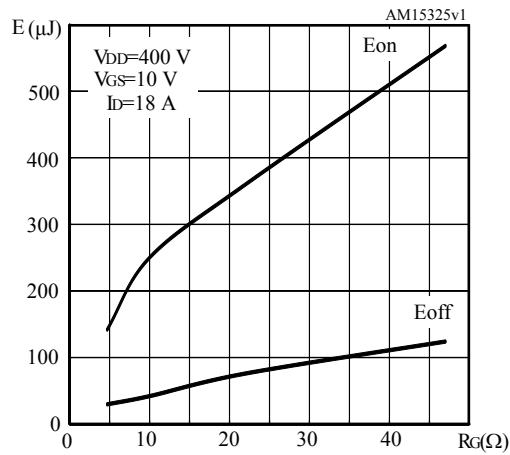
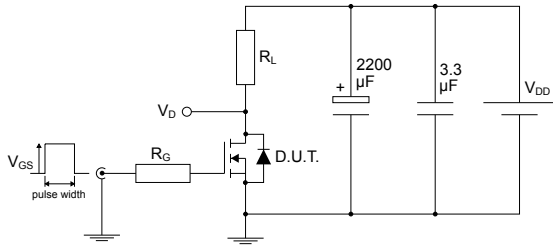
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


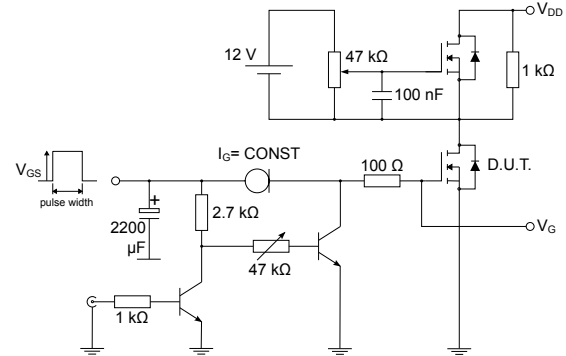
Figure 13. Drain-source diode forward characteristics

Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

Figure 15. Switching energy vs gate resistance


Note: E_{on} including reverse recovery of a SiC diode.

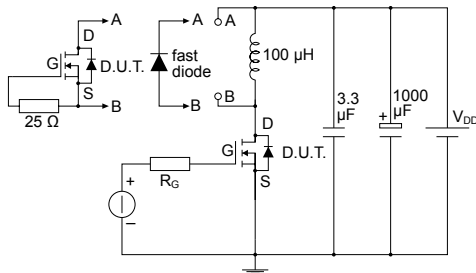
3 Test circuits

Figure 16. Test circuit for resistive load switching times


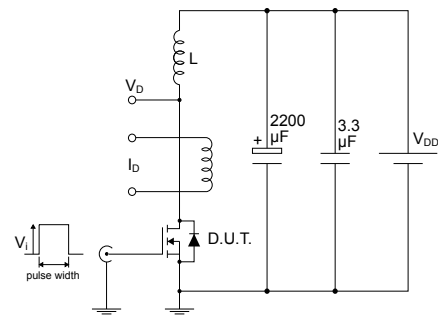
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Figure 17. Test circuit for gate charge behavior


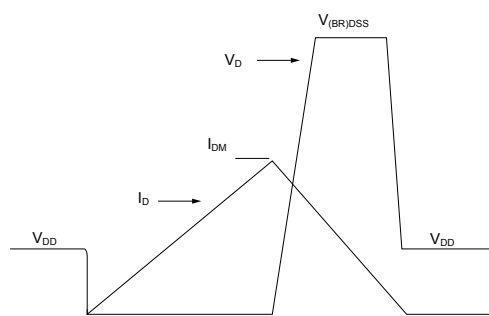
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Figure 18. Test circuit for inductive load switching and diode recovery times


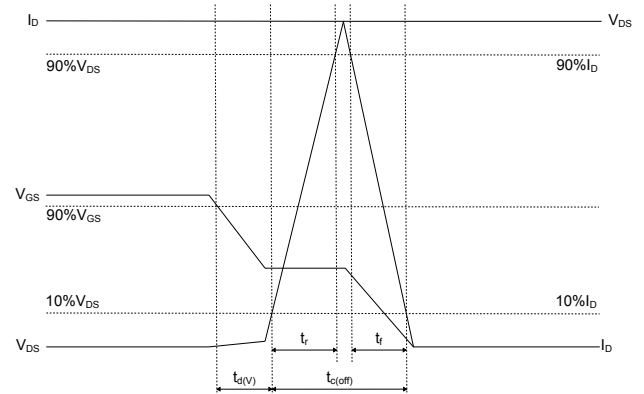
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Figure 19. Unclamped inductive load test circuit


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Figure 20. Unclamped inductive waveform


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Figure 21. Switching time waveform


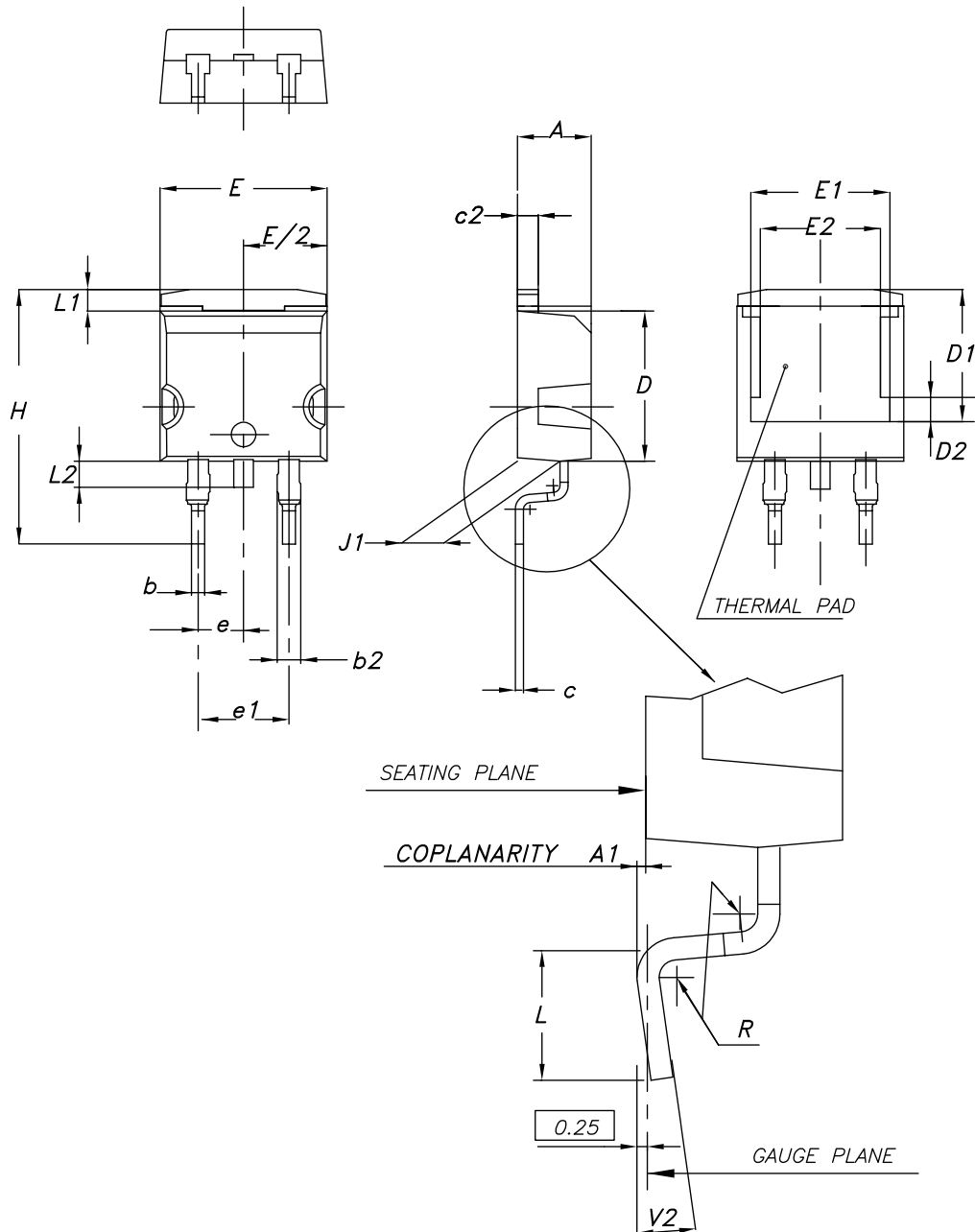
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 22. D²PAK (TO-263) type A2 package outline

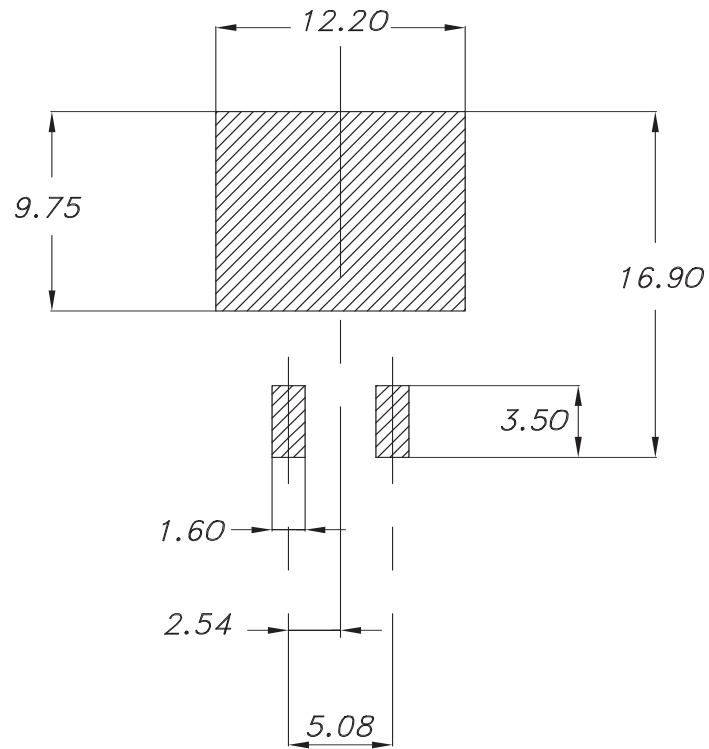


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Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

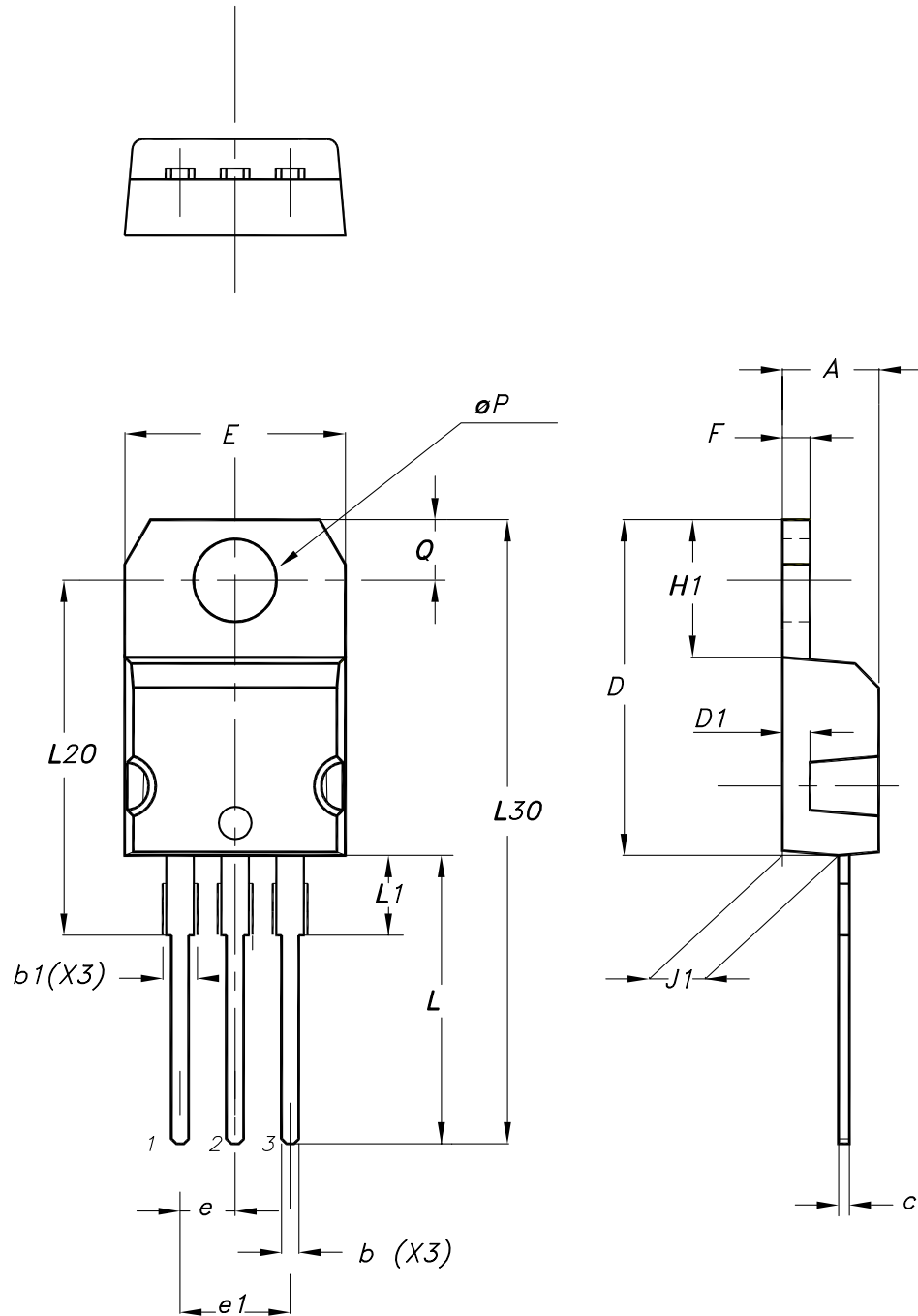
Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 TO-220 type A package information

Figure 24. TO-220 type A package outline



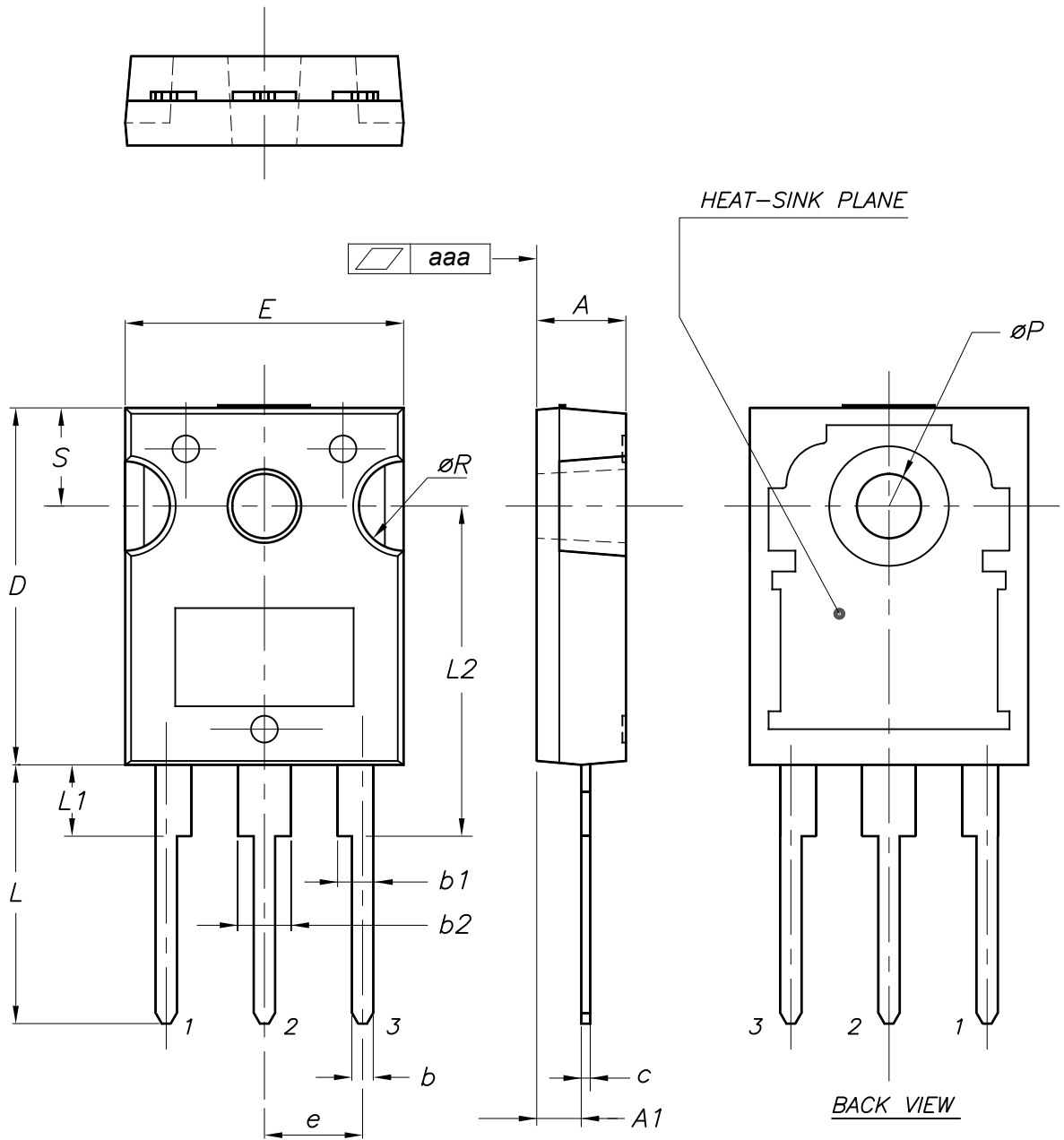
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Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 TO-247 package information

Figure 25. TO-247 package outline



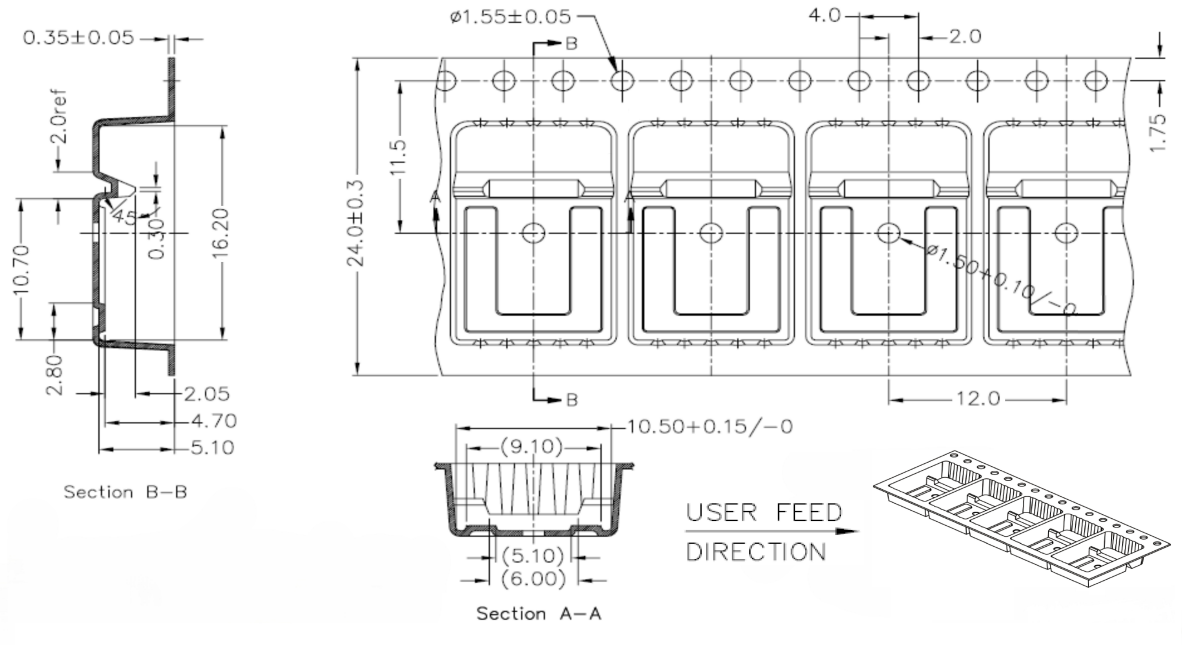
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Table 10. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.4 D²PAK packing information

Figure 26. D²PAK tape drawing (dimensions are in mm)



DM01095771_2



5 Ordering information

Table 11. Order codes

Order codes	Marking	Package	Packing
STB34N65M5	34N65M5	D ² PAK	Tape and reel
STP34N65M5		TO-220	Tube
STW34N65M5		TO-247	

Revision history

Table 12. Document revision history

Date	Revision	Changes
23-Feb-2012	1	First release.
15-Oct-2012	2	Added package, mechanical data: I ² PAKFP. Updated <i>Table 1: Device summary</i> , <i>Table 2: Absolute maximum ratings</i> , <i>Table 3: Thermal data</i> . Minor text changes. Curves inserted.
02-Oct-2013	3	The part numbers STF34N65M5 and STFI34N65M5 have been moved to the separate datasheet. Modified: <i>Figure 1</i> . Added: MOSFET dv/dt ruggedness parameter in <i>Table 2</i> . Updated: <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> . Minor text changes.
18-Sep-2025	4	Removed order code STI34N65M5. Updated <i>Table 6. Switching times</i> and <i>Section 4: Package information</i> . Minor text changes.



Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	D ² PAK (TO-263) type A2 package information	9
4.2	TO-220 type A package information	12
4.3	TO-247 package information	14
4.4	D ² PAK packing information	16
5	Ordering information	17
	Revision history	18



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