P-Channel Power MOSFET

-60V, -14.5A, 68 mΩ

FEATURES

- Improved dV/dt capability
- Fast switching
- Reliability meets AEC-Q101 requirements
- 100% Eas Guaranteed
- Pb-free plating
- RoHS compliant
- Halogen-Free

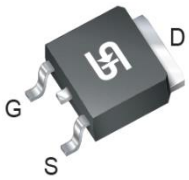
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-60	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	68	mΩ
	V_{GS} = -4.5V	110	
Q_g	V_{GS} = -10V	18	nC

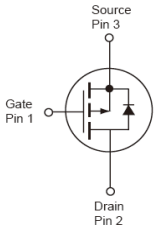
APPLICATIONS

- Motor Drive
- Power Tools
- LED Lighting

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-252 (DPAK)





Notes: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	-14.5	A
	T_C = 100°C		-9.2	
Pulsed Drain Current (Note 2)		I_{DM}	-58	A
Single Pulse Avalanche Current (Note 3)		I_{AS}	-19.1	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	18.2	mJ
Total Power Dissipation	T_C = 25°C	P_D	20.5	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	6.1	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	62	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	$V_{GS(TH)}$	-1.2	-1.4	-2.2	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = -60V	I_{DSS}	--	--	-1	μA
	V_{GS} = 0V, V_{DS} = -48V T_J = 125°C		--	--	-10	
Drain-Source On-State Resistance (Note 3)	V_{GS} = -10V, I_D = -6A	$R_{DS(on)}$	--	53.2	68	mΩ
	V_{GS} = -4.5V, I_D = -3A		--	67.4	110	
Forward Transconductance	V_{DS} = -10V, I_D = -6A	g_{fs}	--	15.3	--	S
Dynamic (Note 5)						
Total Gate Charge	V_{GS} = -10V, V_{DS} = -30V, I_D = -6A	Q_g	--	18	--	nC
Gate-Source Charge		Q_{gs}	--	2.8	--	
Gate-Drain Charge		Q_{gd}	--	3.2	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = -30V, f = 1.0MHz	C_{iss}	--	929	--	pF
Output Capacitance		C_{oss}	--	68	--	
Reverse Transfer Capacitance		C_{rss}	--	55	--	
Gate Resistance	f = 1.0MHz	R_g	--	14	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{GS} = -10V, V_{DS} = -30V, I_D = -1A, R_G = 6Ω	$t_{d(on)}$	--	6.7	--	nS
Rise Time		t_r	--	8.5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	53	--	
Fall Time		t_f	--	35	--	
Source-Drain Diode						
Diode Forward Voltage (Note 4)	V_{GS} = 0V, I_S = -1A	V_{SD}	--	--	-1	V
Reverse Recovery Time	I_S = -1A, di/dt = 100A/μs	t_{rr}	--	11.9	--	nS
Reverse Recovery Charge		Q_{rr}	--	6.2	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. L = 0.1mH, V_{GS} = -10V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

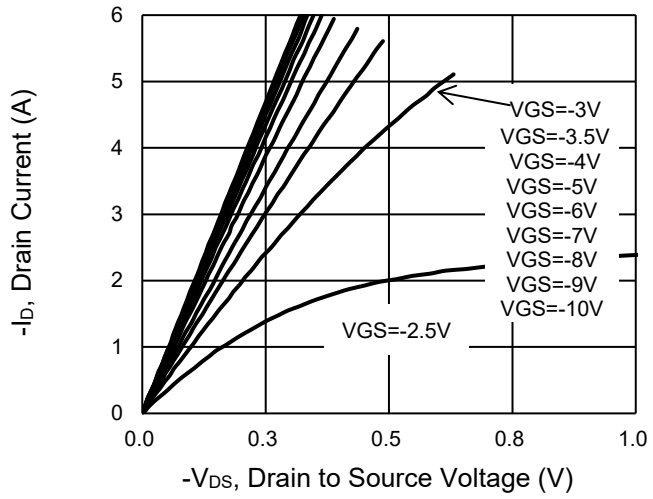
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM680P06CP ROG	TO-252 (DPAK)	2,500pcs / 13” Reel

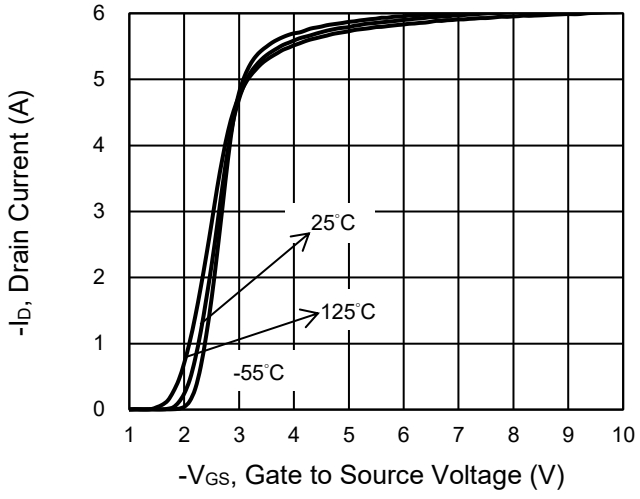
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

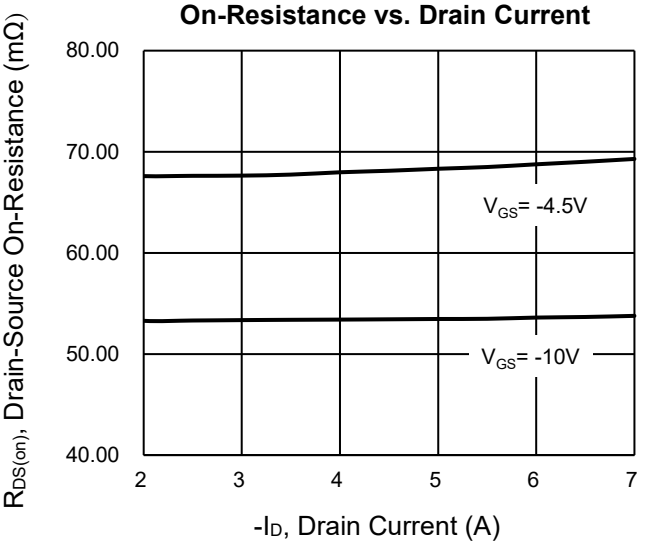
Output Characteristics



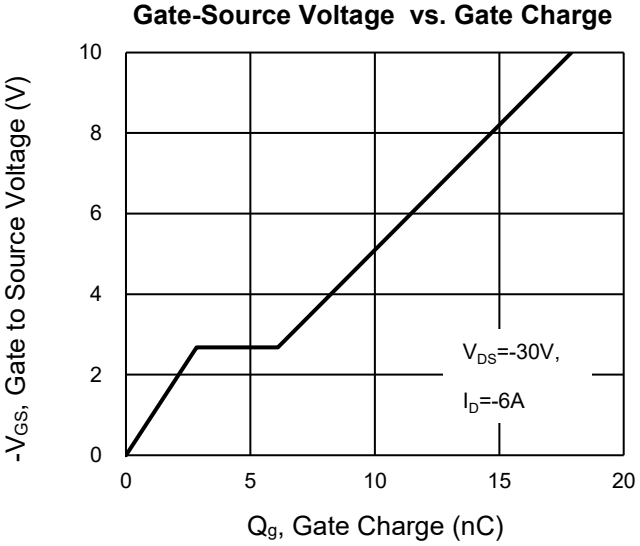
Transfer Characteristics



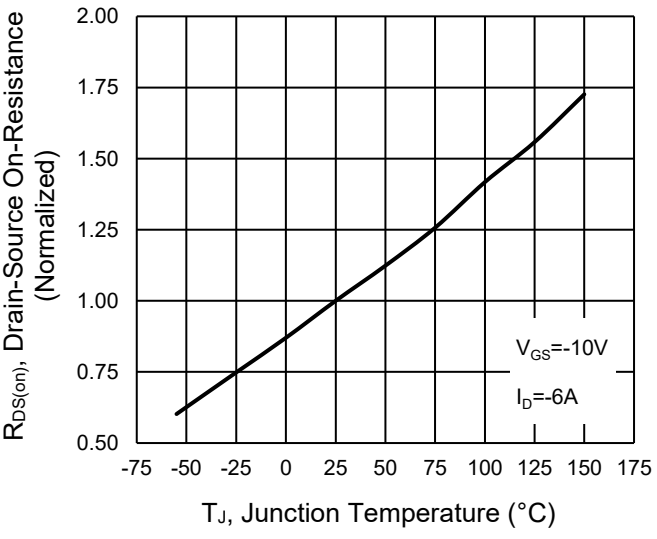
On-Resistance vs. Drain Current



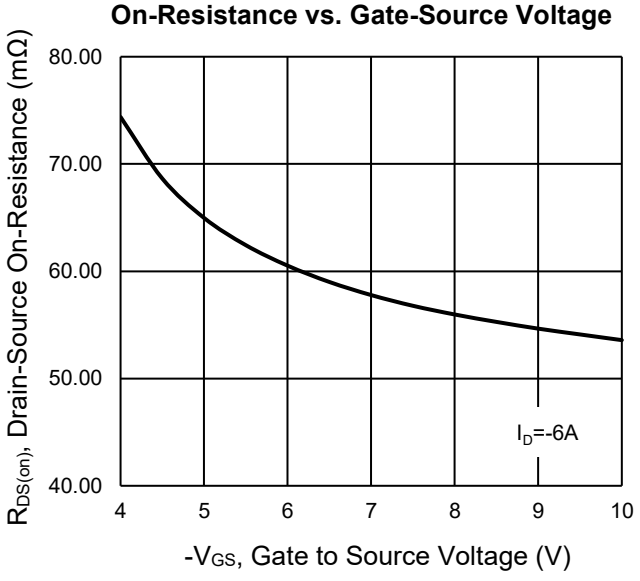
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



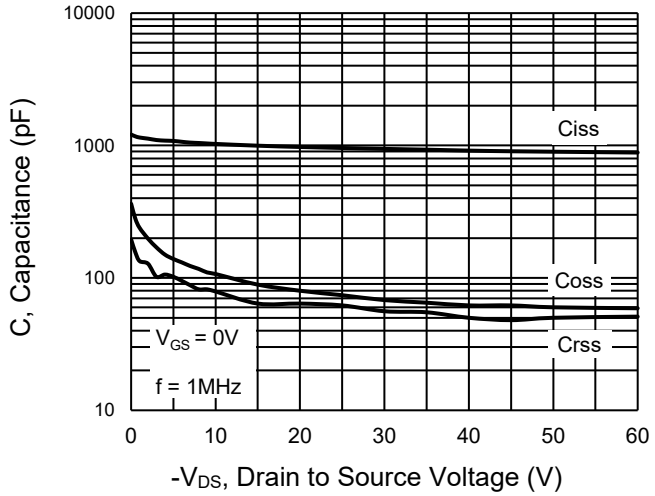
On-Resistance vs. Gate-Source Voltage



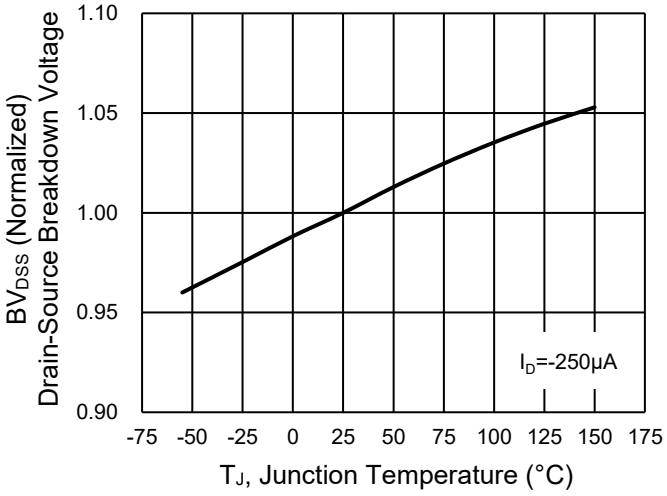
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

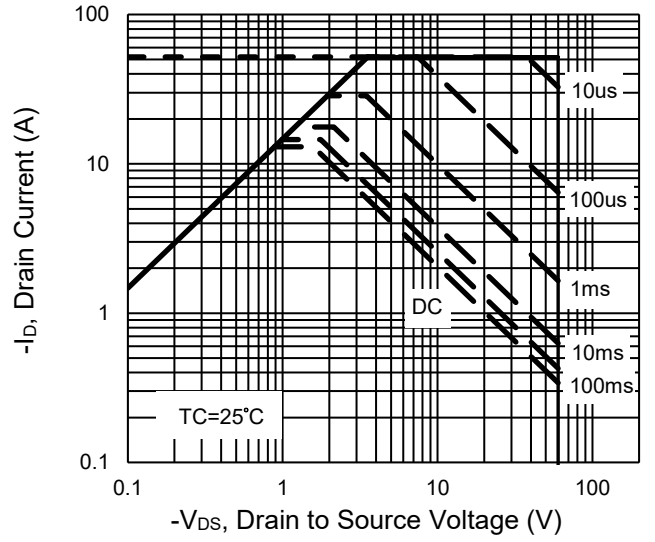
Capacitance vs. Drain-Source Voltage



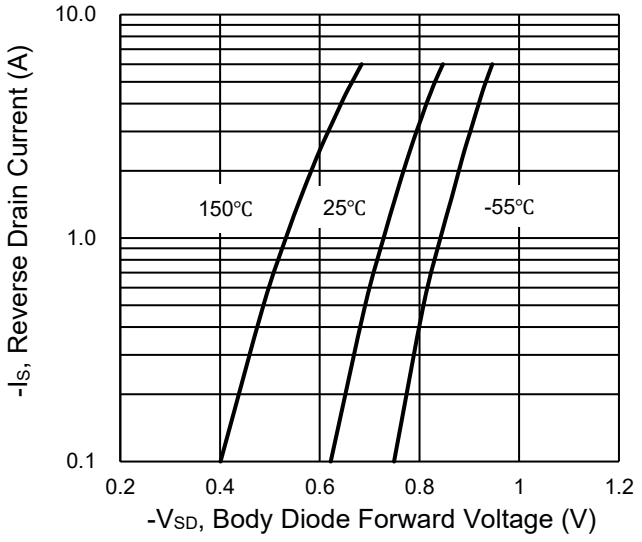
BV_{DSS} vs. Junction Temperature



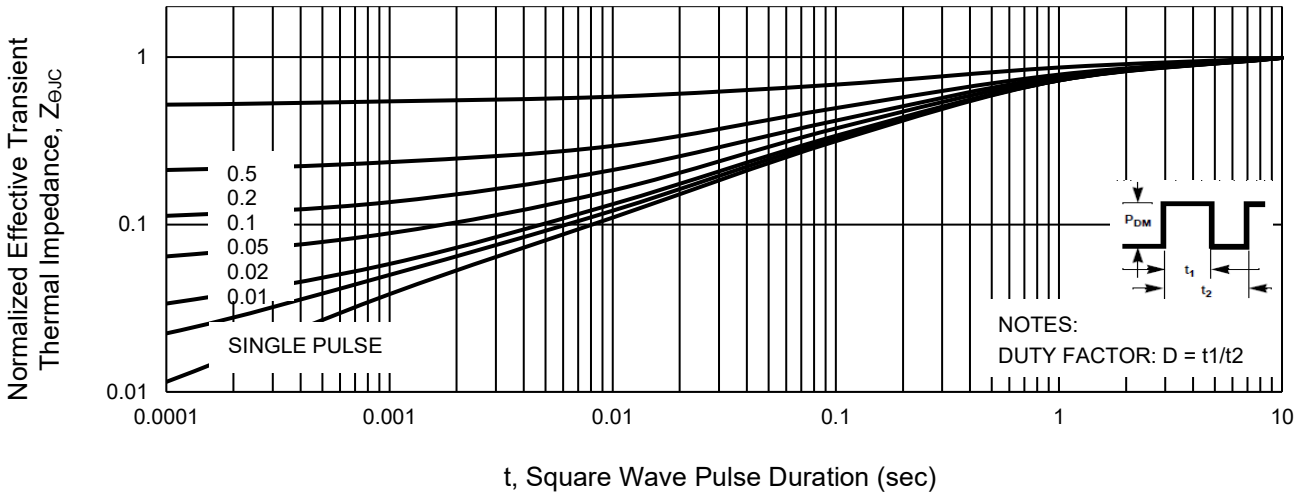
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



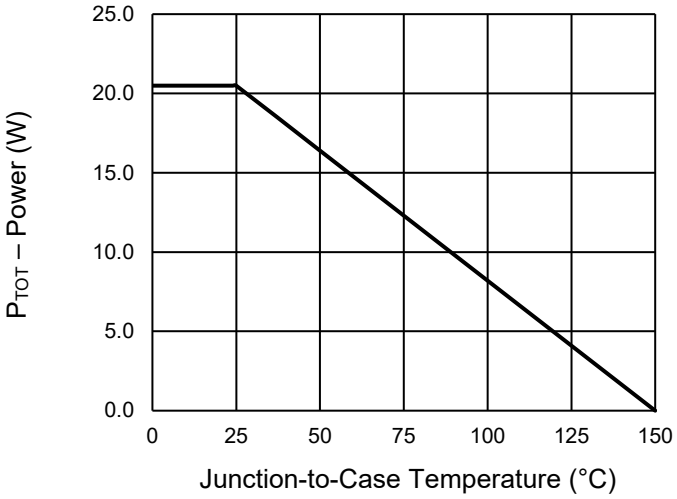
Normalized Thermal Transient Impedance, Junction-to-Case



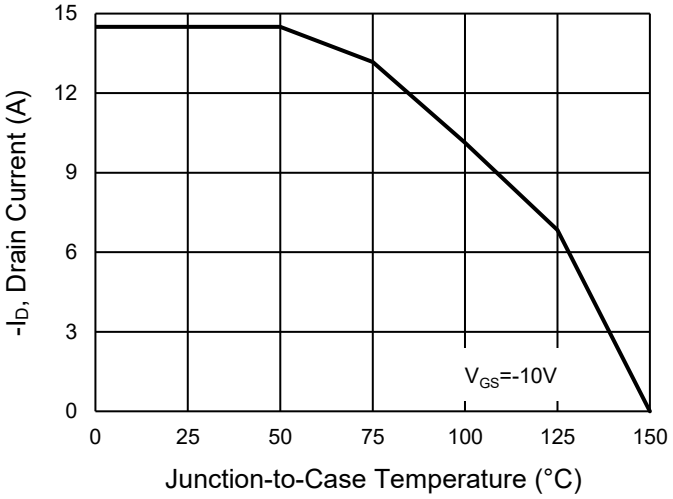
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

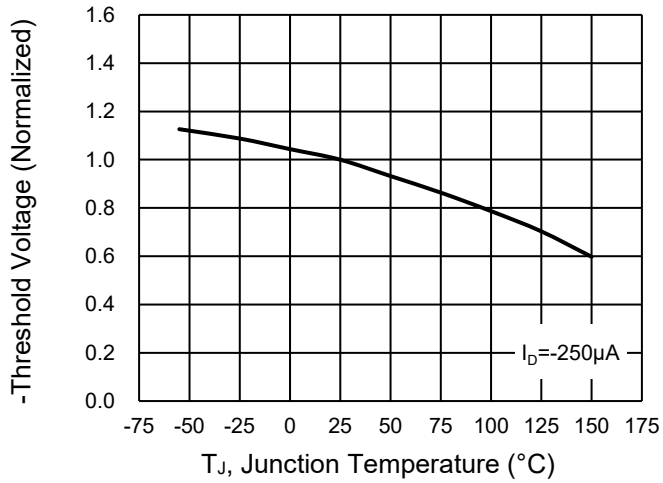
Power Dissipation



Drain Current

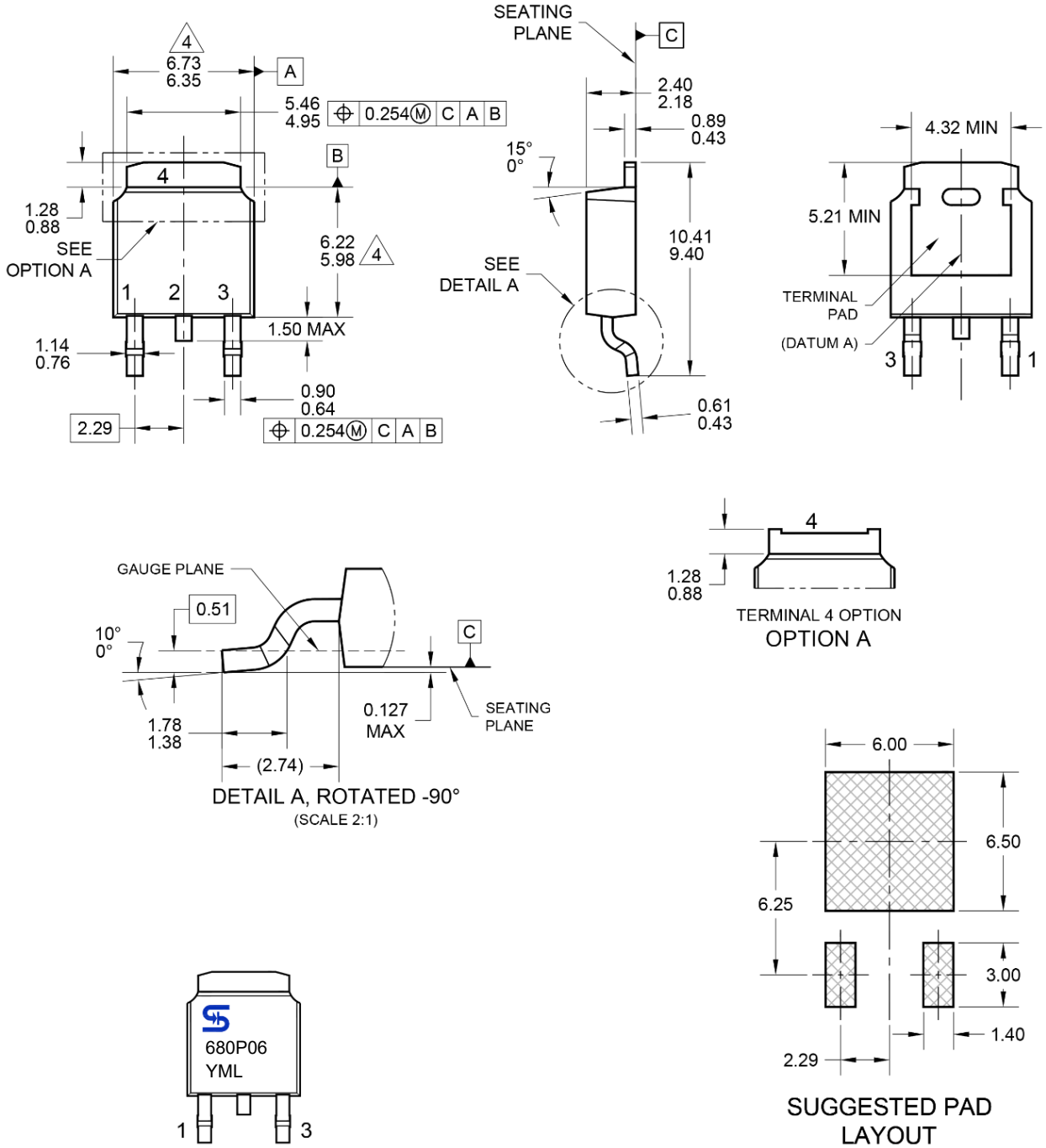


Normalized gate threshold voltage vs Temperature



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK)



MARKING DIAGRAM

680P06 = Device marking
Y = Year Code
M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apr, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
L = Lot Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-TO252AA-013 REV B.

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