

Inverting Regulator – Buck, Boost, Switching

DESCRIPTION

TS34063 is a monolithic switching regulator and subsystem intended for use as DC-to-DC converter. It consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver and high current output switch. The TS34063 is specifically designed to be incorporated in Step-Up, Step-Down and Voltage-Inverting applications with minimum number of external components.

FEATURES

- Power forward control circuit
- Operating voltage from 3V to 40V
- Low standby current
- Current limit adjustable
- Output switch current up to 1.5A
- Variable oscillator frequency up to 100kHz (max.)
- Output voltage adjustable
- RoHS compliant
- Halogen-free

APPLICATION

- Charger
- xD-ROM, xDSL products
- DC to DC converter

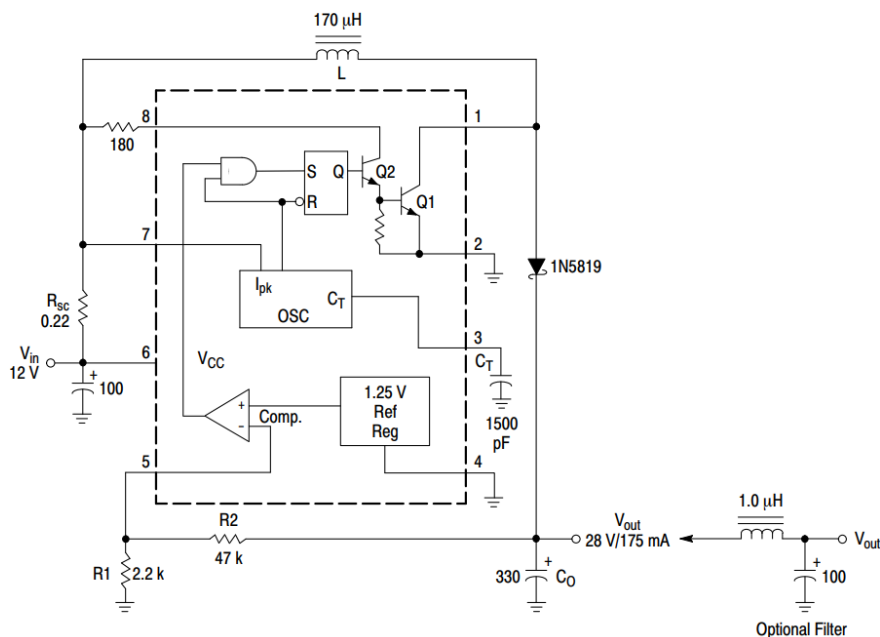


Pin Definition:

- | | |
|---------------------|-------------------------------|
| 1. Switch Collector | 5. Comparator Inverting Input |
| 2. Switch Emitter | 6. V_{CC} |
| 3. Timing Capacitor | 7. I_{pk} |
| 4. GND | 8. Driver Collector |

Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

TYPICAL APPLICATION CIRCUIT



Step-Up Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{FB}	-0.3 ~ 40	V
Switch Collector Output Voltage	$V_{C(SW)}$	40	V
Switch Emitter Voltage	$V_{E(SW)}$	40	mA
Switch Collector to Emitter Voltage	$V_{CE(SW)}$	40	mW
Driver Collector Voltage	$V_{C(DRIVER)}$	40	°C
Driver Collector Current (note 1)	$I_{C(DRIVER)}$	100	V
Output Switching Current	I_{SW}	1.5	A
Power Dissipation	P_D	0.5	W
Operating Ambient Temperature Range	T_{OPR}	-40 ~ +85	°C
Junction Temperature Range	T_J	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

ELECTRICAL SPECIFICATIONS ($V_{CC} = 5V$, $T_A = 25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator						
Frequency	F_{OSC}	$C_T = 1nF$, $V_{pin5} = 0V$	24	33	42	kHz
Charge Current	I_{CHARGE}	$V_{CC} = 5V \sim 40V$	24	30	42	μA
Discharge Current	$I_{DISCHARGE}$	$V_{CC} = 5V \sim 40V$	140	200	260	μA
Discharge to Charge current ratio	$I_{DISCHARGE} / I_{CHARGE}$	Pin7 to V_{CC}	5.2	6.5	7.5	--
Current Limit Sense Voltage	$V_{IPK(SENSE)}$	$I_{DISCHARGE} = I_{CHARGE}$	250	--	350	mV
Output switch (note1)						
Saturation Voltage	$V_{CE(SAT)}$	$I_{SW} = 1A$, Pin1, 8 connected	--	1.0	1.3	V
Saturation Voltage	$V_{CE(SAT)}$	$I_{SW} = 1A$, $I_D = 50mA$	--	0.45	0.7	V
DC current gain	H_{FE}	$I_{SW} = 1A$, $V_{CE} = 0.5V$	50	75	--	--
Collector off-state current	$I_{C(OFF)}$	$V_{CE} = 40V$	--	0.01	100	μA
Comparator						
Threshold Voltage	V_{REF}		1.225	1.25	1.275	V
Line regulation	REG_{LINE}	$V_{CC} = 3V \sim 40V$	--	--	6	mV
Total device						
Supply Current	I_{CC}	$V_{CC} = 5V \sim 40V$, $C_T = 1nF$, pin7= V_{CC} , pin5> V_{TH} , pin2=Gnd, remaining pins open	--	3	5	mA

Note:

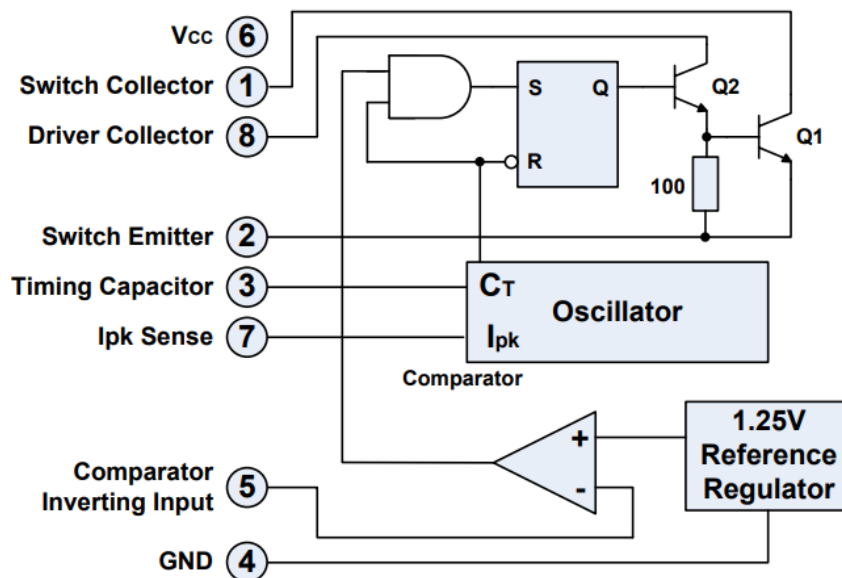
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
- If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300mA$) and high driver currents ($\geq 30mA$), it may take up to $2\mu s$ for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30kHz$ and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a Non-Darlington configuration is used, the following output drive condition is recommended: Forced Beta of output switch: $I_C \text{ output} / (I_C \text{ driver} - 7mA^*) \geq 10$

* The 100ohm resistor in the emitter of the driver divide requires about 7mA before the output switch conducts.

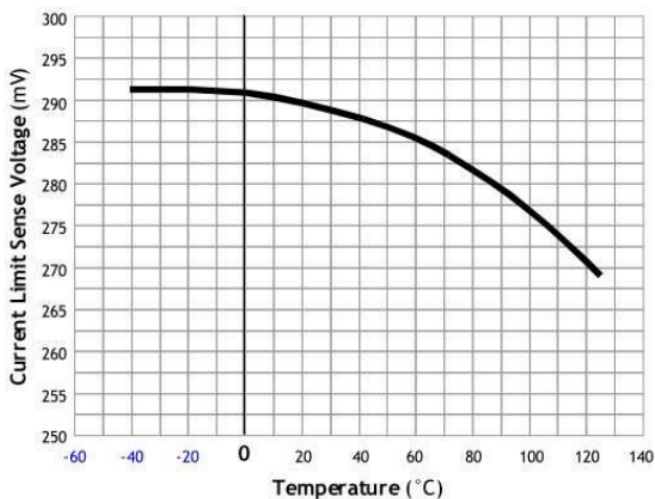
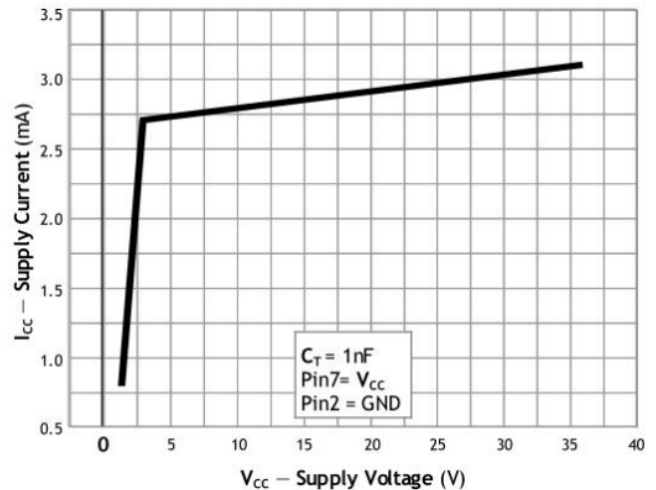
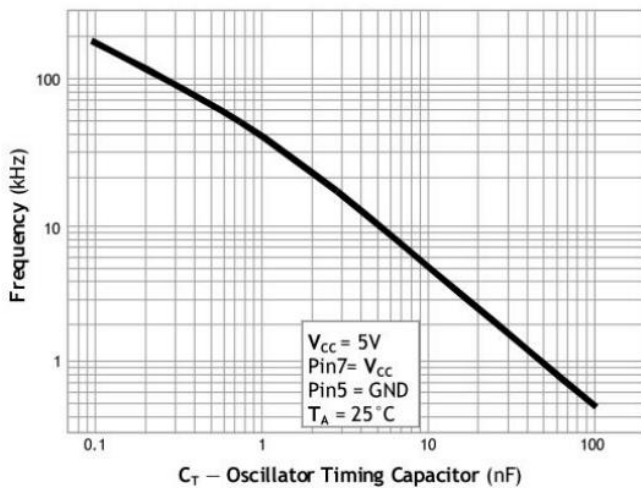
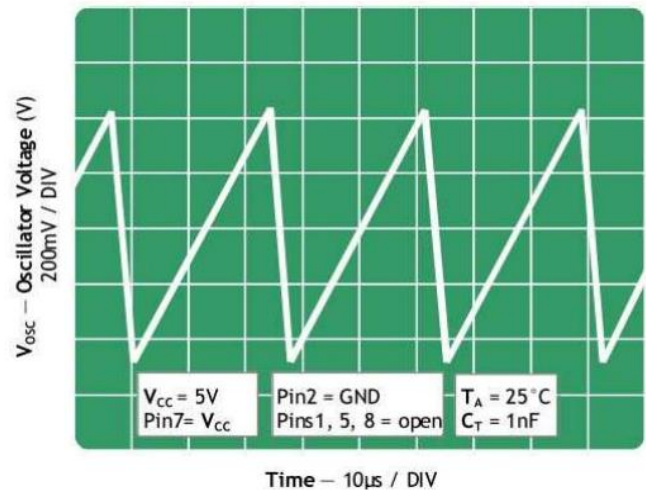
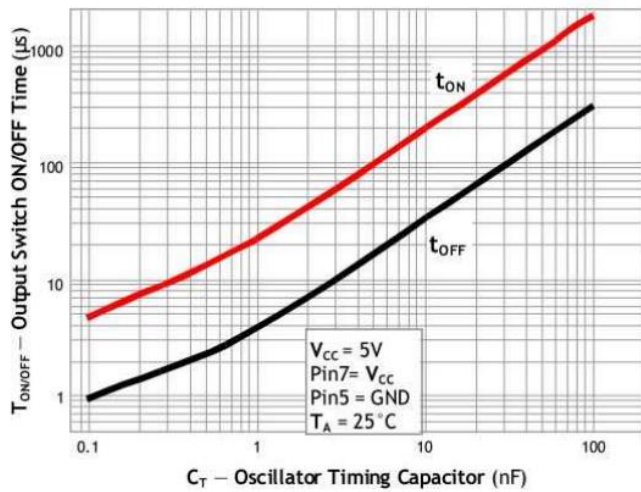
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TS34063CS RLG	SOP-8	2,500pcs / 13" Reel

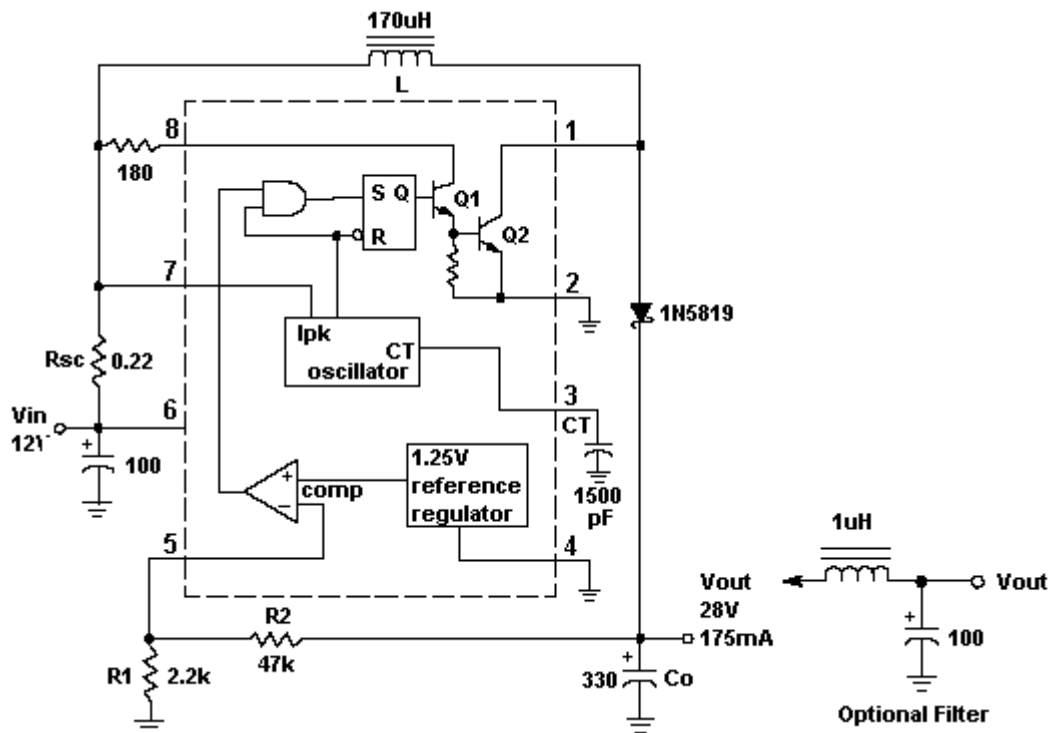
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS CURVE



TYPICAL APPLICATION CIRCUIT



Test	Conditions	Results
Line Regulation	$V_{IN} = 8V \sim 16V$, $I_O = 175mA$	$30mV = \pm 0.05\%$
Load Regulation	$V_{IN} = 12V$, $I_O = 75mA$ to $175mA$	$10mV = \pm 0.017\%$
Output Ripple	$V_{IN} = 12V$, $I_O = 175mA$	$400mV_{pp}$
Efficiency	$V_{IN} = 12V$, $I_O = 175mA$	87.7%
Output Ripple with Optional Filter	$V_{IN} = 12V$, $I_O = 175mA$	$40mV_{pp}$

Fig 6. Step-Up Converter

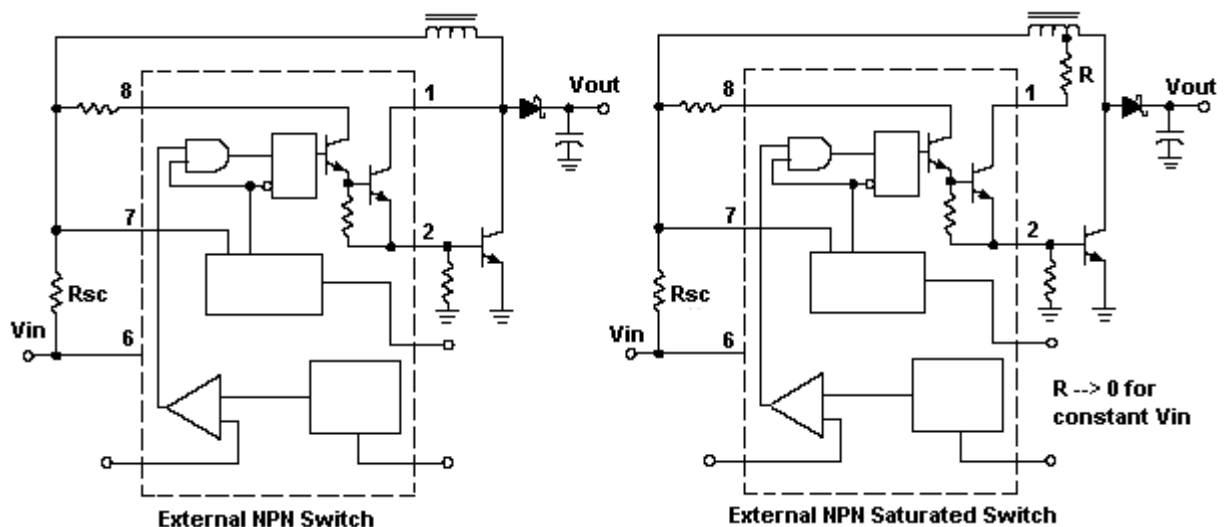
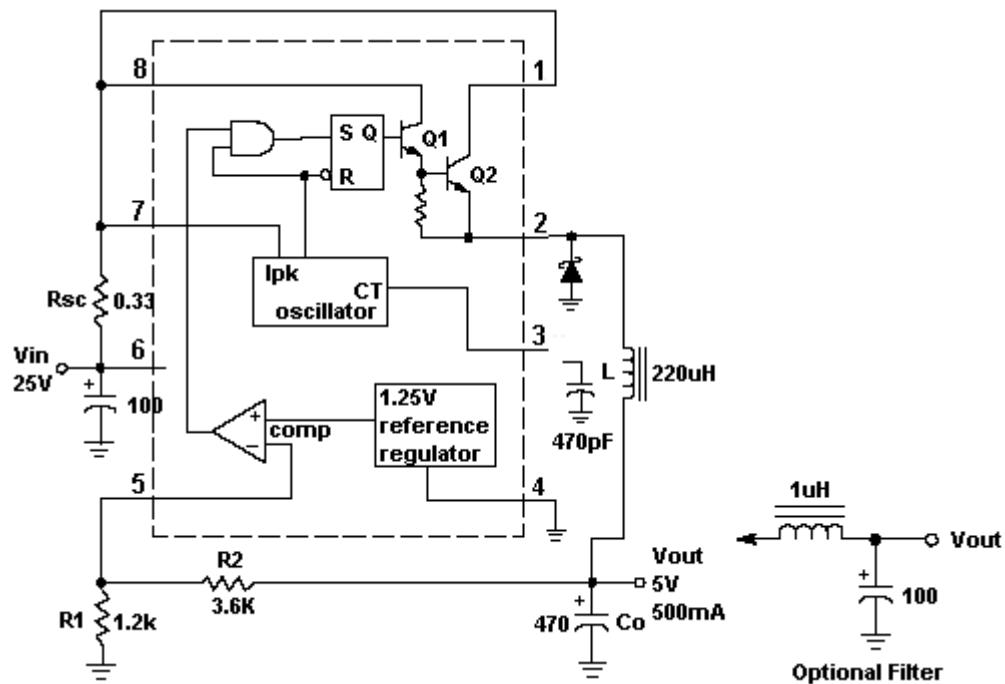


Fig. 7. External current Boost connections for IC peak greater than 1.5A

TYPICAL APPLICATION CIRCUIT (CONTINUE)



Test	Conditions	Results
Line Regulation	$V_{IN} = 15V \sim 25V$, $I_o = 500mA$	$12mV = \pm 12\%$
Load Regulation	$V_{IN} = 25V$, $I_o = 50mA$ to $500mA$	$3mV = \pm 0.03\%$
Output Ripple	$V_{IN} = 25V$, $I_o = 500mA$	$120mV_{pp}$
Short Circuit Current	$V_{IN} = 25V$, $R_L = 0.1m\Omega$	$1.1A$
Efficiency	$V_{IN} = 25V$, $I_o = 500mA$	83.7%
Output Ripple with Optional Filter	$V_{IN} = 25V$, $I_o = 500mA$	$40mV_{pp}$

Fig 8. Step-Down Converter

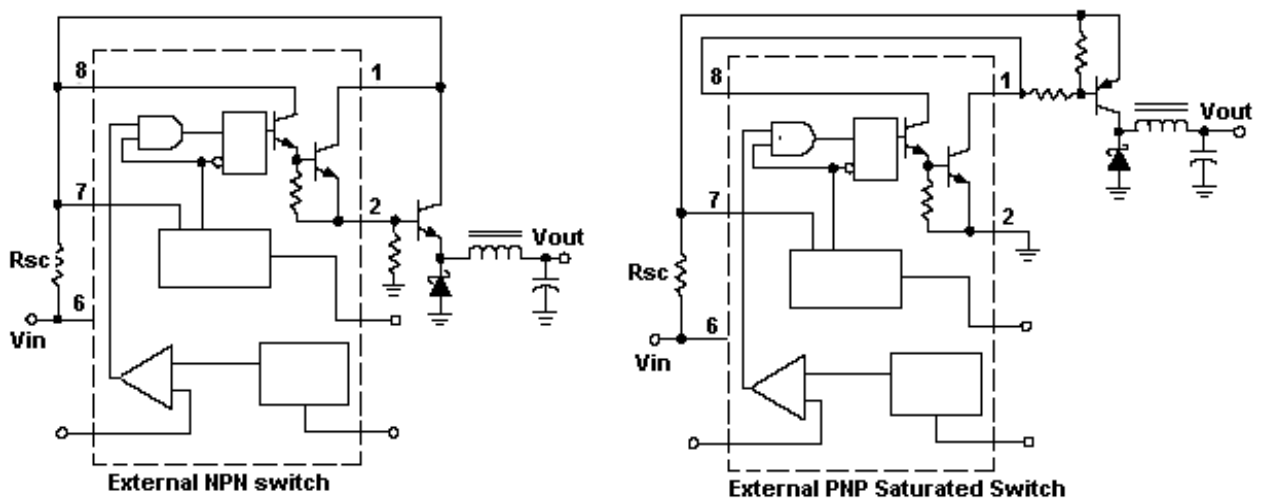
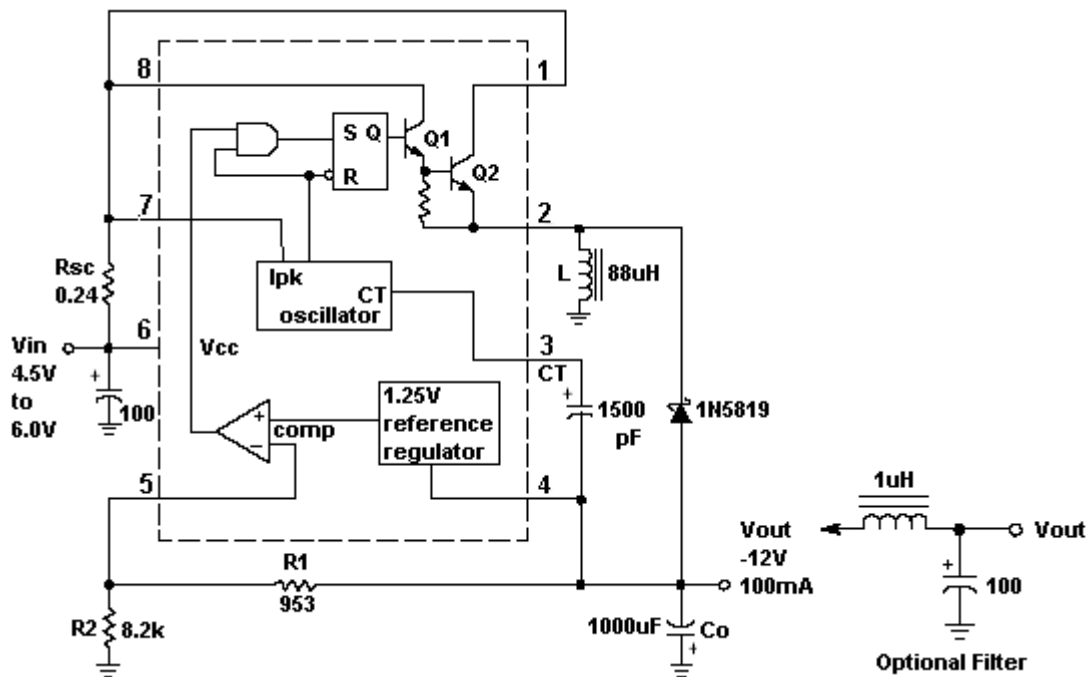


Fig. 9. External current Boost connections for IC peak greater than 1.5A

TYPICAL APPLICATION CIRCUIT (CONTINUE)



Test	Conditions	Results
Line Regulation	$V_{IN} = 4.5V \sim 6V$, $I_o = 100mA$	$3mV = \pm 120.012\%$
Load Regulation	$V_{IN} = 5V$, $I_o = 10mA$ to $100mA$	$0.022V = \pm 0.09\%$
Output Ripple	$V_{IN} = 5V$, $I_o = 100mA$	$500mV_{pp}$
Short Circuit Current	$V_{IN} = 5V$, $R_L = 0.1\Omega$	$910mA$
Efficiency	$V_{IN} = 5V$, $I_o = 100mA$	62.2%
Output Ripple with Optional Filter	$V_{IN} = 5V$, $I_o = 100mA$	$70mV_{pp}$

Fig 10. Voltage Inverting Converter

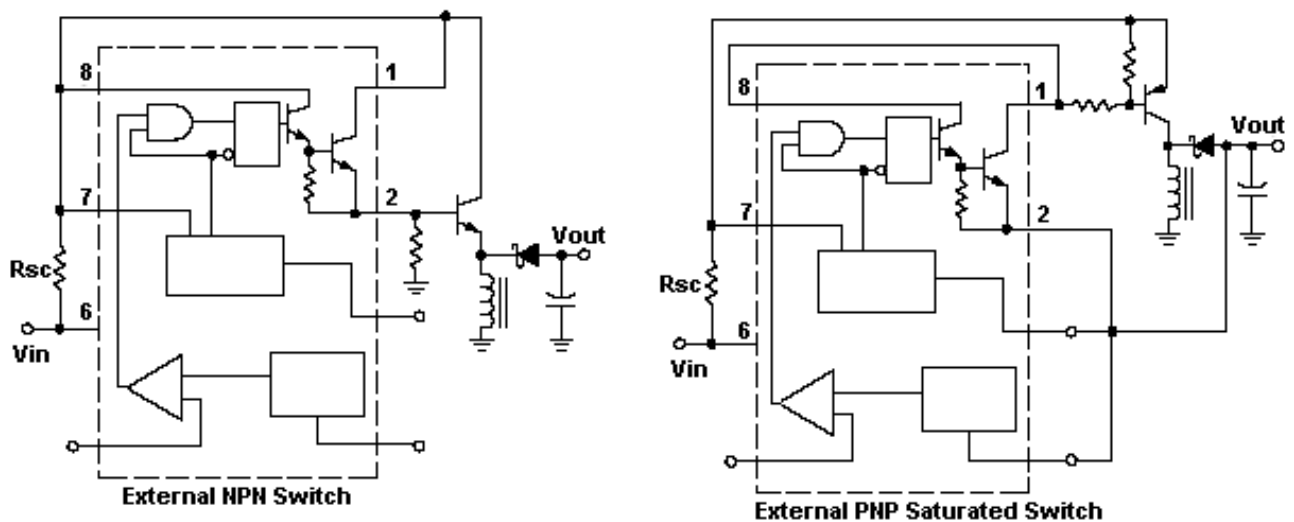


Fig. 11. External current Boost connections for IC peak greater than 1.5A

DESIGN FORMULA TABLE

Test	Step-Up	Step-Down	Voltage Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_f - V_{in(min)}}{V_{cc(min)} - V_{sat}}$	$\frac{V_{out} + V_f}{V_{cc} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_f}{V_{cc} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5} \text{ ton}$	$4.0 \times 10^{-5} \text{ ton}$	$4.0 \times 10^{-5} \text{ ton}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$\left(\frac{0.3}{I_{pk(switch)}} \right)$	$\left(\frac{0.3}{I_{pk(switch)}} \right)$	$\left(\frac{0.3}{I_{pk(switch)}} \right)$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) * t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) * t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) * t_{on(max)}$
C_o	$\left(9 \frac{I_{out} * t_{on}}{V_{ripple(pp)}} \right)$	$\left(\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}} \right)$	$\left(9 \frac{I_{out} * t_{on}}{V_{ripple(pp)}} \right)$

- V_{sat} = Saturation Voltage of the output switch.
- V_F = Forward Voltage drop of the rectifier.

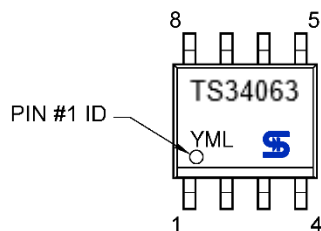
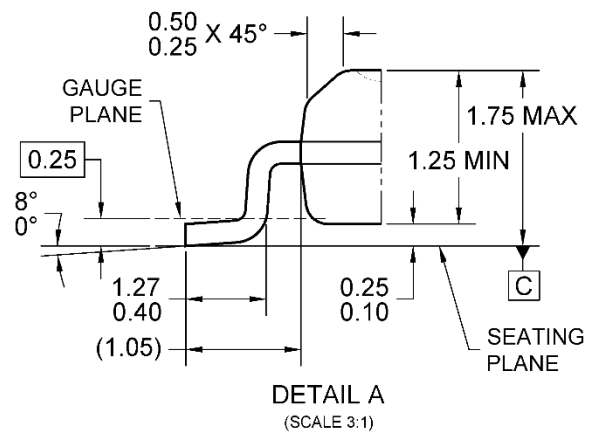
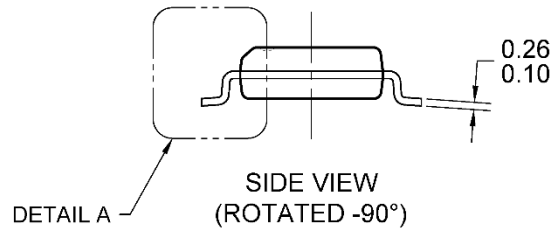
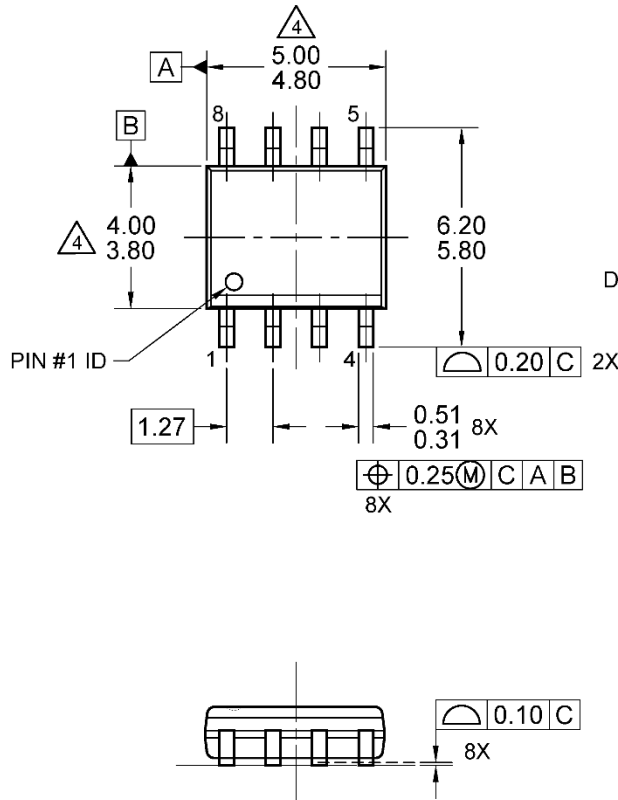
The following power supply characteristics must be chosen:

- V_{in} = Normal input voltage
- V_{out} : Desired Output voltage, $|V_{OUT}| = 1.25 (1 + R_2 / R_1)$
- I_{out} : Desired output current.
- f_{min} : Minimum desired output switching frequency at the selected values for V_{in} and I_o .
- $V_{ripple(p-p)}$: Desired peak-to-peak output ripple voltage. in practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

SOP-8



MARKING DIAGRAM

P/N = PRODUCT DEVICE CODE

Y = YEAR CODE

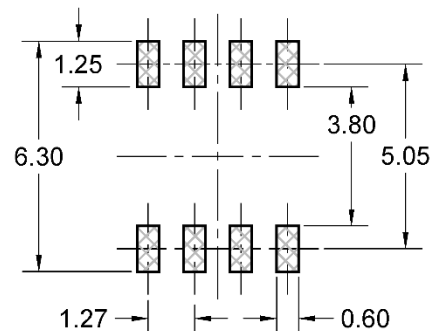
M = MONTH CODE FOR HALOGEN FREE PRODUCT

O = JAN P = FEB Q = MAR R = APR

S = MAY T = JUN U = JUL V = AUG

W = SEP X = OCT Y = NOV Z = DEC

L = LOT CODE



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PACKAGE OUTLINE REFERENCE: JEDEC MS-012, ISSUE G, VARIATION AA.

4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

5. DWG NO REF: HQ2SD07-SOP8STD-028 REV A.

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