Product/process change notification

PCN N° 2024-092-A

Dear customer,

Please find attached our Infineon Technologies AG PCN:

Transfer of wafer production site to Vanguard International Semiconductor Corporation – Fab3, Taiwan for IRL6372TRPBF

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before **2025-02-28.**
- Infineon aligns with the widely recognized JEDEC STANDARD **"JESD46",** which stipulates: **"Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."**

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

Infineon Technologies AG
Postal address D-81726 München Internet www.infineon.com Headquarters Am Campeon 1-15, D-85579 Neubiberg

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- **Products affected**

Please refer to attached affected product list
PCN_2024-092-A_[*customer-no*].pdf

- **Detailed change information**

Subject

Transfer of wafer production site to Vanguard International Semiconductor Corporation – Fab3, Taiwan for Gen12.2 product - IRL6372TRPBF

Reason

Transferring wafer production site to ensure supply continuity

Description

	Old	New
Wafer fab location	- Nexperia Newport Ltd, Newport, United Kingdom	- Vanguard International Semiconductor Corporation – Fab3, Taiwan
Wafer test location	- Nexperia Newport Ltd, Newport, United Kingdom	- ETREND Hightech Corp., Taiwan

- **Product identification**

Traceability assured via lot number & country of diffusion on product barcode label

- **Impact of change**

- No impact on electrical performance
- Quality and reliability verified by qualification
- No change in form, fit and function

- **Attachments**

PCN_2024-092-A_[*customer-no*].pdf	affected product list
2_cip24092_A.pdf	qualification report

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- **Time schedule**

- Final qualification report	available
- First samples available	on request
- Intended start of delivery	2025-04-15

If you have any questions, please do not hesitate to contact your local sales office.

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Transfer of wafer production site to Vanguard International Semiconductor Corporation - Fab3, Taiwan for IRL6372TRPBF

Sales name	SP number	OPN	Package	Customer part number
IRL6372TRPBF	SP001569038	IRL6372TRPBF	SO8	IRL6372TRPBF

RESTRICTED

Qualification Test Report

PCN No: 2024-092-A **Date: 2023-12-20**

Transfer of wafer production site to Vanguard International Semiconductor Corporation – Fab3, Taiwan for IRL6372TRPBF

Reason for choosing the following test vehicles:

IRL6372TRPBF	Large die for package; dual die; high voltage
IRLML6344TRPBF	Large die for package; dual die; high voltage
IRLHS6276TRPBF	Large die for package; dual die; high voltage

Scope of qualification: Gen 12.2 devices at VIS3

Assessment of Q-Results: **PASS**

Stress test	Abbreviation	Test conditions	Readout	IRL6372TRPBF	IRLML6344TRPBF	IRLHS6276TRPBF
				PG-DSO-8	PG-SOT23-3	PG-TSDSON-6
				fails / stressed	fails / stressed	fails / stressed
MSL Preconditioning JESD22-A113	**PC**	MSL # and 3x reflow at x °C	0h	MSL 1 and 3x reflow at 260 °C	MSL 1 and 3x reflow at 260 °C	MSL 1 and 3x reflow at 260 °C
High Temperature Reverse Bias JESD22-A108	**HTRB**	Tj = Tj max Vds = 80% Vds max	1000 h	0/77	0/77	0/77
Temperature Humidity Bias JESD22-A118	**H3TRB/THB**	T = 85 °C; RH = 85% Vds = 80% Vds max up to 100V	1000 h	0/77	0/77	0/77
Temperature Cycling JESD22-A104	**TC**	-55°C to 150°C	1000 x	0/77	0/77	0/77
Intermitted Operational Life Test MIL-STD 750/Meth.1037	**IOL**	Delta T = 100 K	1000 h	0/77	0/77	0/77

*Precondition is done only for SMD Packages before AC,UHAST, TC, IOL, and H3TRB

-- not performed

RESTRICTED

Qualification Test Report

PCN No: 2024-092-A **Date: 2020-05-04**

Transfer of wafer production site to Vanguard International Semiconductor Corporation – Fab3, Taiwan for IRL6372TRPBF

Reason for choosing the following test vehicles:

IRLR6225TRPBF	Medium Chip in package type 20V
IRLH6224TRPBF IRLML6346TRPBF	Medium Chip in package type 20V
IRLTS6342TRPBF	Medium Chip in package type 30V
IRLHS6376TRPBF	Biggest Chip in package type 30V
IRL6297SDTRPBF	Medium Chip in package type 30V
IRFH6200TRPBF IRLHM630TRPBF	Medium Chip in package type 20V
	Biggest Chip in package type 20V
	Biggest Chip in package type 30V

Scope of qualification: VIS qualification for fabrication of the Gen-12.2 silicon wafers

Assessment of Q-Results: **Pass**

Reference Products				**IRLR6225TRPBF**	**IRLH6224TRPBF**	**IRLML6346TRPBF**	**IRLTS6342TRPBF**	**IRLHS6376TRPBF**	**IRL6297SDTRPBF**	**IRFH6200TRPBF**	**IRLHM630TRPBF**
Package Type				PG-TO252-3	PG-TDSON-8	PG-SOT23-3	PG-TSOP-6	PG-TSDSON-6	MG-WDSON-6	PG-TDSON-8	PG-TSDSON-8
Stress test	**Abbreviation**	**Test conditions**	**Readout**	fails / stressed	fails / stressed	fails / stressed	fails / stressed	fails / stressed	fails / stressed	fails / stressed	fails / stressed
MSL Preconditioning JESD22-A113	**PC**	MSL & 3x reflow at x °C	0h	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C	MSL 1 & 3x reflow at 260 °C
High Temperature Gate Bias JESD22-A108	**HTGB**	Ta = Tj max Vgs = 80% Vgs max	1000 h	0 / 77	0 / 77	0 / 231 (3 lots x 77)	0 / 77	0 / 231 (3 lots x 77)	0 / 154 (2 lots x 77)	0 / 77	0 / 154 (2 lots x 77)
High Temperature Reverse Bias JESD22-A108	**HTRB**	Tj = Tj max Vds = 80% Vds max	1000 h	0 / 77	0 / 77	0 / 231 (3 lots x 77)	0 / 77	0 / 231 (3 lots x 77)	0 / 154 (2 lots x 77)	0 / 77	0 / 154 (2 lots x 77)
Temperature Humidity Bias JESD22-A101	**H3TRB/THB***	T = 85 °C RH = 85% Vds = 80% Vds max up to 100 Vds	1000 h	0 / 77	0 / 77	0 / 231 (3 lots x 77)	0 / 77	0 / 154 (2 lots x 77)	0 / 154 (2 lots x 77)	0 / 77	0 / 154 (2 lots x 77)
Temperature Cycling JESD22-A104	**TC***	Ta min= -55 °C Ta max= + 150 °C	1000 **c**	0 / 77	0 / 77	0 / 231 (3 lots x 77)	0 / 77	0 / 231 (3 lots x 77)	0 / 154 (2 lots x 77)	0 / 77	0 / 154 (2 lots x 77)
Intermitted Operational Life Test MIL-STD 750/Meth.1037	**IOL***	Delta T = 100 K	1000 **h**	0 / 77	0 / 77	-	-	-	-	0 / 77	0 / 154 (2 lots x 77)
Unbiased Temperature/Humidity JESD22-A118	**UHAST***	Ta = 130 °C, RH = 85%	96 h	0 / 77	0 / 77	-	-	-	-	0 / 77	0 / 154 (2 lots x 77)

*Precondition is done only for SMD Packages before AC,UHAST, TC, IOL, and H3TRB

-- not performed

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Customer approval form

Transfer of wafer production site to Vanguard International Semiconductor Corporation – Fab3, Taiwan for Gen12.2 product - IRL6372TRPBF

☐ **Please list product(s) affected in your application(s):**

Please check the appropriate box below:

☐ **We agree with this proposed change and its schedule.**

☐ **We have objections:**

☐ **We need more information:**

☐ **We need samples:**

Sender

Company: Name:

Address/location: E-Mail:

Telephone:

Signature Date:

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Please return to your sales partner:

Company: Infineon Technologies AG

Name:

Address/Location:

E-mail:

Telephone: