

FEATURES

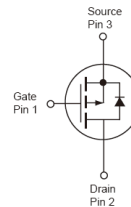
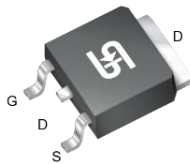
- Low $R_{DS(on)}$ to minimize conductive losses
- Low gate charge for fast power switching
- Reliability meets AEC-Q101 requirements
- 100% UIS tested
- RoHS Compliant
- Halogen-Free

APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC converter
- Secondary Synchronous Rectification



TO-252(DPAK)



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	-104	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	-7	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	90.2	mJ
Total Power Dissipation	P_D	60	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.5	-2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = -60V$	I_{DSS}	--	--	-1	μA
	$V_{GS} = 0V, V_{DS} = -48V$		--	--	-10	
	$T_J = 125^{\circ}C$					
Drain-Source On-State Resistance (Note 3)	$V_{GS} = -10V, I_D = -8A$	$R_{DS(on)}$	--	40	48	m Ω
	$V_{GS} = -4.5V, I_D = -4A$		--	51	65	
Forward Transconductance (Note 3)	$V_{DS} = -10V, I_D = -8A$	g_{fs}	--	19	--	S
Dynamic						
Total Gate Charge	$V_{GS} = -10V, V_{DS} = -30V$ $I_D = -8A$	Q_g	--	24	--	nC
Gate-Source Charge		Q_{gs}	--	3.9	--	
Gate-Drain Charge		Q_{gd}	--	4.8	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = -30V,$ $f = 1.0MHz$	C_{iss}	--	1309	--	pF
Output Capacitance		C_{oss}	--	86	--	
Reverse Transfer Capacitance		C_{rss}	--	36	--	
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = -10V, V_{DS} = -30V,$ $I_D = -1A, R_G = 6\Omega$	$t_{d(on)}$	--	6.6	--	nS
Rise Time		t_r	--	2.7	--	
Turn-Off Delay Time		$t_{d(off)}$	--	63	--	
Fall Time		t_f	--	32	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = -1A$	V_{SD}	--	--	-1	V

Notes:

- Limited by maximum junction temperature.
- $L = 3.68\text{mH}$, $V_{GS} = 10V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

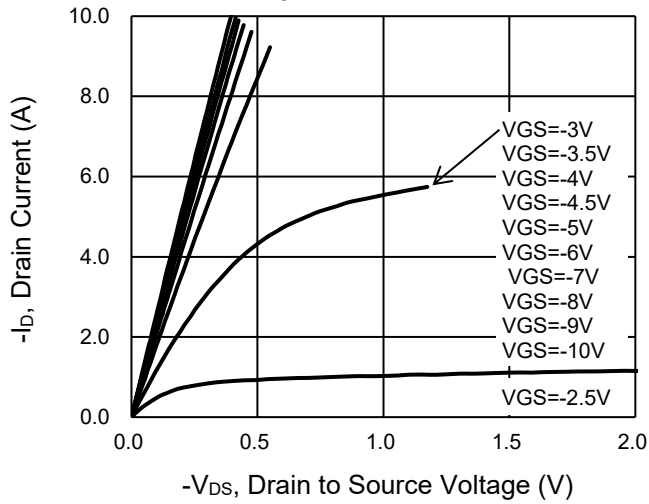
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM480P06CP ROG	TO-252(DPAK)	2,500pcs / 13" Reel

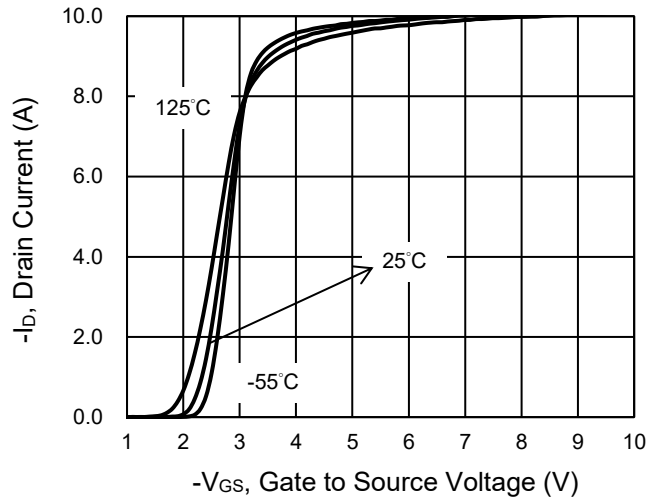
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

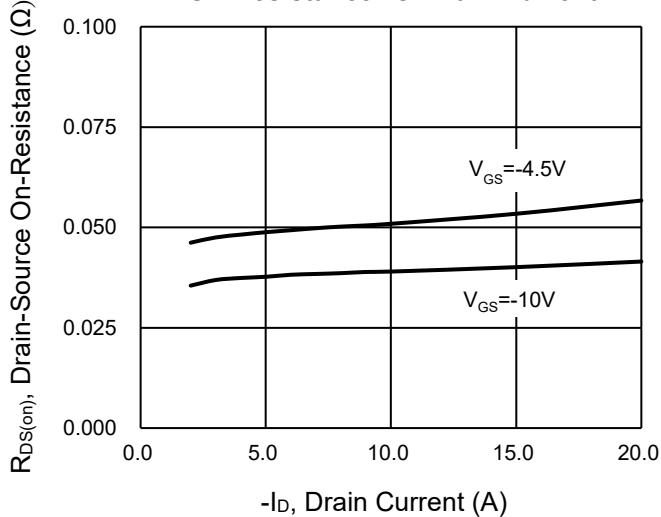
Output Characteristics



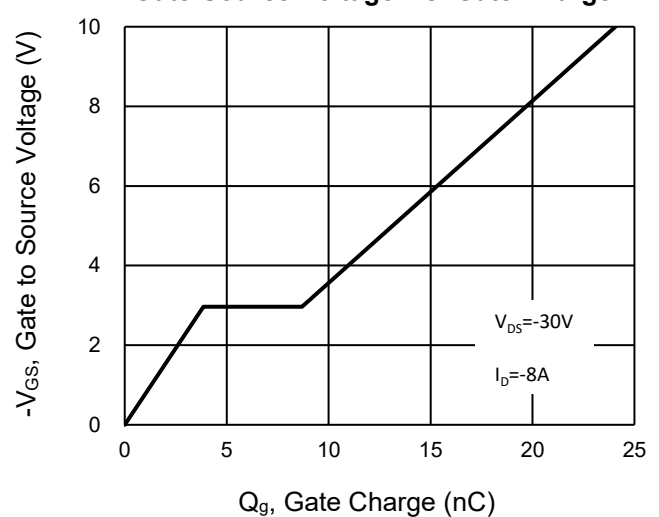
Transfer Characteristics



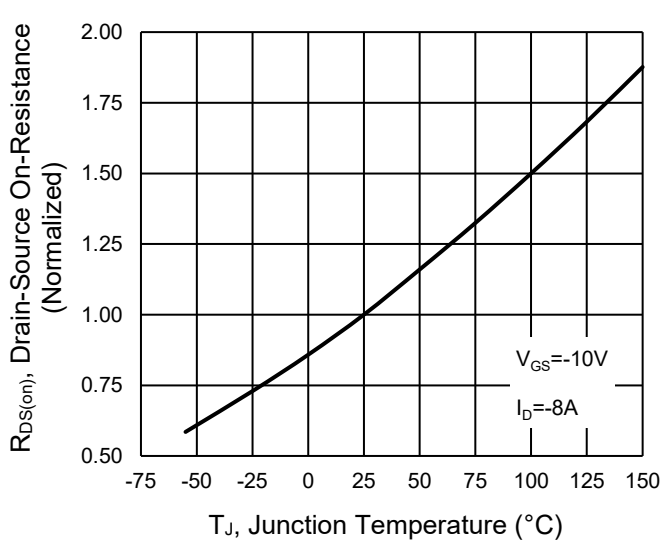
On-Resistance vs. Drain Current



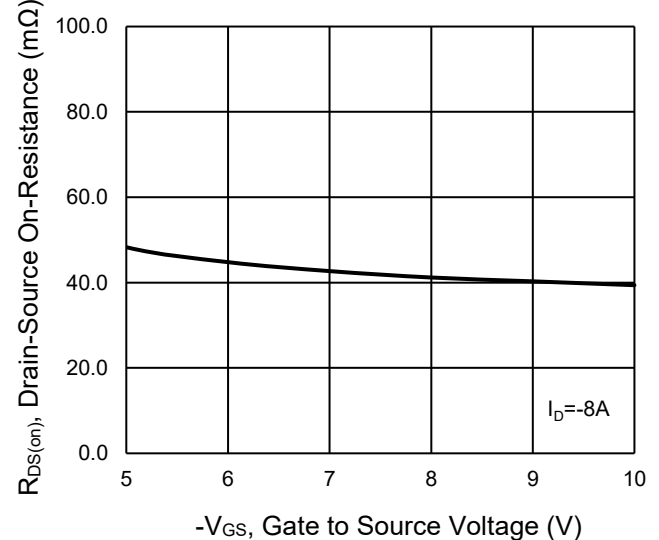
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



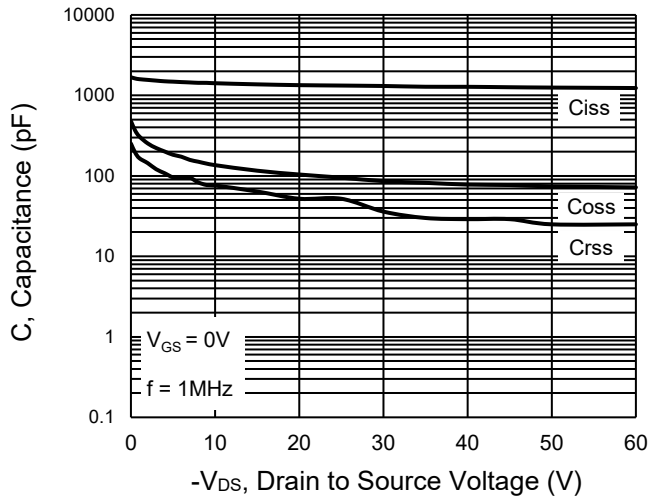
On-Resistance vs. Gate-Source Voltage



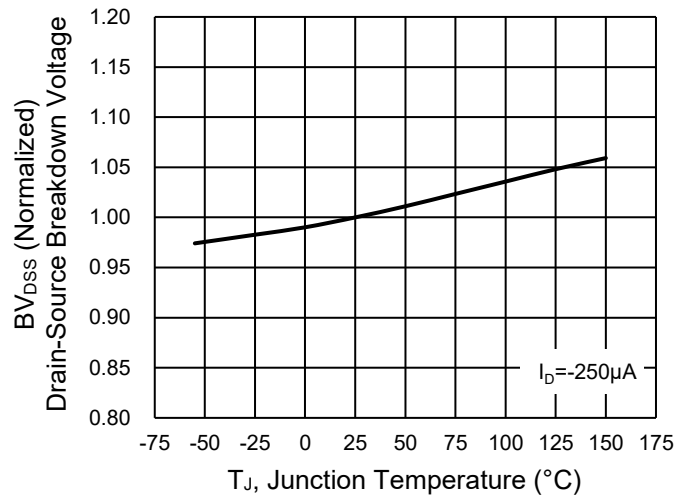
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

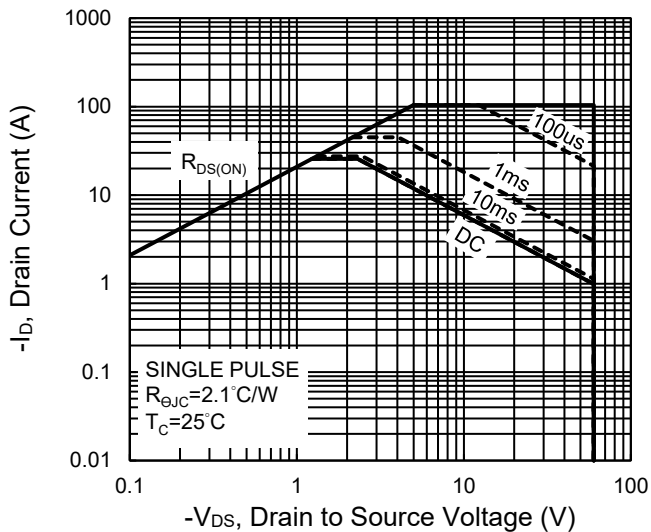
Capacitance vs. Drain-Source Voltage



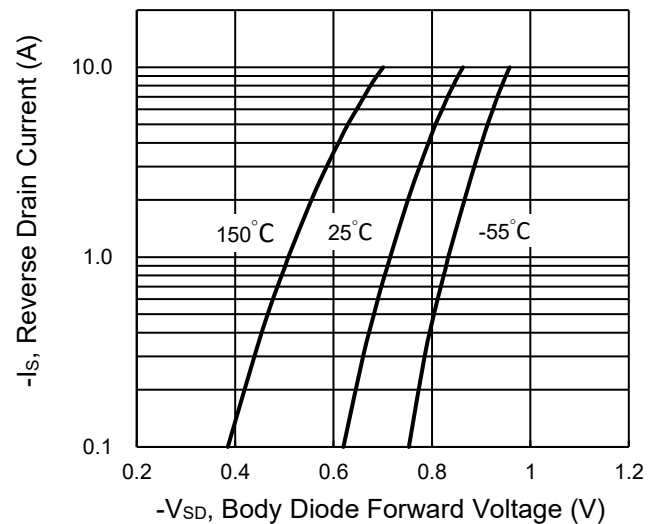
BV_{DSS} vs. Junction Temperature



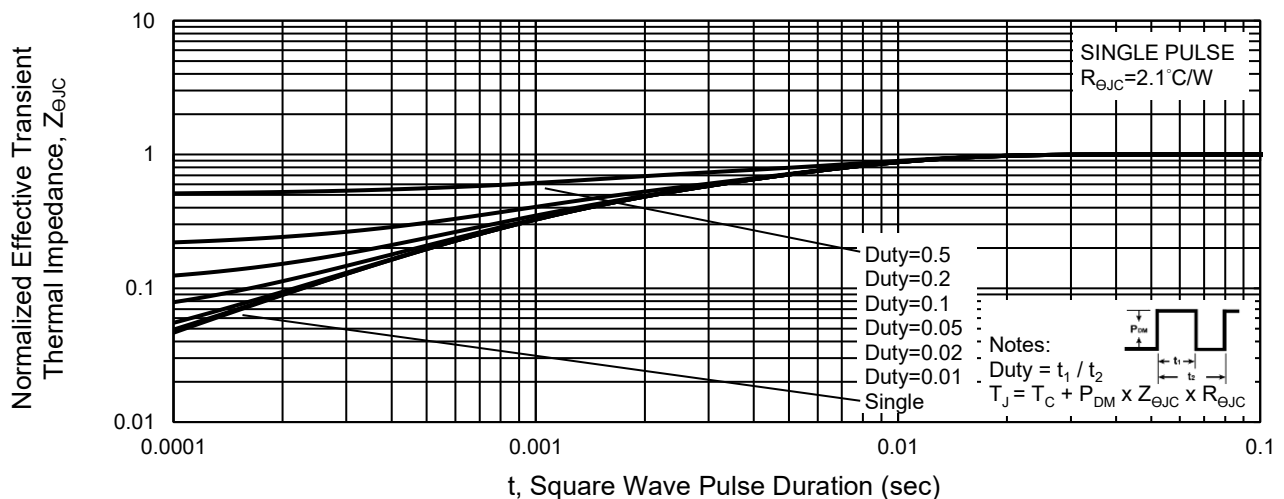
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

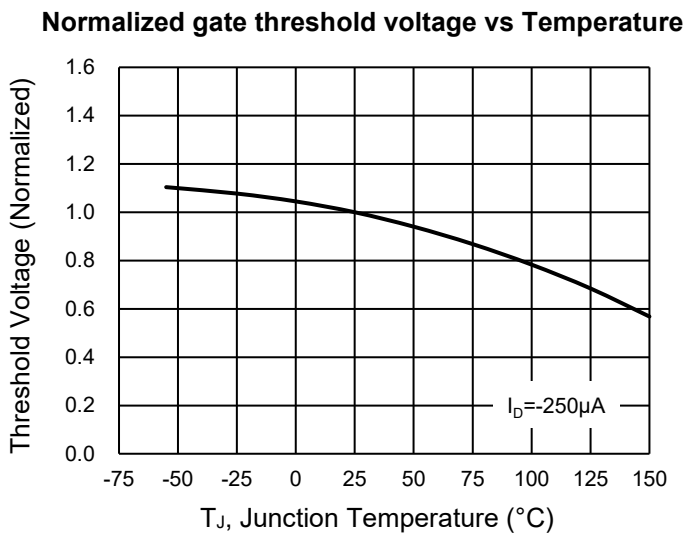
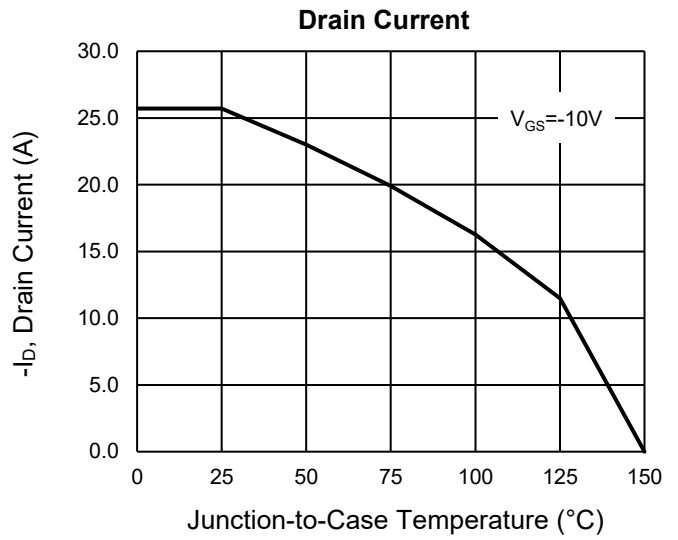
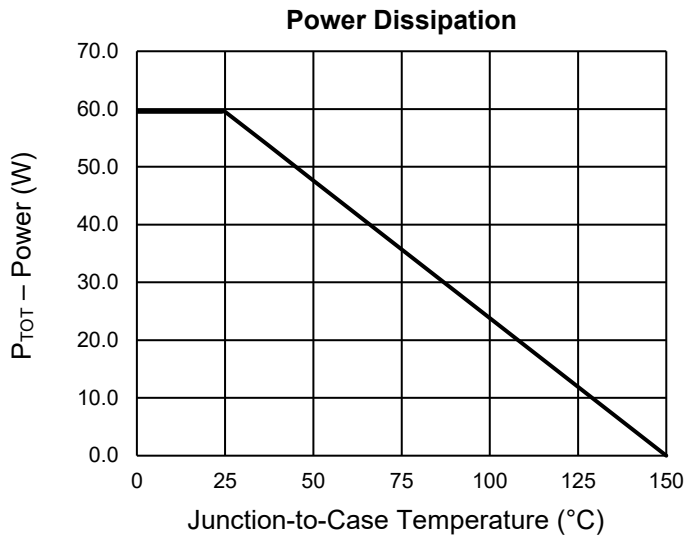


Normalized Thermal Transient Impedance, Junction-to-Case



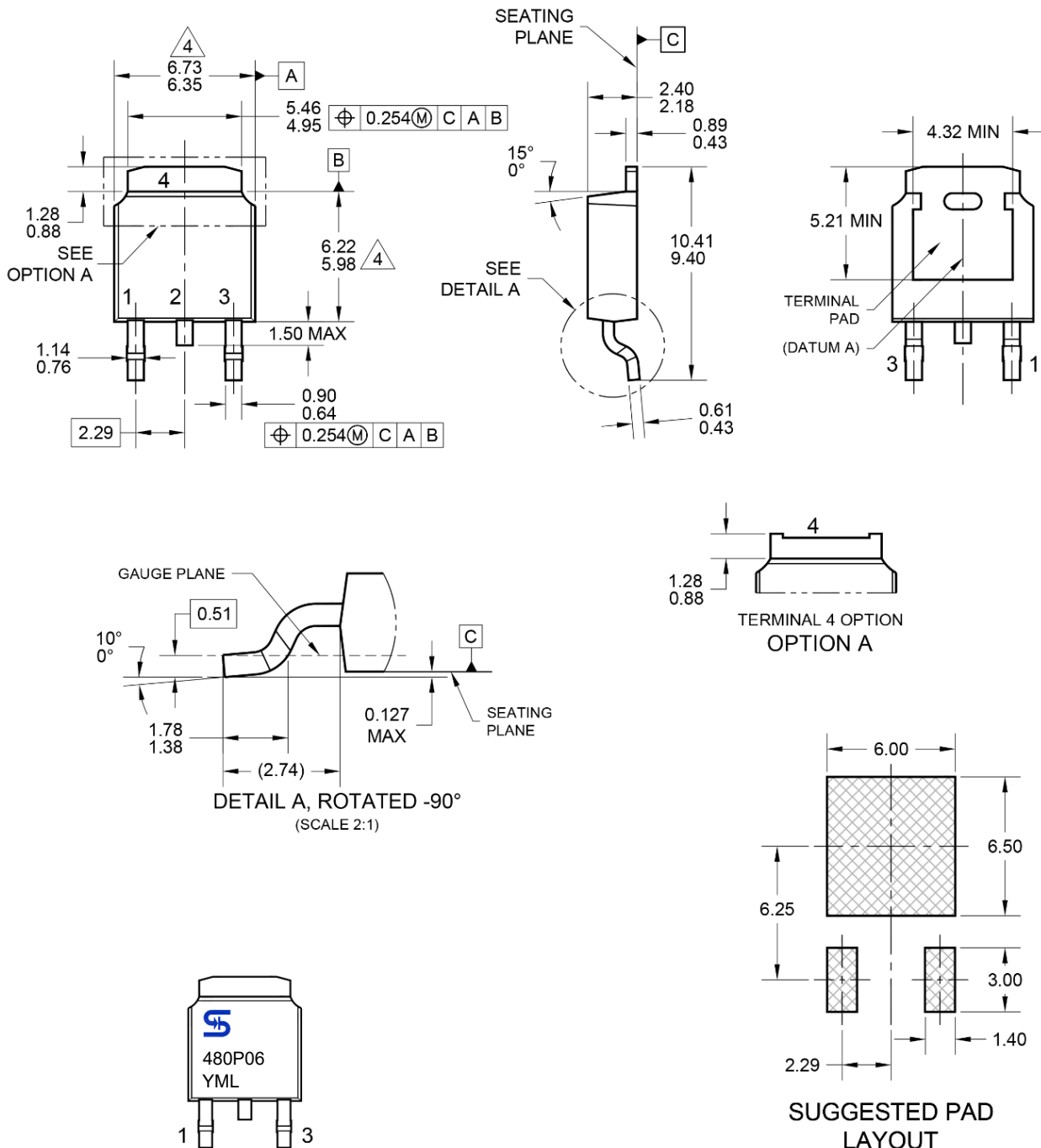
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252(DPAK)



MARKING DIAGRAM

480P06 = Device marking
Y = Year Code
M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apr, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
L = Lot Code

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
- MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
- DWG NO. REF: HQ2SD07-TO252AA-013 REV B.

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