ESP32-P4 Chip Revision v3.2 Upgrade
Chip Revision v1.3 Demand Collection and EOL Plan Description

PCN 编号 **PCN No.**	PCN202600801	**提出日期** **Issue Date of PCN**	2026/05/20
PCN 类型 **PCN Category**	☑ 客户需要批准/ Customer Approval Required ☐客户通知/ Customer Notification		

1. 受影响的物料编码/ Affected Part Number

Product Type	Part Number Planned for EOL (Previous Revision)	Recommended Upgrade Part Number (New Revision)	Key Hardware Differences
Chip	ESP32-P4NRW16	ESP32-P4NRW16X	1) Different part number 2) Different ESP32-P4 chip revision 3) Different ESP32-P4 pin definition (Pin 54) 4) ESP32-P4NRW16X adds optional in-package PSRAM material
Chip	ESP32-P4NRW32	ESP32-P4NRW32X	1) Different part number 2) Different ESP32-P4 chip revision 3) Different ESP32-P4 pin definition (Pin 54)
Development Board	ESP32-P4-Function-EV-Board	ESP32-P4X-Function-EV-Board	1) Different part number 2) Different ESP32-P4 chip revision 3) Different ESP32-P4 pin definition (Pin 54)
Development Board	ESP32-P4-EYE	ESP32-P4X-EYE	1) Different part number 2) Different ESP32-P4 chip revision 3) Different ESP32-P4 pin definition (Pin 54)

2. 停产及版本升级原因/ EOL and Chip Revision Upgrade Reasons

1) Espressif continues to improve product performance and has released the ESP32-P4 chip revision v3.2 (hereinafter referred to as the new revision). Compared with ESP32-P4 chip revision v1.3 (hereinafter referred to as the previous revision), **the new revision provides comprehensive functional upgrades in clock speed, image processing, power management, and security to better meet end-product requirements**. For more information, see: ESP32-P4 chip upgrade news.

   Therefore, Espressif recommends that users currently developing or producing with the ESP32-P4 chip revision v1.3 series products evaluate and upgrade to chip revision v3.2 as soon as possible to improve product performance and obtain more stable software and hardware support and more flexible supply assurance. Meanwhile, ESP32-P4 chip revision v1.3 is planned to enter the end-of-life (EOL) process.

2) To avoid supply risks from a single raw material and improve supply stability, ESP32-P4NRW16X adds optional in-package PSRAM material.

3. 新版本特性与性能提升/ New Revision Features and Performance Improvements

No.	Item	Previous Revision	New Revision
3.1	Chip Revision	v1.3	v3.2
3.2	Overall Performance (CPU, PSRAM)	CPU stable at 360 MHz. PSRAM interface frequency stable at 200 MHz. GUI rendering and display frame rate are limited.	ESP32-P4 chip revision v3.2 includes multiple underlying hardware enhancements. CPU frequency increases from 360 MHz to 400 MHz; PSRAM interface frequency stably supports up to 250 MHz; DMA and pixel processing accelerator (PPA) enhancements significantly improve graphics rendering and data transfer efficiency. In typical multimedia scenarios, this revision stably supports 1920×1080 / RGB888 @ 30 Hz HD display output, and at 1280×720 / RGB565 resolution, LVGL framework benchmarks can reach 40 fps, providing smoother touch and visual interaction for high-end HMI applications.
3.3	Camera Feature (MIPI-CSI, ISP, LCD_CAM DVP)	MIPI-CSI and DVP support limited byte order and format types. ISP lacks modules such as BLC; image color quality is suboptimal.	ESP32-P4 chip revision v3.2 supports more data formats and better image quality. Details are as follows: 1) MIPI-CSI supports 16-bit byte order conversion and format conversion. 2) ISP supports BLC, DPC, LSC and Crop modules, as well as a standalone WB Gain module and a multi-window AWB statistics module. 3) DVP supports 8-bit byte order conversion.
3.4	Memory Allocation	Total L2MEM after deducting 0~512 KB configurable cache usage (256~768 KB) is divided by a fixed 79 KB ROM data segment into low 183 KB, ROM data, and high (remaining 0~512 KB) three	ESP32-P4 chip revision v3.2 optimizes memory address layout. Available L2MEM (192 + 0~512 KB) is now contiguous and supports longer contiguous memory allocations.

		regions. User static or dynamic allocations cannot cross the ROM data region; maximum contiguous available memory is limited.	
3.5	Power Consumption	Lacks an independent CPU power domain and updated memory retention mode; Light-sleep power optimization is limited.	ESP32-P4 chip revision v3.2 supports shutting down the CPU power domain separately during Light-sleep, significantly optimizing active and sleep power consumption. For details, refer to ESP32-P4 Series Datasheet > "Active Mode and Low-Power Mode Power Consumption" section.
3.6	Security	1) HUK function unavailable. 2) Limited side-channel attack resistance, including: a) ECC/ECDSA: no constant-time and constant-power design. b) AES/XTS-AES accelerator lacks pseudo-round DPA resistance.	1) HUK function fixed. ESP32-P4 chip revision v3.2 can use HUK-based flash encryption key deployment in ROM and HUK features in ESP-IDF. See ESP32-P4 Series Datasheet > Key Manager section. 2) ESP32-P4 chip revision v3.2 underlying hardware enhances side-channel attack resistance, including: a) ECC/ECDSA adds constant-time and constant-power design. b) AES/XTS-AES accelerator lacks pseudo-round DPA resistance.
3.7	For more information, refer to design changes 及 ESP32-P4 Series SoC Errata.		

4. 新旧版本硬件差异/ Hardware Differences Between Previous and New Revisions

1) ESP32-P4 series products: wafer metal layer updated; chip revision upgraded from v1.3 to v3.2.
2) ESP32-P4 pin difference (Pin 54): previous revision Pin 54 is defined as NC (not connected); new revision Pin 54 is defined as the VDD_HP power pin.
3) Product part numbers differ.
4) ESP32-P4NRW16X adds optional in-package PSRAM material.

5. 新旧版本识别方法/ How to Identify Previous and New Revisions

See Appendix I: Comparison of Revision Identification and Pin Differences

6. 版本升级影响说明/ Impact of Revision Upgrade

1) 品质和性能/ Quality & Performance:

ESP32-P4 chip revision v3.2 achieves performance optimizations. See Para 3 for details.

2) 交期/ Delivery:

ESP32-P4 chip revision v1.3 series products (previous revision) are planned to enter the EOL process. If you still need the previous revision, contact the Espressif customer support team before 2026/6/30 for demand communication and supply arrangement evaluation. Espressif will fully support your product needs during the transition and ensure a smooth switch.

3) 物料编码/ Part Number:

Please place orders using the new part numbers. New revision part numbers are listed in Para 1.

4) 认证/ Certification:

ESP32-P4 series products have no RF function and do not affect RF-related testing of end products.

For end-product certification, customers are advised to consult the relevant certification body.

5) 软件/ Software:

ESP32-P4 chip revision v3.2 is not software-compatible with chip revision v1.3.

As the ESP32-P4 series upgrades to v3.2, if you currently use v1.3 or earlier, existing ESP-IDF versions may not support v3.2. To ensure compatibility, upgrade ESP-IDF to the required version or later (see the table below "Required ESP-IDF Version for ESP32-P4 Chip Revision v3.2"). After upgrading ESP-IDF, set Kconfig option ESP32P4_SELECTS_REV_LESS_V3=n, rebuild the project, and the resulting binary can run on the updated product.

Note: Even with upgraded ESP-IDF, previous and new revision products cannot run the same binary.

If you already built binaries with the required ESP-IDF version or later, no further software update is needed.

Required ESP-IDF Version for ESP32-P4 chip revision v3.2：

ESP-IDF Versions/Branches	Recommended Version	Required Version
release/v5.5	v5.5.3 or above	v5.5.3
release/v6.0	v6.0 or above	v6.0

Note: Your local esptool may not yet support the upgraded product; you may see stub crashes or connection failures. Run install in the ESP-IDF directory to get the latest esptool supporting the new product. Current latest versions: v5.3.dev3 (ESP-IDF v6.0 and above), v4.12.dev2 (ESP-IDF v5.5.3 and above).

6) 硬件兼容性/ Hardware Compatibility:

ESP32-P4 chip revision v3.2 is not hardware-compatible with chip revision v1.3. Refer to the following for hardware design:

a) For new projects that have not started PCB design:

When using ESP32-P4 chip revision v3.2 chips, refer to the ESP32-P4 Hardware Design Guidelines. Connect the new power pin (Pin 54) externally to VDD_HP.

b) For PCBs designed with ESP32-P4 chip revision v1.3, when using upgraded ESP32-P4 chip revision v3.2:

✓ PCB design must be updated:

Pin 54 must be connected to VDD_HP externally; otherwise, the normal operation of the USB, SDIO, and GMAC modules may be affected.

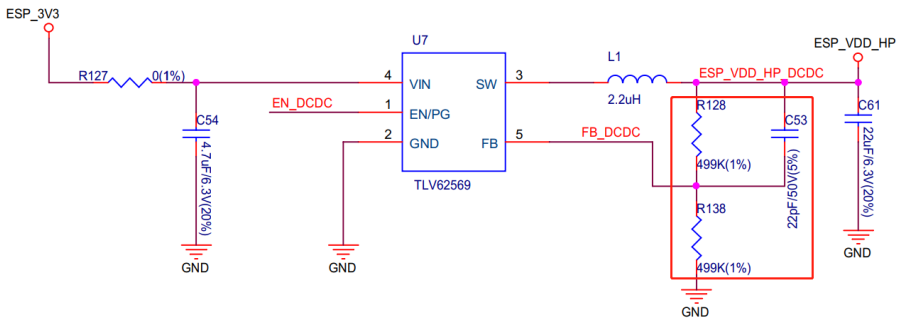
✓ Component placement must be updated:

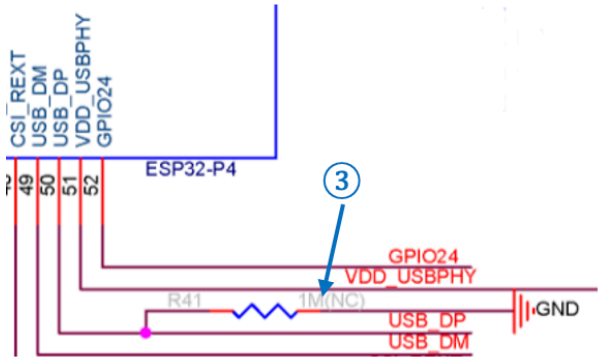
① For the DCDC connected to VDD_HP externally, **ensure both 499 kΩ feedback resistors are populated, or the chip may be damaged.**

② **Feedforward capacitor: populate 22 pF on the C53 feedforward capacitor.**

③ USB_DP pin: remove the 1 MΩ resistor.

Component placement adjustment diagram:





7) 技术文档/ Technical Documentation:

[ESP32-P4 Series Datasheet]

[ESP32-P4 Chip Revision v3.x User Guide]

[ESP32-P4 Technical Reference Manual]

[ESP32-P4 Series SoC Errata]

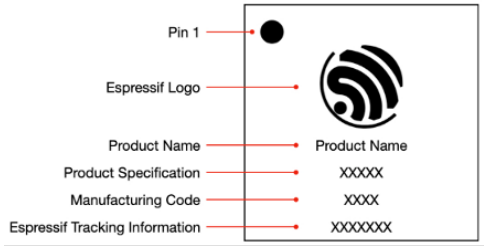
[ESP32-P4 Hardware Design Guidelines]

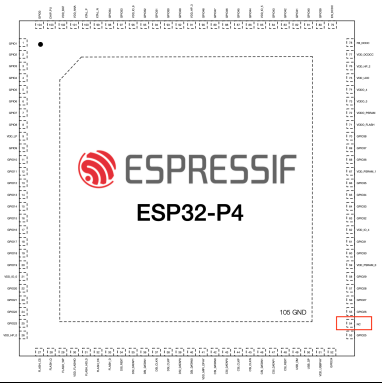
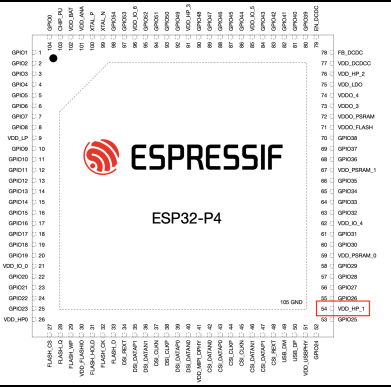
7. 给使用者的验证建议/ Verification Suggestion to Users

Before using ESP32-P4 chip revision v3.2 series products, ensure software and hardware are upgraded. For hardware design notes, see Para 6.6) Hardware Compatibility. Upgrade software to ESP-IDF v5.5.3+ or v6.0+, run install again to ensure esptool is updated. Current latest esptool versions: v5.3.dev3 (ESP-IDF v6.0 and above), v4.12.dev2 (ESP-IDF v5.5.3 and above).

If you encounter issues or have questions about this upgrade, contact Espressif customer support or your distributor. Espressif provides full technical support to help complete your upgrade. We apologize for any inconvenience and appreciate your understanding and cooperation!

Appendix I Comparison of Revision Identification and Pin Differences

1	新旧版本标识对比/ Comparison of Previous and New Revision Identification			
No.	**Item**		**Previous Revision**	**New Revision**
1.1	Chip Revision		v1.3	v3.2
1.2	eFuse 芯片版本标示位/ Chip Revision Identification by eFuse Bits			
	主版本号 Major Number	EFUSE_RD_MAC_SPI_SYS_2_REG[23]	0	0
		EFUSE_RD_MAC_SPI_SYS_2_REG[5]	0	1
		EFUSE_RD_MAC_SPI_SYS_2_REG[4]	1	1
	次版本号 Minor Number	EFUSE_RD_MAC_SPI_SYS_2_REG[3]	0	0
		EFUSE_RD_MAC_SPI_SYS_2_REG[2]	0	0
		EFUSE_RD_MAC_SPI_SYS_2_REG[1]	1	1
		EFUSE_RD_MAC_SPI_SYS_2_REG[0]	1	0
1.3	Chip Marking			
	Product Specification		NRW16 or NRW32	NRW16X or NRW32X
	Manufacturing Code		xExx	xHxx

2	产品管脚差异信息/ Pin Difference		
No.	**Item**	**Previous Revision**	**New Revision**
2.1	Chip Revision	v1.3	v3.2
2.2	Pin		
		Pin 54 is NC	Pin 54 is VDD_HP

邮件订阅
Espressif Email Notifications

乐鑫为注册用户提供电子邮件通知服务，用户可通过乐鑫订阅系统接收技术文档更新、新闻通讯、PCN 等邮件通知。
Espressif sends email notifications of technical documentation changes, along with newsletters, PCNs and other valuable information, to subscribed customers only. If you wish to stay updated on our products and services, please subscribe here.

客户响应要求
Customer Response Requirements

需客户批准的变更/ Change Requiring Customer Approval：

a) 客户须在乐鑫发出 PCN 后的 30 天内告知乐鑫已收到 PCN。如客户未在接收到 PCN 后的 30 天内告知已收到，则视为客户收到变更。
Customers are requested to acknowledge receipt of the PCN within 30 calendar days from the date of issue of the PCN. Customers would be considered as notified 30 calendar days after issue of the PCN if no acknowledgement is received.

b) 自发布 PCN 之日起 90 天内，客户没有任何其他反馈，则表示客户接受该 PCN。
The lack of any additional responses from customers within 90 calendar days from the date of issue of the PCN constitutes acceptance of the proposed changes.

客户通知/ Customer Notification：

a) 客户需在乐鑫发出 PCN 后 14 天内通知乐鑫收到该 PCN。如客户未在接收到 PCN 14 日反馈乐鑫，则视为客户确认该 PCN。
Customers are requested to acknowledge receipt of the PCN within 14 calendar days from the date of issue of the PCN. Customers would be considered as having acknowledged the PCN if no response is received after 14 calendar days.

客户批准/确认信息
Customer Approval / Acknowledgement and Remarks

客户公司全称： Customer's Company Name:			
PCN 评审结果 PCN Review Result	☐批准/确认 Accepted / Acknowledged ☐不批准 Rejected ☐需要分析 Further Analysis Required		
客户意见/ Comment:			
公司代表人姓名 Representative's Name		公司代表人职责 Representative's Job Title	
公司代表人签名 Representative's Signature		日期 Date	